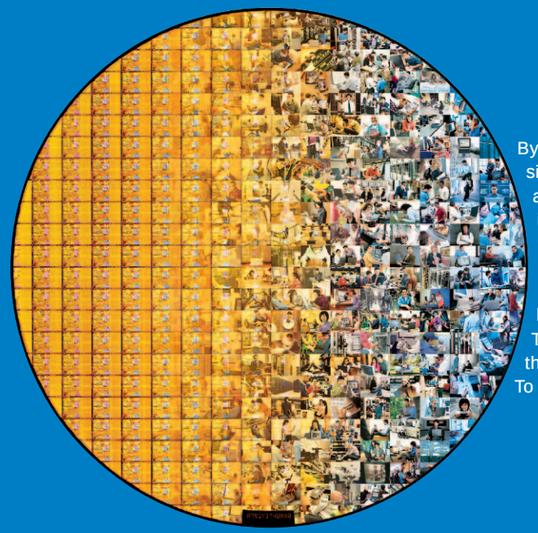

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industry forward,
we help empower
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To enhance their
knowledge.
To strengthen
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To change the world.

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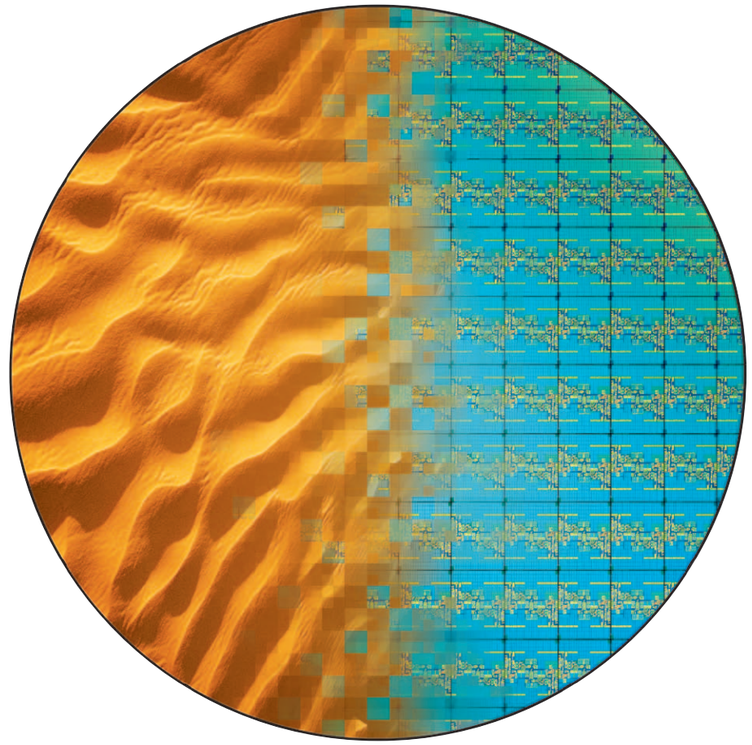
From sand to circuits



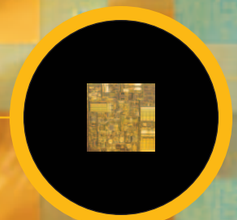
How Intel makes integrated circuit chips

From sand  to circuits

Revolutionary

They are small, about the size of a fingernail. Yet tiny silicon chips like the Intel® Pentium® 4 processor that you see here are changing the way people live, work, and play.

This Intel® Pentium® 4 processor contains more than 50 million transistors.



Today, silicon *chips* are everywhere — powering the Internet, enabling a revolution in mobile computing, automating factories, enhancing cell phones, and enriching home entertainment. Silicon is at the heart of an ever expanding, increasingly connected digital world.

The task of making chips like these is no small feat. Intel's manufacturing technology — the most advanced in the world — builds individual *circuit* lines 1,000 times thinner than a human hair on these slivers of silicon. The most sophisticated chip, a *microprocessor,* can contain hundreds of millions or even billions of *transistors* interconnected by fine wires made of copper. Each transistor acts as an on/off switch, controlling the flow of electricity through the chip to send, receive, and process information in a fraction of a second.

Explore this brochure to learn how Intel makes silicon chips — the most complex devices ever manufactured. If you are unfamiliar with a technical term, check the "Terminology" section at the end of the brochure. Words that are italicized in the text are defined there.

From sand  to circuits

Design

Silicon chip manufacturing starts with a design, or a blueprint. Intel considers many factors during this phase. What type of chip is needed and why? How many transistors can be built on the chip? What is the optimal chip size? What technology will be available to create the chip? When does the chip need to be ready? Where will it be manufactured and tested?

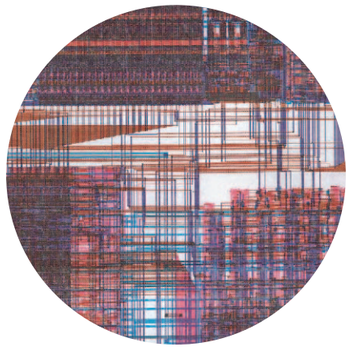
To answer these questions, Intel works with customers, software companies, and Intel's marketing, manufacturing, and testing staff. Intel design teams take this input and begin the monumental task of defining a chip's features and design.

When the specifications for the chip are ready, Intel creates *schematics,* symbolic representations of the millions of transistors and interconnections that control the flow of electricity through a chip. After this phase is complete, designers create physical representations of each layer of the chip and its transistors. These stencil-like patterns, or *masks,* are used to protect parts of a chip from ultraviolet light during a fabrication process called *photolithography.*

This Intel® Pentium® 4 processor contains more than 50 million transistors.

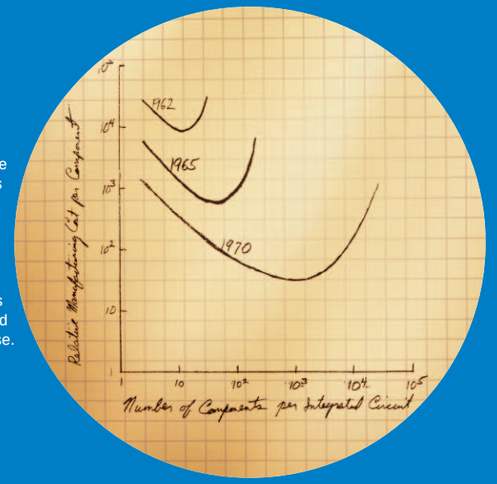
To complete the design, testing, and simulation of a chip, Intel uses sophisticated *computer-aided design (CAD)* workstations. CAD helps designers work quickly, create more complex designs, and perform comprehensive simulations and testing. For example, when simulating chip functions, the system tests not only how transistors turn on and off, but how the chip will be used to perform an action, such as launching a computer operating system.

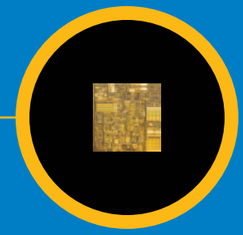
After extensive testing and fine-tuning, the chip is ready for fabrication. It takes an average of 200 people working full time for two years to design, test, and ready a new chip design for fabrication.



Intel creates thousands of schematics to design a new chip.

In 1965, Gordon Moore sketched out his prediction of the pace of silicon technology. Decades later, "Moore's Law" remains true, driven largely by Intel's unparalleled silicon expertise.





Moore's Law

Moore's Law states that the transistor density on integrated circuits doubles about every two years. Moore's Law has been amazingly accurate over time. In 1971, the Intel 4004 processor held 2,300 transistors. In 2005, the Intel® Itanium® processor held more than 1 billion transistors. Intel continues to drive Moore's Law, increasing functionality and performance, and helping to bring growth to industries worldwide.

†Note: Vertical scale of illustration not proportional to actual transistor count.

From sand  to circuits

Fabrication

The process for making chips is called *fabrication,* and the factories where they are made are called fabrication facilities, or *fabs*. The “recipe” for fabricating a chip varies depending on the chip’s proposed use. Intel uses a variety of ingredients and performs as many as 300 steps that use chemicals, gas, or light to complete fabrication.

A sandy start

It all starts with *silicon*. Intel builds chips in batches on *wafers* made of ultra-pure silicon, the principal ingredient of common beach sand. Intel uses silicon because it is a natural *semiconductor* that oxidizes easily. This means that unlike insulators such as glass (that always resist the passage of electrons) or conductors such as copper (that generally let electrons pass through), you can alter silicon to be a conductor or an insulator.

To make wafers, silicon is chemically processed so that it becomes 99.9999% pure. The purified silicon is melted and grown into long, cylindrical *ingots*. The ingots are then sliced into thin wafers that are polished until they have flawless, mirror-smooth surfaces. When Intel first began making chips, the company used 2-inch wafers. Now the company uses both 300-millimeter (12-inch) wafers and 200-millimeter (8-inch) wafers, resulting in larger yields and decreased costs.

Layer by layer

Intel uses a photolithographic “printing” process to form a chip’s multi-layered transistors and electrical passages, or interconnects, on a wafer.

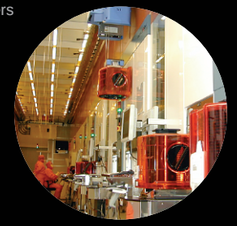
Wafer sort

The final step of fabrication is *wafer sort,* an electrical test that identifies nonfunctioning chips. A computer completes a series of tests to ensure that chip circuits meet specifications to perform as designed.

Sand | Silicon Ingot | Wafer

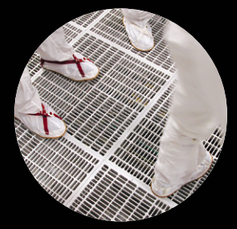
Silicon, the most abundant element on earth except for oxygen, is used because it is a natural semiconductor.

Intel manufactures chips on wafers made of ultra-pure silicon.

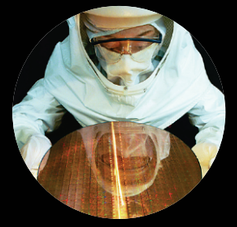


FOUPs carry 300mm wafers in an automated fab.

Highly trained technicians monitor each phase of chip fabrication.



Purified air recirculates through ceiling and floor tiles.



Many Intel fabs use 300mm (12-inch) wafers to make chips.

Fabs

Intel fabs are among the most technically advanced manufacturing facilities in the world. Within these sophisticated fabs, Intel makes chips in a special area called a *cleanroom*. Because invisible particles of dust can ruin the complex circuitry on a chip, cleanroom air must be ultra-clean. Purified air is constantly recirculated, entering through the ceiling and exiting through floor tiles.

Technicians wear a special suit, commonly called a bunny suit, before they enter a cleanroom. This helps keep possible contaminants such as lint and hair off the wafers. In a cleanroom, a cubic foot of air contains less than one particle measuring 0.5 micron (millionth of a meter) across or larger. That’s thousands of times cleaner than a hospital operating room.

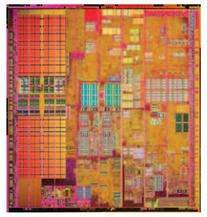
Automation also plays a critical role in a fab. Batches of wafers are kept clean and processed quickly and efficiently as they travel through the fab inside *front-opening unified pods (FOUPs)* on an overhead monorail. Each FOUP receives a barcode tag that identifies the recipe that will be used to make its chips. This labeling ensures correct processing at each step of fabrication. In 300mm fabs, a FOUP contains up to 25 wafers and weighs more than 25 pounds. Production automation allows for this FOUP weight, which is too heavy to be handled manually by a technician.

From sand  to circuits

Process

The process of building transistors on a computer chip is precise and complex. The following provides a summary of the major steps.

Insulating and coating > An insulating layer of *silicon dioxide* is “grown” on top of a polished silicon wafer in a furnace at very high temperatures in the presence of oxygen. The wafer is then coated with a light-sensitive substance called *photoresist* that, like photographic film, chemically changes when exposed to ultraviolet light.



A completed die contains millions of circuits that appear as an intricate pattern.

Masking > The masks created during the design phase define the circuit pattern on each layer of a chip. A very complex machine called a stepper aligns the mask to the wafer. The stepper flashes ultraviolet light through the exposed places in the mask. The portions of the photoresist exposed to light become a soluble, gooey layer.

Etching > The exposed portions of photoresist are removed, revealing part of the silicon dioxide layer underneath. This revealed silicon dioxide is removed through a process called *etching*. Then the remaining photoresist is removed, leaving a pattern of silicon dioxide on the silicon wafer.

Adding layers > Additional materials such as *polysilicon,* which conducts electricity, are deposited on the wafer through further masking and etching steps. Each layer of material has a unique pattern. Many layers are deposited across the wafer and then removed in small areas to create transistors and interconnects. Together, they will form the chip’s circuitry in a three-dimensional structure.

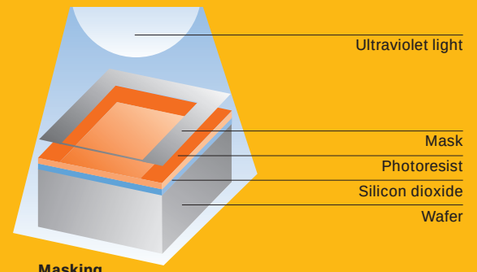
Doping > In an operation called *doping,* the exposed areas of the silicon wafer are bombarded with various chemical impurities called ions, altering the way the silicon in these areas conducts electricity. Doping is what turns silicon into silicon transistors. Doping helps transistors turn on and off — the two states that represent *binary* 1s and 0s. Binary notation is translated into letters, numbers, colors, and graphics, and provides the basis for storing information in a computer.

Creating contacts > To provide a link to the additional layers put on the wafer, electrical “contacts” are formed by repeating masking and etching steps.

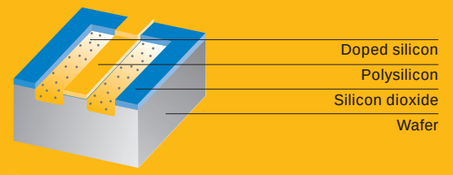
Adding metal > Multiple layers of metal are applied to form the electrical connections between the chip’s layers. Intel uses copper in this process because of its low resistance and because it can be cost-effectively integrated into the manufacturing process.

Completing the wafer > A completed wafer contains millions of transistors. A transistor acts as a switch, either preventing or allowing electrical current to pass through. A positive charge fed to a transistor’s *gate* attracts electrons. This gate creates a channel between the transistor’s *source* and *drain* through which electrical current flows. A negative charge at the gate prevents the current from being able to flow through.

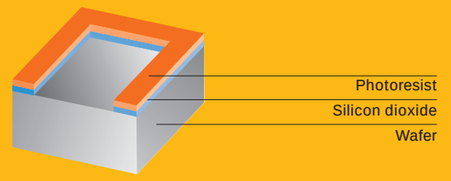
The microscopic size of circuits allows Intel to fit more transistors on a chip and decrease the distance that electricity has to travel. The result is a high-performance chip with more capabilities.



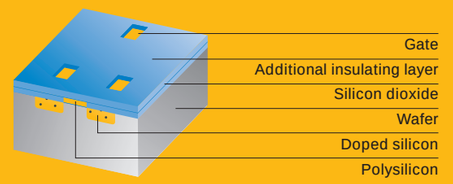
Masking



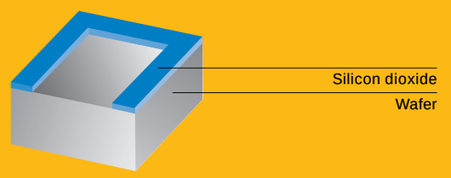
Doping



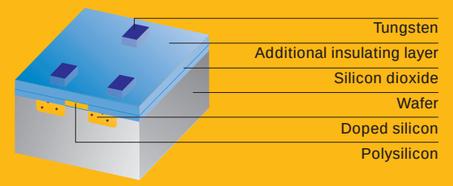
After etching



Creating contacts

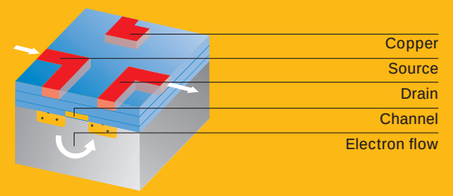


After removing photoresist



Adding metal

Adding layers



Completing the wafer

Packaging

After being sorted, wafers arrive at an Intel assembly facility, where a precision saw separates each wafer into individual chips called *die*. Each functioning die is then assembled into a package that, in addition to protecting a die, delivers critical power and electrical connections to the main circuit board on a computer. It is this final "package" that is ultimately placed directly on a computer circuit board or in other devices such as cell phones and personal digital assistants (PDAs).

As processor technologies advance, the demands on packaging to support and optimize the technologies increase. Because Intel makes chips that have many different applications, the company uses a variety of packaging technologies.

High-performance packages

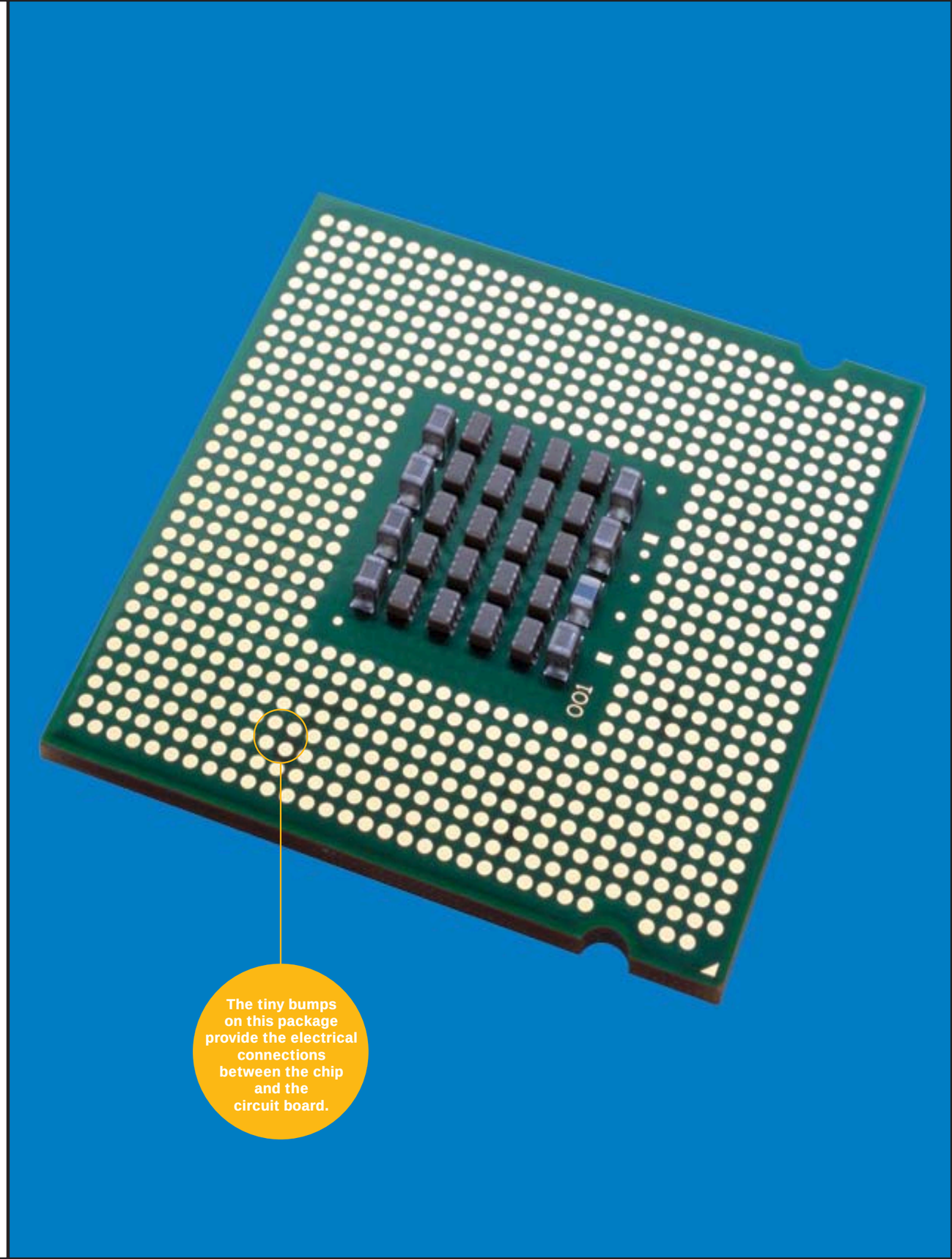
Flip-chip packaging > This is an example of one of the advanced packages that Intel uses. To package the die, Intel begins by attaching tiny metal bumps on the die surface to the supporting base, or substrate of the package, completing an electrical connection from the chip to the package. These chips are called "flip chips" because the silicon die are "flipped" to their front side for this attachment method, as opposed to other types of packaging that attach the back of the die. Intel uses an organic, or polymer, substrate to enable higher performance copper electrical interconnections from the die to the circuit board. A compliant material is then added between the substrate and die to manage mechanical stress. In the last step, another material, called a heat spreader, is attached to help disperse the heat generated by the chip during normal use.

Wire bond for *stacked-chip packaging* > This family of innovative packaging technology results in packages that are only slightly larger than the multiple silicon die that they contain. Intel stacks multiple memory and logic die in a single package to increase performance and maximize space, which are both critical in today's handheld devices. When attaching the die, Intel uses a special material that is optimized for mechanical, thermal, and electrical performance to "glue" the first die to the substrate. The other die are then stacked and "glued" to each other to create a combination of chips that meet product performance goals.

After the die are attached, sophisticated tools bond extremely fine wires from each die to the substrate. This process, called *wire bonding,* is repeated for each die included in the stack until all die are electrically connected to the same package. The die are then encapsulated with a molding process and protective coating that flows into the narrow spaces between the die and the package. Lastly, Intel attaches specialized alloy "balls" to the package bottom to electrically connect the package to the circuit board.

One more check

Intel performs reliability and electrical "tests" on each completed unit. The company verifies that the units perform at their designed speed across a range of temperatures. Because chips may end up in items ranging from automobile engines to spacecraft and laptops, they must be able to withstand a variety of environmental stresses. Upon approval, chips are electrically coded, visually inspected, packaged in protective shipping material, and prepared for shipment to Intel customers.



The tiny bumps on this package provide the electrical connections between the chip and the circuit board.

From sand  to circuits

Innovation

Intel's advanced computer chip technology and high-volume production help power the digital economy and provide the foundation for the next generation of computing. Intel expects to continue to push the leading edge of Moore's Law well into the future.

New technologies offer exciting opportunities. For example, multi-core processors — chips with multiple "brains" — enable a new era of computing and allow computers to simultaneously manage many different activities. Multi-core processors can significantly improve performance without increasing power consumption, which is an important consideration in the design and manufacturing of today's chips. Similarly, as the number of transistors per chip increases according to Moore's Law, Intel continues to add new features and enhance the functionality of these tiny silicon "engines" that drive the worldwide digital revolution.

As computing, communications, and consumer electronics come together in an era of convergence of multi-feature, interoperating devices, Intel will continue to deliver innovation.

Intel's advanced chips and manufacturing are helping to bring together the best of computing, communications, and consumer electronics to enable broader and ever more valuable benefits from technology.

From sand  to circuits

Terminology

Binary > Having two parts. The binary number system that computers use is composed of the digits 0 and 1.

Bipolar > A fast but relatively expensive technology. Used for Intel's first product, the 3101 memory component.

Chip > A tiny, thin square or rectangle that contains integrated electronic circuitry. Chips are built in batches on wafers of silicon. A chip is also referred to as a die. The most sophisticated chip is a microprocessor. See also "Microprocessor."

Circuit > A path through which electrical current can flow.

Cleanroom > The sterile room where chips are fabricated. The air in these rooms is thousands of times cleaner than that in a typical hospital operating room.

CMOS (complementary metal oxide semiconductor) **>** Combines both positive- and negative-channel transistors on the same circuit design. Yields circuits that consume relatively low amounts of power. Currently, most of Intel's chips are built using this technology.

Computer-aided design (CAD) **>** Sophisticated computerized workstations and software used to design integrated circuit chips.

Die > See "Chip" and "Microprocessor."

Doping > A wafer fabrication process in which exposed areas of silicon are bombarded with chemical impurities to alter the way the silicon in those sections conducts electricity.

Drain > A highly doped region adjacent to a transistor's current-carrying channel. Carries electrons out of the transistor to the next circuit element or conductor.

Etching > The removal of selected portions of materials to define patterned layers on chips.

Fabrication > The process of making chips.

Fab > A shortened term for fabrication facility, where Intel manufactures silicon chips.

Flip-chip packaging > A type of chip package that "flips" a chip to its front side and attaches it to the package, as opposed to packaging such as wirebond that attaches the back of the die to the package.

Front-opening unified pod (FOUP) **>** A container that is part of an automated system in a fab that holds and transports wafers. The color of a FOUP identifies whether the wafers contain copper or aluminum. Orange holds copper; green holds aluminum.

Gate > The input control region of a transistor where a negative or positive charge is applied.

Ingot > A cylinder-shaped chunk of nearly pure silicon from which silicon wafers are sliced.

Mask > A quartz plate with a stencil-like pattern etched in chrome. Used during wafer fabrication to "print" layered circuit patterns on a chip.

Microprocessor > The "brain" of a computer. Multiple microprocessors working together are the "hearts" of servers, communications products, and other digital devices. See also "Chip."

Nanometer > One billionth of a meter.

NMOS (negative-channel metal oxide semiconductor) **>** The preferred technology for leading-edge chips in the 1970s and early 1980s. Less expensive and denser than bipolar technology, and faster than PMOS technology.

Photolithography > The process of reproducing the chip's circuitry pattern onto the wafer surface using masks to transfer the image photomechanically.

Photoresist > A substance that becomes soluble when exposed to ultraviolet light. Used to help define circuit patterns during chip fabrication.

Pin grid array (PGA) **>** A packaging technology used primarily for high-performance microprocessors.

PMOS (positive-channel metal oxide semiconductor) **>** A slow, now obsolete technology that was used for Intel's earliest MOS products.

Polysilicon > Short for polycrystalline silicon, or silicon made up of many crystals. This conductive material is used as an interconnect layer on a chip.

Schematic > A diagram that represents a circuit's logical behavior.

Semiconductor > A material (such as silicon) that can be altered to either conduct electrical current or block its passage.

Silicon > The element used to make the wafers upon which chips are fabricated. It is a natural semiconductor and is the most common element on earth except for oxygen.

Silicon dioxide > Grown or deposited on a wafer during chip fabrication to serve as an insulating layer. Glass is a common form of silicon dioxide.

Source > The region of a transistor where electrons move into the channel.

Surface-mount technology (SMT) **>** A package that allows chips to be mounted on the surface rather than through holes on a printed circuit board.

Stacked-chip packaging > Packages that contain multiple die stacked in a single package.

Transistor > A type of switch that controls the flow of electricity. A chip may contain millions or billions of transistors.

Wafer > A thin piece of silicon sliced from a cylindrical crystal ingot. Used as the base material for building integrated circuits.

Wafer sort > An electrical test procedure that identifies the chips on a wafer that are not fully functional.

Wire bonding > The process of connecting extremely thin wires from a chip's bond pads to leads on a package.

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