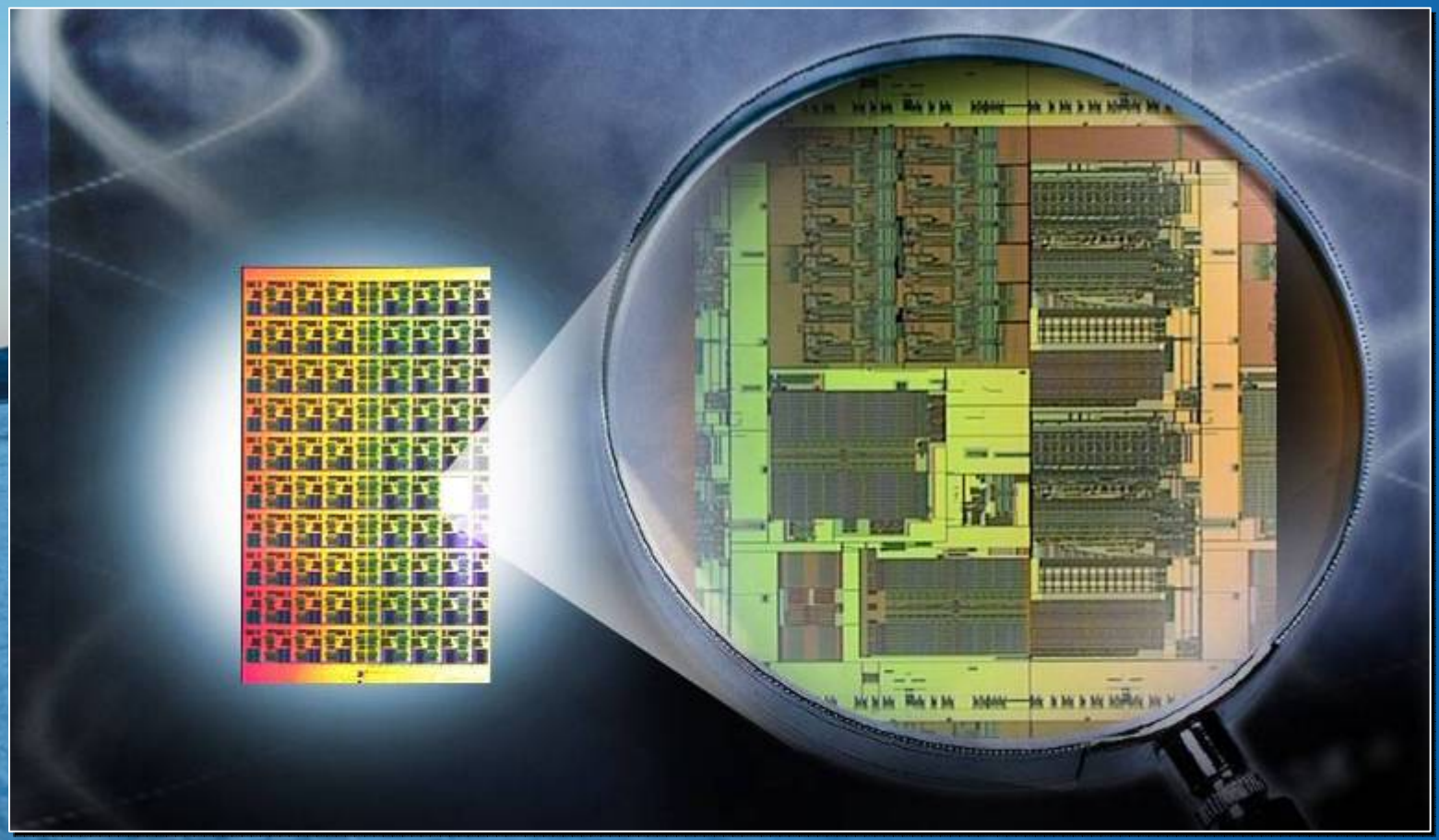
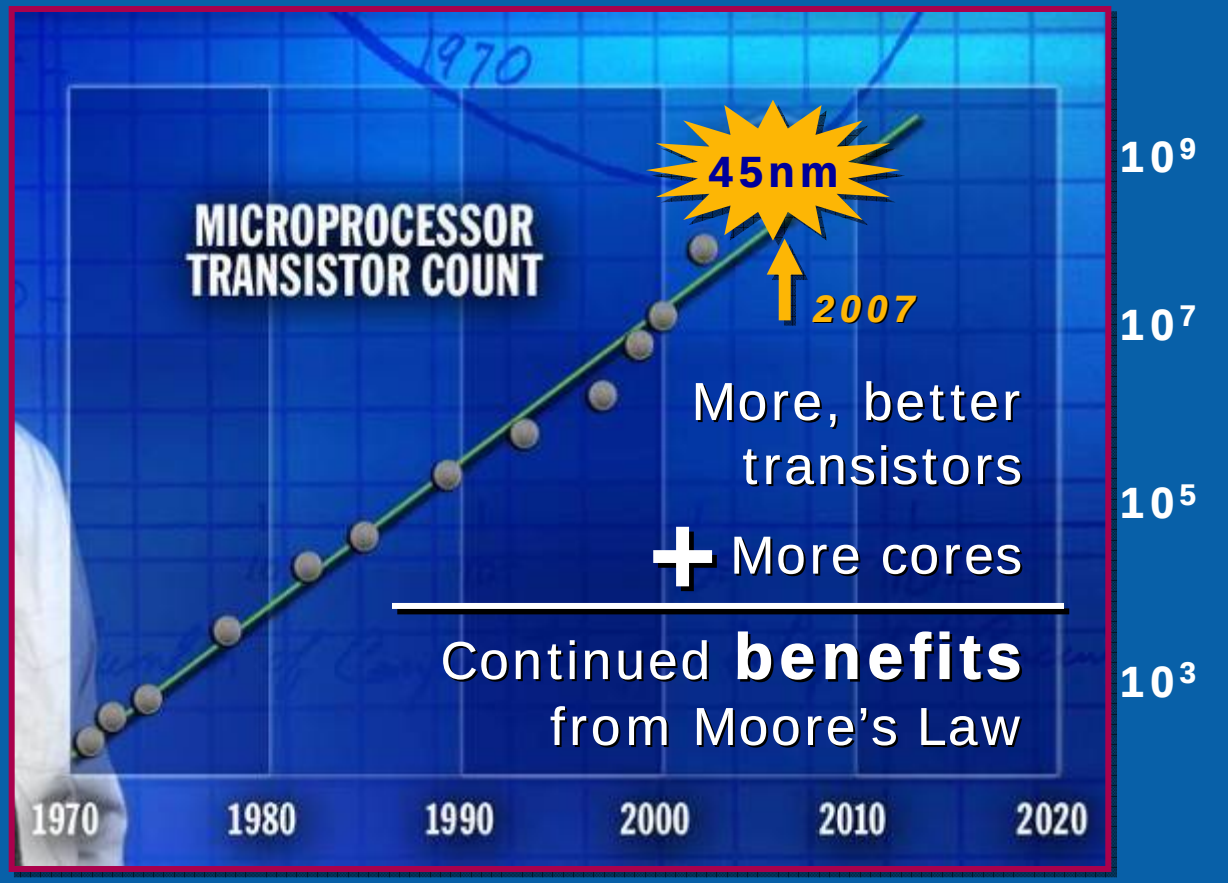
Teraflops Research Chip

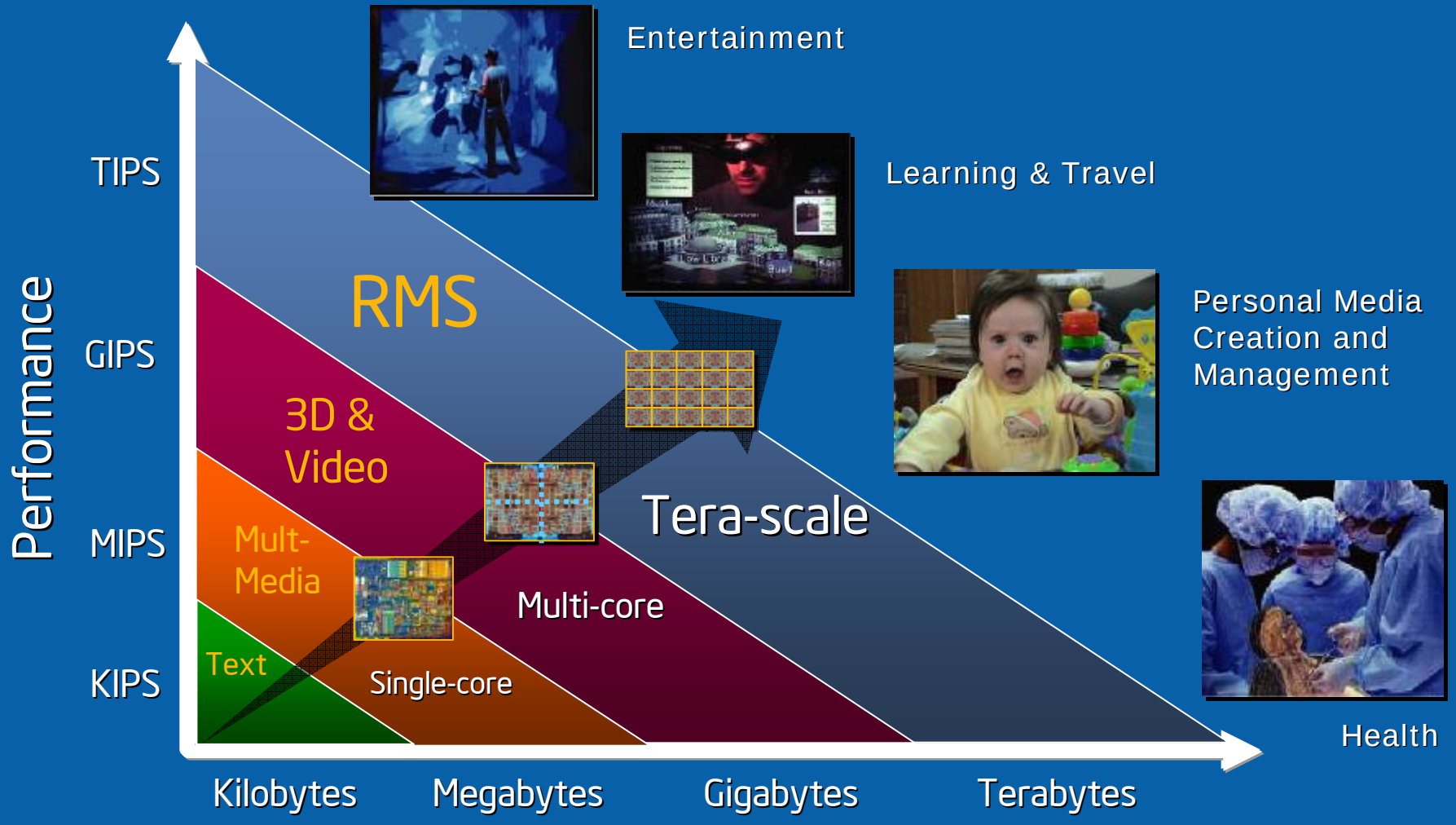


Moore's Law Motivates Multi-Core



What is Tera-scale?

Teraflops of performance operating on Terabytes of data



Intel Tera-scale Research

100+ Research Projects Worldwide

Microprocessor

Examples:

Scalable memory
Multi-core architectures
Specialized cores
Scalable fabrics
Energy efficient circuits

Platform

Examples:

3D Stacked Memory
Cache Hierarchy
Virtualization/Partitioning
Scaleable OS's
I/O & Networking

Programming

Examples:

Speculative Multithreading
Transactional memory
Workload analysis
Compilers & Libraries
Tools

ACCELERATE TRANSITION TO PARALLEL PROGRAMMING

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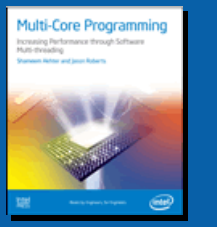


A Historical Perspective: ASCI Red

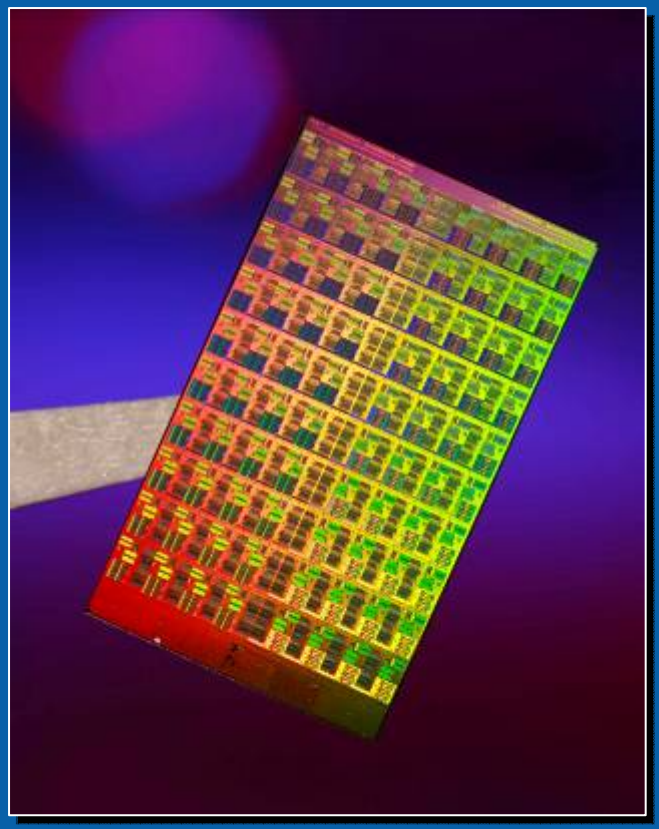
1996: First Teraflops Supercomputer Developed by Intel for Sandia National Lab

- 104 cabinets, over 2500sq feet
- Almost 10,000 Pentium® Pro processors
- Consumed 500kw

Source: Intel, 1996

Teraflops Research Chip

100 Million Transistors • 80 Tiles • 275mm^2



First tera-scale programmable silicon:

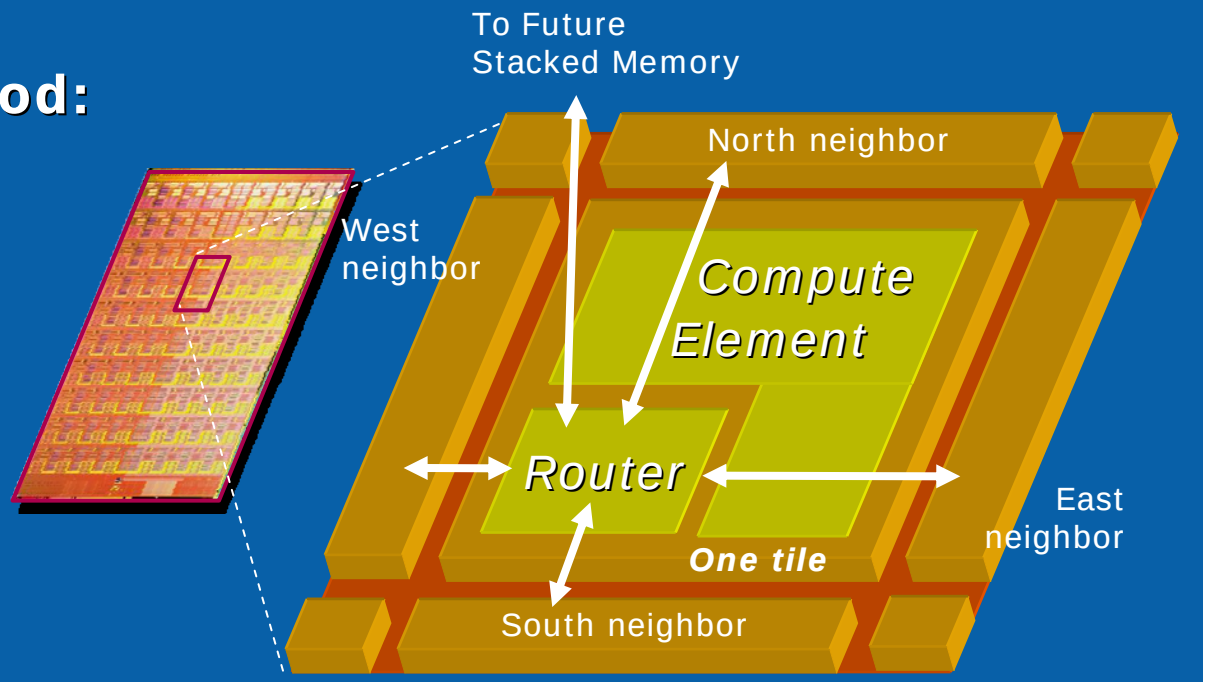
- Teraflops performance
- Tile design approach
- On-die mesh network
- Novel clocking
- Power-aware capability
- Supports 3D-memory

Not designed for IA or product

Tiled Design & Mesh Network

Repeated Tile Method:

- Compute + router
- Modular, scalable
- Small design teams
- Short design cycle



Mesh Interconnect:

- "Network-on-a-Chip"
  - Cores networked in a grid allows for super high bandwidth communications in and between cores
- 5-port, 80GB/s* routers
- Low latency (1.25ns*)
- Future: connect IA/or and special purpose cores

* When operating at a nominal speed of 4GHz

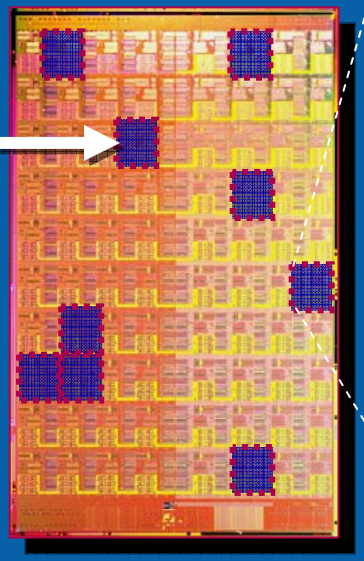
Fine Grain Power Management

- Novel, modular clocking scheme saves power over global clock
- New instructions to make any core sleep or wake as apps demand
- Chip Voltage & freq. control (0.7-1.3V, 0-5.8GHz)

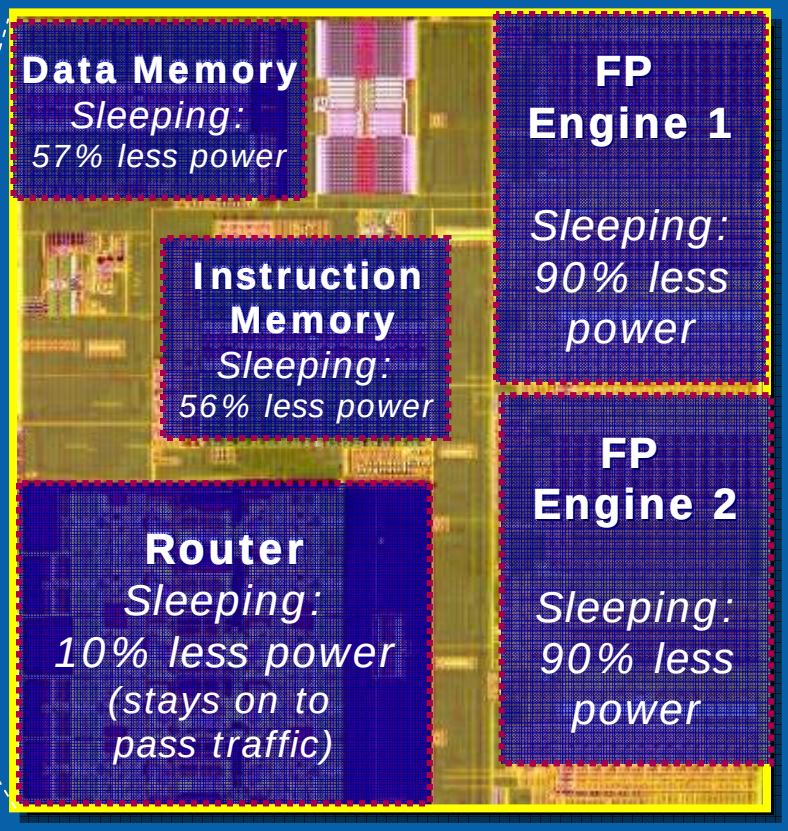
Dynamic sleep

STANDBY:
- Memory retains data
- **50%** less power/tile

FULL SLEEP:
- Memories fully off
- **80%** less power/tile



21 sleep regions per tile *(not all shown)*

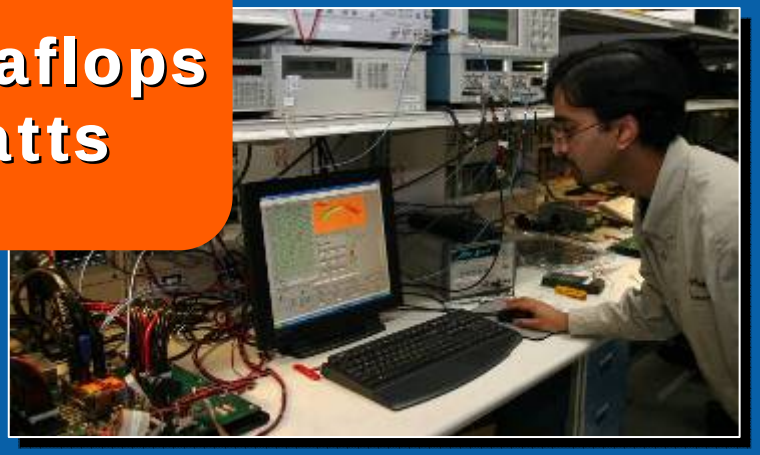


Industry leading energy-efficiency of 16 Gigaflops / Watt

Research Data Summary

Frequency	Voltage	Power	Bisection Bandwidth	Performance
3.16 GHz	**0.95 V**	**62W**	**1.62 Terabits/s**	**1.01 Teraflops**
5.1 GHz	1.2 V	175W	2.61 Terabits/s	1.63 Teraflops
5.7 GHz	1.35 V	265W	2.92 Terabits/s	1.81 Teraflops

1.01 Teraflops
62 Watts

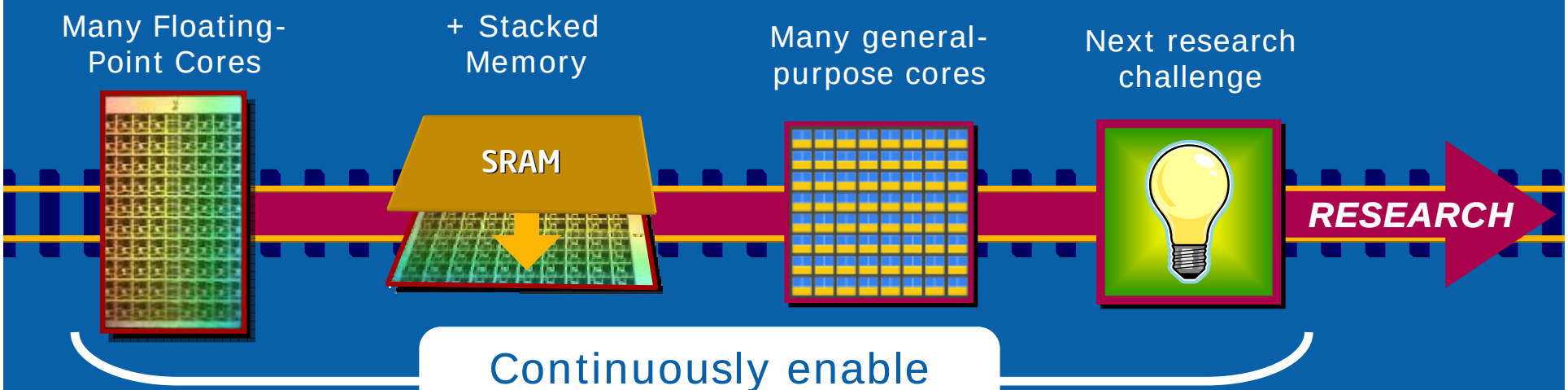


Application Performance

At 1.07V, 4.27GHz operation:

Application Kernels	FLOP count	Teraflops @ 4.27GHz	% Peak Teraflops
Stencil – PDE Solver	358K	1.00	73.3%
SGEMM: Matrix Multiplication	2.63M	0.51	37.5%
Spreadsheet	62.4K	0.45	33.2%
2D FFT	196K	0.02	2.73%

What's Next?



Continuously enable new tech 5-10 years out

Research Labs

Product Groups