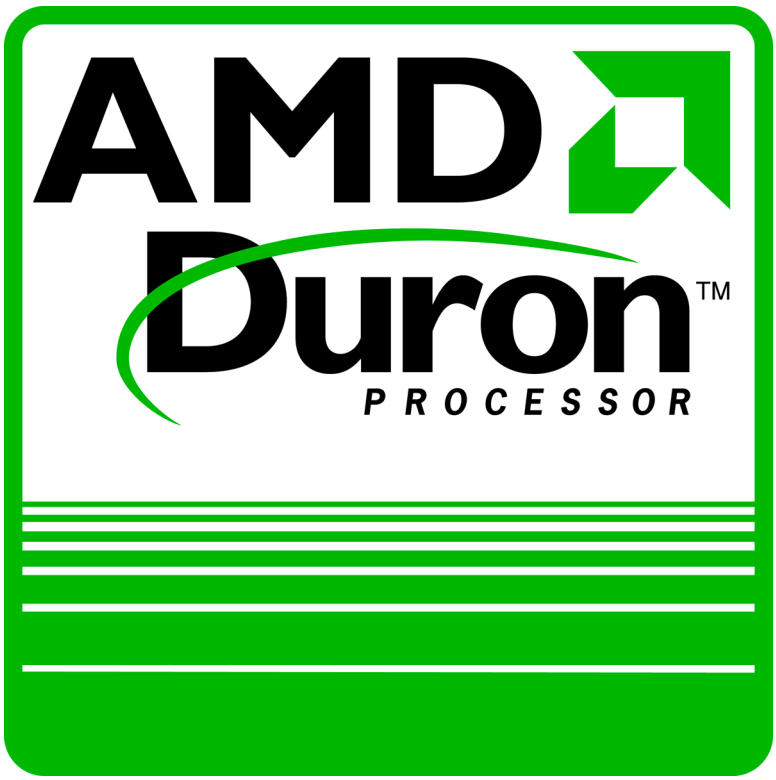
AMD

AMD Duron™ Processor
Revision Guide



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AMD Duron™ Processor Revision Guide

The purpose of the *AMD Duron™ Processor Revision Guide* is to communicate updated product information on the AMD Duron processor to designers of computer systems and software developers. This guide consists of four sections:

- **Product Marking Identification:** This section, which starts on page 2, provides product types, product revisions, OPNs (Ordering Part Numbers), and product marking information.
- **Product Errata:** This section, which starts on page 3, provides a detailed description of product errata, including potential effects on system operation and suggested workarounds. An erratum is defined as a deviation from the product's specification. A product errata may cause the behavior of the AMD Duron processor to deviate from the published specifications.
- **Revision Determination:** This section, which starts on page 7, shows the AMD Duron processor identification numbers returned by the CPUID instruction for each revision of the processor.
- **Technical and Documentation Support:** This section, which starts on page 8, provides a listing of available technical support resources. It also lists corrections, modifications, and clarifications to listed documents.

Revision Guide Policy

Occasionally AMD identifies deviations from or changes to the specification of the AMD Duron processor. These changes are documented in the *AMD Duron Processor Revision Guide* as errata. Descriptions are written to assist system and software designers in using the AMD Duron processor and corrections to AMD's documentation on the AMD Duron processor are included. This release documents currently characterized product errata.

1 Product Marking Identification

1.1 Production Marking

PGA OPN

D 700 A S T 1 B

Max FSB: A = B = 200 MHz
Size of L2 Cache: 1=64 Kbytes, 2=128 Kbytes
Case Temperature: Q=60ºC, X=65ºC, R = 70°C, Y=75ºC, T=90ºC
Operating Voltage: S = 1.5V, U = 1.6V, P = 1.7V, N = 1.8V
Package Type: M = Card Module, A = PGA
Speed: 550=550 MHz, 600=600 MHz, 650=650 MHz, 700=700 MHz, etc.
Family/Architecture: D = AMD Duron™ Processor Architecture

Note: Spaces are added to the number shown above for viewing clarity only.

2 Product Errata

This section documents AMD Duron processor product errata. The errata are divided into categories to assist referencing particular errata. A unique tracking number for each erratum has been assigned within this document for user convenience in tracking the errata within specific revision levels. Table 1 cross-references the revisions of the processor to each erratum. An "X" indicates that the erratum applies to the stepping. The absence of an "X" indicates that the erratum does not apply to the stepping.

Note: *There can be missing errata numbers. Errata that have been resolved from early revisions of the processor have been deleted, and errata that have been reconsidered may have been deleted or renumbered.*

Table 1. Cross-Reference of Product Revision to Errata

Errata Numbers and Description	Revision Numbers	
	A0	A2
3 CPUID Instruction Reports Incorrect L2 Cache Size	X	
5 MCA Bus Unit Control Register MSR 408H Returns Incorrect Information	X	X
10 Resistance Value of the ZN and ZP Pins	X	

3 CPUID Instruction Reports Incorrect L2 Cache Size

Products Affected. A0

Normal Specified Operation. The CPUID instruction should report a 64-Kbyte L2 Cache using extended function 8000_0006h.

Non-conformance. The CPUID instruction reports an incorrect L2 cache size as 1 Kbytes.

Potential Effect on System. System software that relies on the CPUID instruction for L2 cache information may not behave as expected.

Suggested Workaround. For Revision A0, system software should assume a 64-Kbyte L2 cache size. See Technical Note TN13—*AMD Duron™ Processor Rev. A0: CPUID Reporting of L2 Cache Size*.

Resolution Status. Fixed in a future revision.

5 MCA Bus Unit Control Register MSR 408H Returns Incorrect Information

Products Affected. A0, A2

Normal Specified Operation. System reads to MSR 408h, MCA Bus Unit Control Register MC2_CTL, should return correct information—the lower 32 bits in EAX and all zeros for the upper 32 bits in EDX.

Non-conformance. A read to the Machine Check Architecture (MCA) Bus Unit Control MSR 408h (MC2_CTL) returns incorrect information in EDX. It returns the information stored in the upper 32 bits of the BU Status MSR 409h (MC2_STATUS) instead.

Potential Effect on System. If the system reads this MCA control register, the upper 32 bits, which are reported in EDX, can contain unexpected data.

Suggested Workaround. This register is only implemented as a 32-bit register. Ignore the upper 32 bits which are reported in EDX.

Resolution Status. No fix planned.

10 Resistance Value of the ZN and ZP Pins

Products Affected. A0

Normal Specified Operation. The ZN and ZP pins are specified such that the AMD system bus output drivers autocompensate to whatever resistance value is applied between ZN and VDD and ZP and VSS.

Non-conformance. The AMD system bus driver impedance is approximately 20 ohms higher than the applied resistor value.

Potential Effect on System. The AMD system bus signal quality for signals driven to the northbridge may be adversely affected.

Suggested Workaround. All motherboards should have ZN/ZP resistors set to approximately 20 ohms less than the characteristic board impedance.

Resolution Status. Fixed in future revisions.

Note: *When future revisions of the processor are used with motherboards implementing the workaround, the expected output impedance of the driver will continue to yield good signal quality. (For example, with a motherboard setting of 40 ohms for ZN and ZP, an old part that drives with a 60-ohm driver works properly. A revised part with a true 40-ohm driver also works properly.)*

3 Revision Determination

Table 2 shows the AMD Duron processor identification numbers returned by the CPUID instruction for each revision of the processor.

Table 2. CPUID Values for the Revisions of the AMD Duron™ Processor

Revision	CPUID
A0	630
A2	631

4 Technical and Documentation Support

4.1 Documentation Support

The following documents provide additional information regarding the operation of the AMD Duron processor:

- AMD Duron™ Processor Data Sheet, order number 23802
- AMD-751™ System Controller Data Sheet, order number 21910
- AMD-756™ Peripheral Bus Controller Data Sheet, order number 22548

For the latest updates, refer to www.amd.com and download the appropriate files.