AMD Athlon™ MP Processor Model 6

Data Sheet

Multiprocessor-Capable for Workstation and Server Platforms

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Revision History

Date	Rev	Description
June 2001	B	Initial Public Release.
April 2001	A-0	Initial NDA Release.

1 Overview

The AMD Athlon™ MP Processor Model 6 powers the next generation in computing platforms, delivering compelling performance for cutting-edge applications and an unprecedented computing experience.

The AMD Athlon MP processor model 6 with performance-enhancing cache memory is the latest member of the AMD Athlon family of processors. Offering multiprocessor capability, these processors are designed to meet the reliability and computation-intensive requirements of cutting-edge software applications running required by workstations and servers.

Delivered in a socket A PGA package and achieving frequencies of up to 1.2 GHz (1200 MHz), the AMD Athlon MP processor model 6 delivers the integer, floating-point, and 3D multimedia performance for enterprise applications running on x86 system platforms. The AMD Athlon MP processor model 6 offers compelling performance for productivity software, including workstation-class Digital Content Creation (DCC), Electronic Design Automation (EDA), and Computer-Aided Design (CAD), as well as infrastructure and collaborative server applications. It also offers the scalability and 'peace-of-mind' reliability that IT managers and business users require for mission-critical computing.

The AMD Athlon MP processor model 6 features the seventh-generation microarchitecture, including a high-speed execution core that includes multiple x86 instruction decoders; a dual-ported, 128-Kbyte, split level-one (L1) cache; a 256-Kbyte on-chip L2 cache; three independent integer pipelines, three address calculation pipelines; and a superscalar, fully pipelined, out-of-order, three-way floating-point engine. The integrated L2 cache supports the growing processor and system bandwidth requirements of emerging software, graphics, I/O, and memory technologies. The processor also features the advanced MOESI cache coherency protocol to ensure efficient cache integrity in a multiprocessing environment. The floating-point engine is capable of delivering superior performance on the numerically complex applications typical of servers and workstations.

Prototyping, modeling, and high-end visualization applications can take advantage of the exclusive L2 Translation Lookaside Buffer (TLB) and hardware pre-fetch features of the AMD Athlon MP processor model 6. These full-speed cache features allow applications to spend less time searching for frequently used data and more time on computing tasks.

The AMD Athlon MP processor model 6 microarchitecture incorporates enhanced 3DNow!™ Professional technology, a high-performance cache architecture, and a system bus that is designed to run at up to 266-MHz and 2.1-Gigabyte per second. This system bus combines the latest technological advances, such as point-to-point topology, source-synchronous packet-based transfers, and low-voltage signaling. The AMD Athlon MP processor model 6 offers one of the most powerful, scalable system bus architectures available for x86 microprocessors.

The AMD Athlon MP processor model 6 features a point-to-point front-side bus architecture, providing a more efficient, higher bandwidth bus that allows each processor, in a multi-processor configuration, to communicate to the system chipsets through two, full speed, independent buses rather than through a common, shared bus. Combined with the AMD-760™ MP chipset, the processor and the system bus interface with double-data rate (DDR) memory subsystems, providing scalable headroom for bandwidth-hungry applications such as large databases, CAD/CAM modeling, and simulation engines.

The front-side bus of the AMD Athlon MP processor model 6 also provides multiple-bit error detection and single-bit error correction with 8-bit Error Correcting Code (ECC). The front-side bus with 8-bit ECC delivers the high reliability and consistency demanded by mission-critical applications.

The AMD Athlon MP processor model 6 is binary-compatible with existing x86 software and backwards compatible with applications optimized for MMX™ and 3DNow!™ Professional technologies. Using a data format and Single-Instruction Multiple-Data (SIMD) operations based on the MMX instruction model, the AMD Athlon MP processor model 6 can produce as many as four, 32-bit, single-precision floating-point results per clock cycle. The 3DNow! Professional technology implemented in the AMD Athlon MP processor model 6 includes new integer multimedia instructions and software-directed data movement instructions for optimizing such applications as digital content creation and streaming video for the internet, as well as new instructions for Digital Signal Processing (DSP)/communications applications. The new multimedia instructions incorporated in the AMD Athlon MP processor model 6 further extends the capability of 3DNow! to more software than any other processor in the world.

1.1 AMD Athlon™ MP Processor Model 6 Microarchitecture Summary

The following features summarize the AMD Athlon MP processor model 6 microarchitecture:

- A nine-issue, superpipelined, superscalar, x86 processor microarchitecture designed for high clock frequencies
- Multiple x86 instruction decoders
- Three out-of-order, superscalar, fully pipelined floating-point execution units, which execute all x87 (floating-point), MMX and 3DNow! Professional instructions
- Three out-of-order, superscalar, pipelined integer units
- Three out-of-order, superscalar, pipelined address calculation units
- 72-entry instruction control unit
- Advanced dynamic branch prediction
- 3DNow! Professional technology with new instructions to enable improved integer-math calculations for speech or video encoding and improved data movement for internet plug-ins and other streaming applications
- 266-MHz AMD Athlon system bus (scalable beyond 400 MHz) enabling leading-edge system bandwidth for data movement-intensive applications
- Point-to-point front-side bus architecture allowing each processor in a multi-processor configuration to communicate to the system chipsets through two, full speed, independent buses
- High-performance cache architecture featuring an integrated 128-Kbyte L1 cache and a 16-way, 256-Kbyte on-chip L2 cache for a total of 384 Kbytes of on-chip cache

- Exclusive L2 Translation Lookaside Buffer (TLB) and hardware pre-fetch
- Multiple-bit error detection and single-bit error correction with 8-bit Error Correcting Code (ECC)
- Full MP featured Local APIC implementation
- Advanced MOESI cache coherency protocol to ensure efficient cache integrity in a multiprocessing environment

The AMD Athlon MP processor model 6 delivers superior scalability and system performance in a cost-effective, industry-standard form factor. The processor is compatible with motherboards based on AMD's Socket A. For information about the AMD Athlon MP processor module, see the *AMD Athlon™ Processor Module Data Sheet*, order# 21016.

2 Interface Signals

2.1 Overview

The AMD Athlon™ system bus architecture is designed to deliver superior data movement bandwidth for next-generation x86 platforms as well as the high-performance required by enterprise-class application software. The system bus architecture consists of three high-speed channels (a unidirectional processor request channel, a unidirectional probe channel, and a 72–bit bidirectional data channel, including 8–bit Error Code Correction [ECC] protection), source-synchronous clocking, and a packet-based protocol. In addition, the system bus supports several control, clock, and legacy signals. The interface signals use an impedance controlled push-pull low-voltage swing signaling technology contained within the Socket A mechanical connector.

For more information, see “AMD Athlon™ System Bus Signals” on page 6, Chapter 10, “Pin Descriptions” on page 43, and the *AMD Athlon™ and AMD Duron™ System Bus Specification*, order# 21902.

2.2 Signaling Technology

The AMD Athlon system bus uses a low-voltage, swing signaling technology, that has been enhanced to provide larger noise margins, reduced ringing, and variable voltage levels. The signals are push-pull and impedance compensated. The signal inputs use differential receivers, that require a reference voltage (V_{REF}). The reference signal is used by the receivers to determine if a signal is asserted or deasserted by the source. Termination resistors are not needed because the driver is impedance-matched to the motherboard and a high impedance reflection is used at the receiver to bring the signal past the input threshold.

For more information about pins and signals, see Chapter 10, “Pin Descriptions” on page 43.

2.3 Push–Pull (PP) Drivers

The AMD Athlon MP processor model 6 supports Push-Pull (PP) drivers. The system logic configures the processor with the configuration parameter called SysPushPull (1=PP). The impedance of the PP drivers is set to match the impedance of the motherboard by two external resistors connected to the ZN and ZP pins.

See “ZN and ZP Pins” on page 66 for more information.

2.4 AMD Athlon™ System Bus Signals

The AMD Athlon system bus is a clock-forwarded, point-to-point interface with the following three point-to-point channels:

- A 13-bit unidirectional output address/command channel
- A 13-bit unidirectional input address/command channel
- A 72-bit bidirectional data channel

For more information, see Chapter 7, “Electrical Data” on page 23 and the *AMD Athlon™ and AMD Duron™ System Bus Specification*, order# 21902.

3 Logic Symbol Diagram

Figure 1 is the logic symbol diagram of the processor. This diagram shows the logical grouping of the input and output signals.

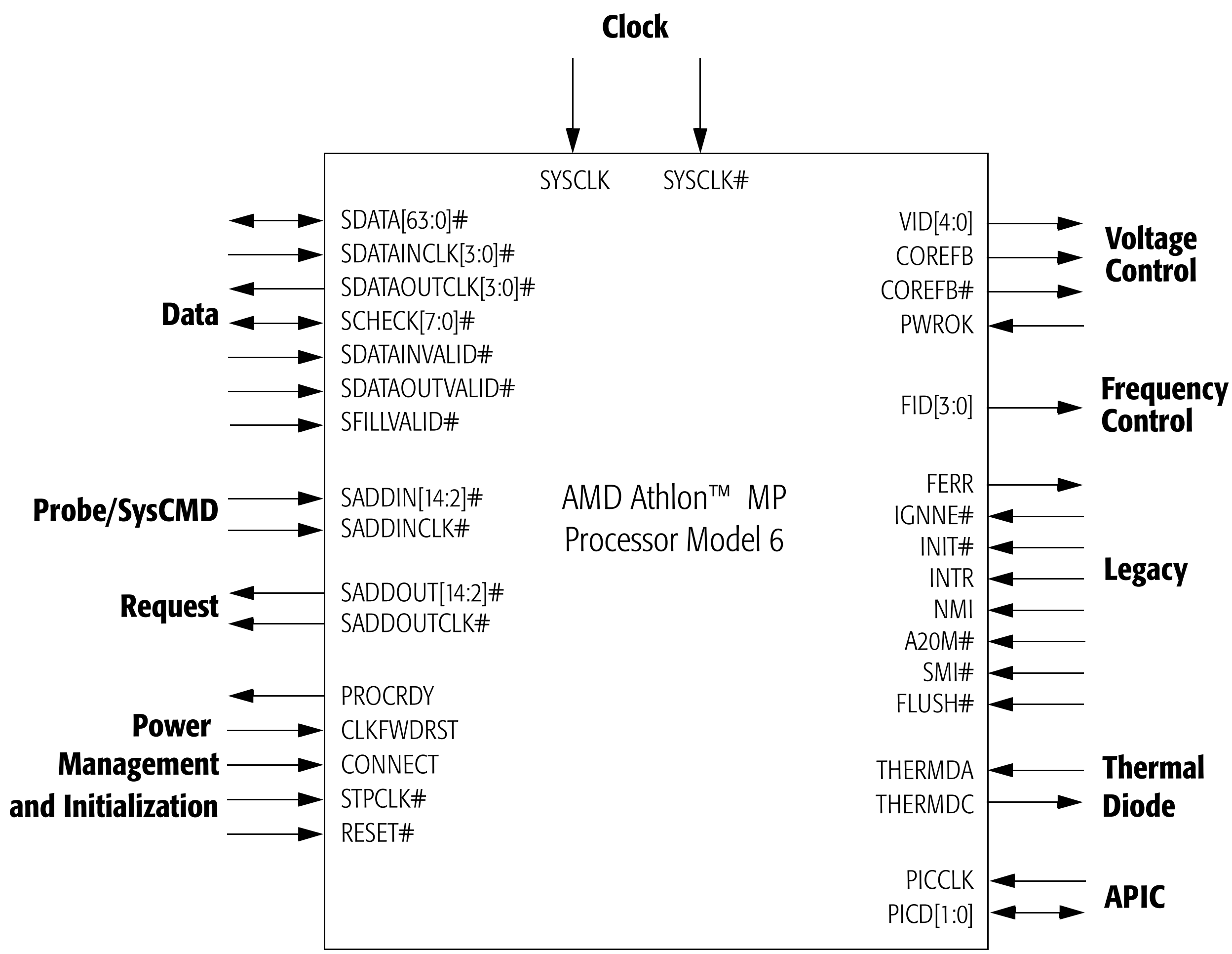


Figure 1. Logic Symbol Diagram

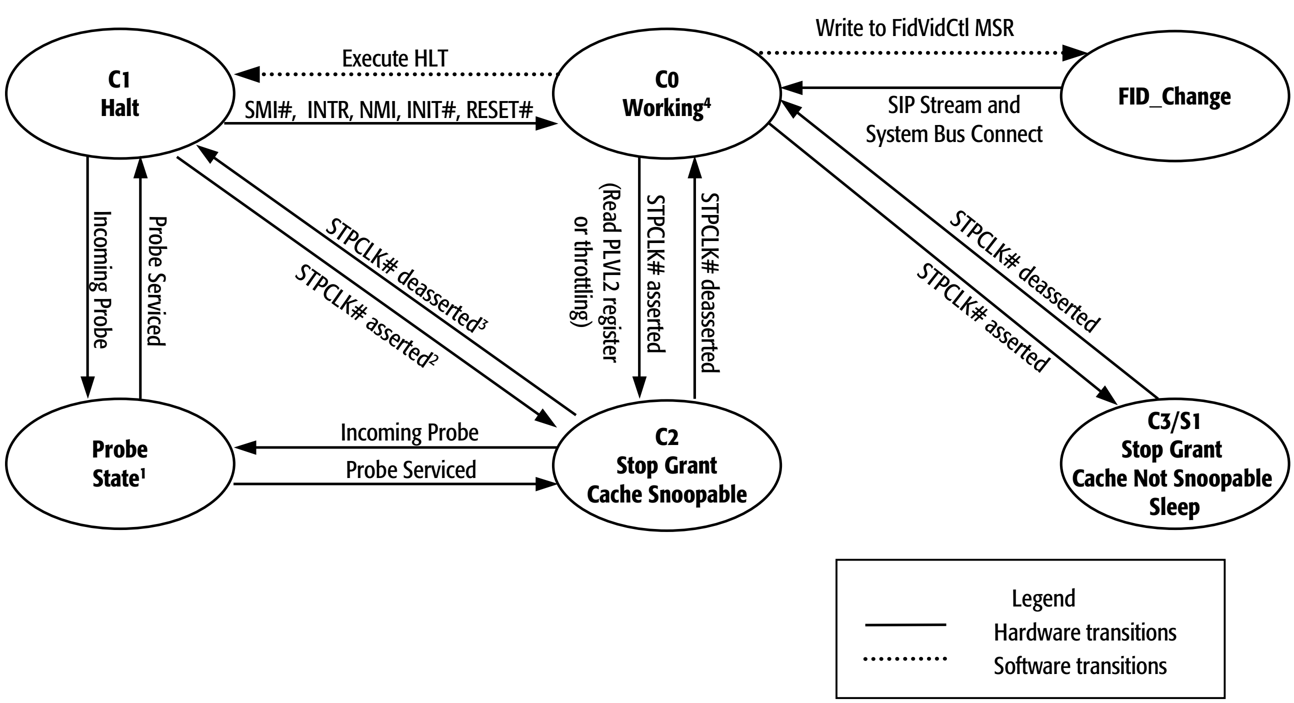
4 Power Management

This chapter describes the power management control system of the AMD Athlon™ MP processor model 6. The power management features of the processor are compliant with the ACPI 1.0b and ACPI 2.0 specifications.

4.1 Power Management States

The AMD Athlon MP processor model 6 supports low-power Halt and Stop Grant states. These states are used by Advanced Configuration and Power Interface (ACPI) enabled operating systems for processor power management.

Figure 2 shows the power management states of the processor. The figure includes the ACPI "Cx" naming convention for these states.



Note: The AMD Athlon™ System Bus is connected during the following states:
1) The Probe state
2) During transitions between the Halt state and the C2 Stop Grant state
3) During transitions between the C2 Stop Grant state and the Halt state
4) C0 Working state

Figure 2. AMD Athlon™ MP Processor Model 6 Power Management States

The following sections provide an overview of the power management states. For more details, refer to the *AMD Athlon™ and AMD Duron™ System Bus Specification,* order# 21902.

Note: *In all power management states that the processor is powered, the system must not stop the system clock (SYSCLK/SYSCLK#) to the processor.*

Working State

The Working state is the state in which the processor is executing instructions.

Halt State

When the processor executes the HLT instruction, the processor enters the Halt state and issues a Halt special cycle to the AMD Athlon system bus. The processor only enters the low power state dictated by the CLK_Ctl MSR if the system controller (Northbridge) disconnects the AMD Athlon system bus in response to the Halt special cycle.

If STPCLK# is asserted, the processor will exit the Halt state and enter the Stop Grant state. The processor will initiate a system bus connect, if it is disconnected, then issue a Stop Grant special cycle. When STPCLK# is deasserted, the processor will exit the Stop Grant state and re-enter the Halt state. The processor will issue a Halt special cycle when re-entering the Halt state.

The Halt state is exited when the processor detects the assertion of INIT#, RESET#, or SMI#, or an interrupt via the INTR or NMI pins, or via a local APIC interrupt message. When the Halt state is exited the processor will initiate an AMD Athlon system bus connect if it is disconnected.

Stop Grant States

The processor enters the Stop Grant state upon recognition of assertion of STPCLK# input. There are two mechanisms for asserting STPCLK#—hardware and software. The Southbridge can force STPCLK# assertion for throttling to protect the processor from exceeding its maximum case temperature. This is accomplished by asserting the THERM# input to the Southbridge. Throttling asserts STPCLK# for a percentage of a predefined throttling period: STPCLK# is repetitively asserted and deasserted until the THERM# pin is deasserted.

Software can force the processor into the Stop Grant state by accessing ACPI-defined registers typically located in the

Southbridge. Software places the processor in C2 by reading the PLVL_2 register in the Southbridge.

In C2, probes are allowed, as shown in Figure 2 on page 9

The Stop Grant state is also entered for the S1, Powered On Suspend, system sleep state based on a write to the SLP_TYP and SLP_EN fields in the ACPI-defined Power Management 1 control register in the Southbridge. During the S1 sleep state, system software ensures no bus master or probe activity occurs. The Southbridge deasserts STPCLK# and brings the processor out of the S1 Stop Grant state when any enabled resume event occurs.

Probe State

The Probe state is entered when the Northbridge connects the AMD Athlon system bus to probe the processor (for example, to snoop the processor caches) when the processor is in the Halt or Stop Grant state. When in the Probe state, the processor responds to a probe cycle in the same manner as when it is in the Working state. When the probe has been serviced, the processor returns to the same state as when it entered the Probe state (Halt or Stop Grant state). When probe activity is completed the processor only returns to a low-power state after the Northbridge disconnects the AMD Athlon system bus again.

4.2 Connect and Disconnect Protocol

Significant power savings of the processor only occur if the processor is disconnected from the system bus by the Northbridge while in the Halt or Stop Grant state. The Northbridge can optionally initiate a bus disconnect upon the receipt of a Halt or Stop Grant special cycle. The option of disconnecting is controlled by an enable bit in the Northbridge. If the Northbridge requires the processor to service a probe after the system bus has been disconnected, it must first initiate a system bus connect.

Connect Protocol

In addition to the legacy STPCLK# signal and the Halt and Stop Grant special cycles, the AMD Athlon system bus connect protocol includes the CONNECT, PROCRDY, and CLKFWDRST signals and a Connect special cycle.

AMD Athlon system bus disconnects are initiated by the Northbridge in response to the receipt of a Halt or Stop Grant special cycle. Reconnect is initiated by the processor in response to an interrupt for Halt, STPCLK# deassertion, or by the Northbridge to service a probe.

The Northbridge contains BIOS programmable registers to enable the system bus disconnect in response to Halt and Stop Grant special cycles. When the Northbridge receives the Halt or Stop Grant special cycle from the processor and, if there are no outstanding probes or data movements, the Northbridge deasserts CONNECT a minimum of eight SYSCLK periods after the last command sent to the processor. The processor detects the deassertion of CONNECT on a rising edge of SYSCLK and deasserts PROCRDY to the Northbridge. In return, the Northbridge asserts CLKFWDRST in anticipation of reestablishing a connection at some later point.

Note: *The Northbridge must disconnect the processor from the AMD Athlon system bus before issuing the Stop Grant special cycle to the PCI bus, or passing the Stop Grant special cycle to the Southbridge for systems that connect to the Southbridge with HyperTransport™ technology.*

This note applies to current chipset implementation—alternate chipset implementations that do not require this are possible.

Note: *In response to Halt special cycles, the Northbridge passes the Halt special cycle to the PCI bus or Southbridge immediately.*

The processor can receive an interrupt after it sends a Halt special cycle, or STPCLK# deassertion after it sends a Stop Grant special cycle to the Northbridge but before the disconnect actually occurs. In this case, the processor sends the Connect special cycle to the Northbridge, rather than continuing with the disconnect sequence. In response to the Connect special cycle, the Northbridge cancels the disconnect request.

The system is required to assert the CONNECT signal before returning the C-bit for the connect special cycle (assuming CONNECT has been deasserted).

For more information, see the *AMD Athlon™ and AMD Duron™ System Bus Specification*, order# 21902 for the definition of the C-bit and the Connect special cycle.

Figure 3 shows STPCLK# assertion resulting in the processor in the Stop Grant state and the system bus disconnected.

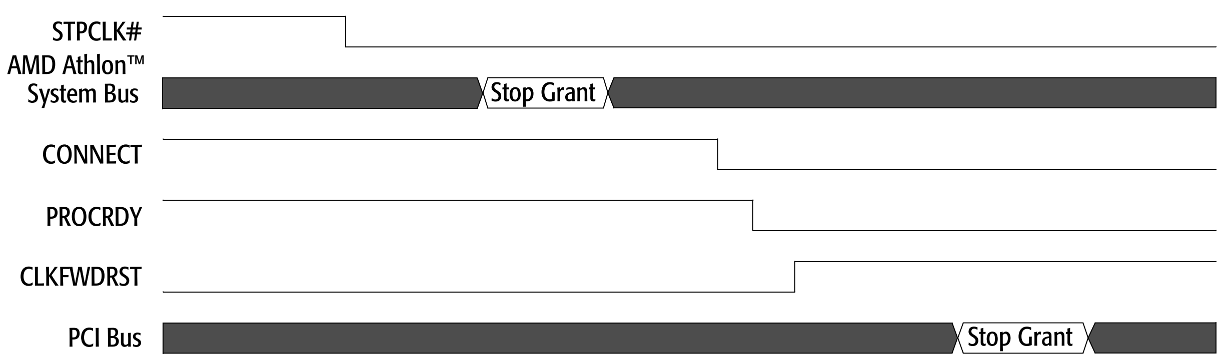


Figure 3. Example of an AMD Athlon™ System Bus Disconnect Sequence in the Stop Grant State

The Northbridge contains BIOS programmable registers to enable the system bus disconnect in response to Halt and Stop Grant special cycles. When the Northbridge receives the Halt or Stop Grant special cycle from the processor and, if there are no outstanding probes or data movements, the Northbridge deasserts CONNECT a minimum of eight SYSCLK periods after the last command sent to the processor. The processor detects the deassertion of CONNECT on a rising edge of SYSCLK and deasserts PROCRDY to the Northbridge. In return, the Northbridge asserts CLKFWDRST in anticipation of reestablishing a connection at some later point.

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This note applies to current chipset implementation—alternate chipset implementations that do not require this are possible.

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For more information, see the *AMD Athlon™ and AMD Duron™ System Bus Specification*, order# 21902 for the definition of the C-bit and the Connect special cycle.

Figure 4 shows the signal sequence of events that takes the processor out of the Stop Grant state, connects the processor to the AMD Athlon system bus, and puts the processor into the Working state.

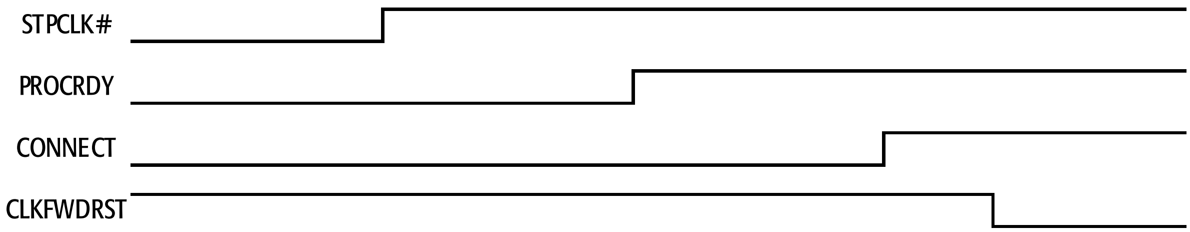
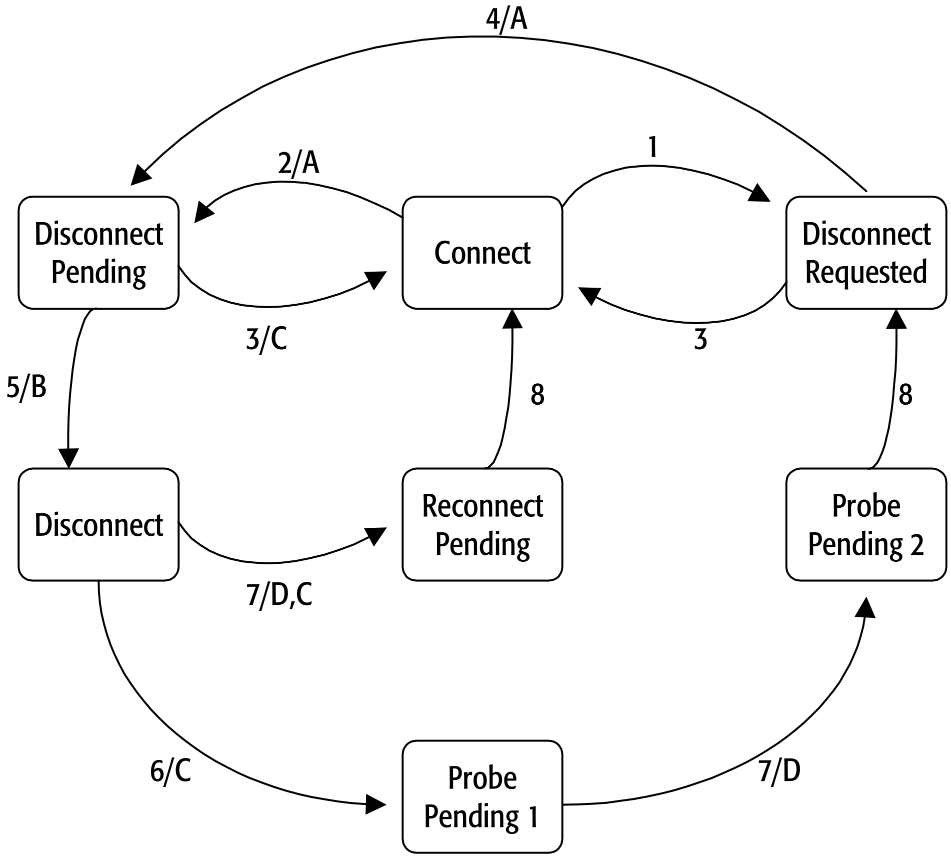


Figure 4. Exiting the Stop Grant State and Bus Connect Sequence

The following sequence of events removes the processor from the Stop Grant state and connects it to the system bus:

1. The Southbridge deasserts STPCLK#, informing the processor of a wake event.
2. When the processor recognizes STPCLK# deassertion, it exits the low-power state and asserts PROCRDY, notifying the Northbridge to connect to the bus.
3. The Northbridge asserts CONNECT.
4. The Northbridge deasserts CLKFWDRST, synchronizing the forwarded clocks between the processor and the Northbridge.
5. The processor issues a Connect special cycle on the system bus and resumes operating system and application code execution.

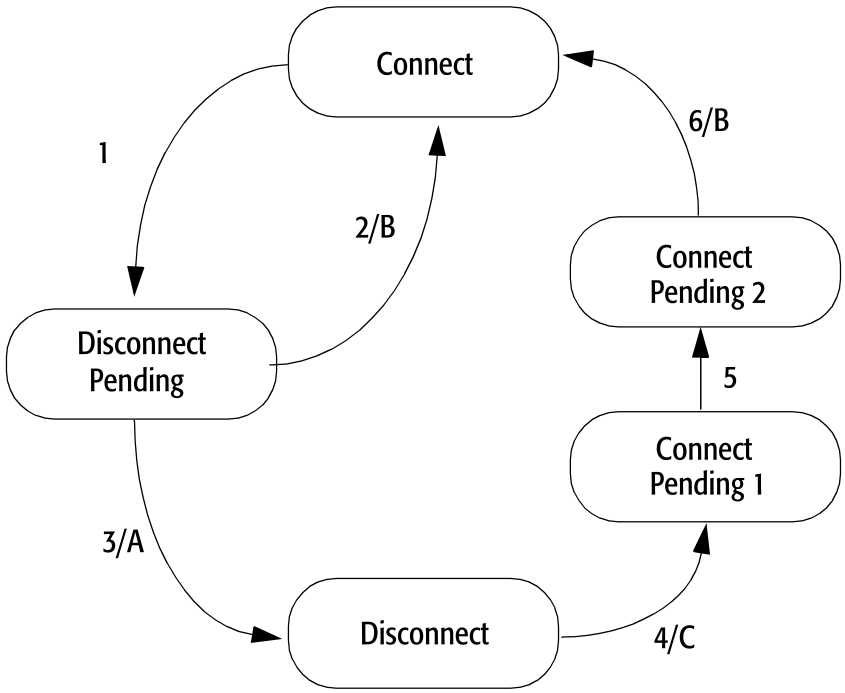
Figure 5 and Figure 6 on page 17 describe the Northbridge and processor connect state diagrams, respectively.



	Condition
1	A disconnect is requested and probes are still pending.
2	A disconnect is requested and no probes are pending.
3	A Connect special cycle from the processor.
4	No probes are pending.
5	PROCRDY is deasserted.
6	A probe needs service.
7	PROCRDY is asserted.
8	Three SYSCLK periods after CLKFWDRST is deasserted. *Although reconnected to the system interface, the Northbridge must not issue any non-NOP SysDC commands for a minimum of four SYSCLK periods after deasserting CLKFWDRST.*

	Action
A	Deassert CONNECT eight SYSCLK periods after last SysDC sent.
B	Assert CLKFWDRST.
C	Assert CONNECT.
D	Deassert CLKFWDRST.

Figure 5. Northbridge Connect State Diagram



	Condition
1	CONNECT is deasserted by the Northbridge (for a previously sent Halt or Stop Grant special cycle).
2	Processor receives a wake-up event and must cancel the disconnect request.
3	Deassert PROCRDY and slow down internal clocks.
4	Processor wake-up event or CONNECT asserted by Northbridge.
5	CLKFWDRST is deasserted by the Northbridge.
6	Forward clocks start three SYSCLK periods after CLKFWDRST is deasserted.

	Action
A	CLKFWDRST is asserted by the Northbridge.
B	Issue a Connect special cycle.*
C	Return internal clocks to full speed and assert PROCRDY

** The Connect special cycle is only issued after a processor wake-up event (interrupt or STPCLK# deassertion) occurs. If the AMD Athlon™ system bus is connected so the Northbridge can probe the processor a Connect special cycle is not issued at that time (it is only issued after a subsequent processor wake-up event).*

Figure 6. Processor Connect State Diagram

4.3 Clock Control

The processor implements a Clock Control (CLK_Ctl) MSR (address C001_001Bh) that determines the internal clock divisor when the AMD Athlon system bus is disconnected.

5 CPUID Support

AMD Athlon™ MP processor model 6 version and feature set recognition can be performed through the use of the CPUID instruction, that provides complete information about the processor—vendor, type, name, etc., and its capabilities. Software can make use of this information to accurately tune the system for maximum performance and benefit to users.

For information on the use of the CPUID instruction see the following documents:

- *AMD Processor Recognition Application Note*, order# 20734
- *AMD Athlon™ Processor Recognition Application Note Addendum*, order# 21922
- *AMD Athlon™ and AMD Duron™ Processors BIOS, Software, and Debug Developers Guide,* order# 21656

6 Thermal Design

The thermal design power represents the maximum sustained power dissipated while executing publicly available software or instruction sequences under normal system operation at nominal VCC_CORE. Thermal solutions must monitor the processor temperature to prevent the processor from exceeding its maximum die temperature.

The maximum die temperature is specified through characterization at 95°C for 1000 MHz and 1200 MHz frequencies.

For information about thermal design for the AMD Athlon™ MP processor model 6, including layout and airflow considerations, see the *AMD Processor Thermal, Mechanical, and Chassis Cooling Design Guide*, order# 23794, and the cooling guidelines on *http://www.amd.com*.

The processor provides a diode that can be used in conjunction with an external temperature sensor to determine the die temperature of the processor. The diode anode (THERMDA) and cathode (THERMDC) are available as pins on the processor.

Refer to "THDA and THDC Pins" on page 64 for more details.

Table 1 shows the thermal design power specifications.

Table 1. Thermal Design Power

Frequency (MHz)	Nominal Voltage	Maximum Thermal Power	Typical Thermal Power	Max Die Temperature
1000	1.75 V	46.1 W	41.3 W	95ºC
1200	1.75 V	54.7 W	49.1 W	95ºC

7 Electrical Data

7.1 Conventions

The conventions used in this chapter are as follows:

- Current specified as being sourced by the processor is *negative*.
- Current specified as being sunk by the processor is *positive*.

7.2 Interface Signal Groupings

The electrical data in this chapter is presented separately for each signal group.

Table 2 defines each group and the signals contained in each group.

Table 2. Interface Signal Groupings

Signal Group	Signals	Notes
Power	VID[4:0], VCCA, VCC_CORE, COREFB, COREFB#	See "Absolute Ratings" on page 28, "Voltage Identification (VID[4:0])" on page 24, "VID[4:0] Pins" on page 65, "VCCA AC and DC Characteristics" on page 25,"VCCA Pin" on page 65, and "COREFB and COREFB# Pins" on page 61.
Frequency	FID[3:0]	See "Frequency Identification (FID[3:0])" on page 25 and "FID[3:0] Pins" on page 61.
System Clocks	SYSCLK, SYSCLK# (Tied to CLKIN/CLKIN# and RSTCLK/RSTCLK#), PLLBYPASSCLK#, PLLBYPASSCLK	See Table 9, "SYSCLK and SYSCLK# DC Characteristics," on page 29, Table 10, "SYSCLK and SYSCLK# AC Characteristics," on page 30, "SYSCLK and SYSCLK#" on page 64, and "PLL Bypass and Test Pins" on page 63.
AMD Athlon™ System Bus	SADDIN[14:2]#, SADDOUT[14:2]#, SADDINCLK#, SADDOUTCLK#, SFILLVAL#, SDATAINVAL#, SDATAOUTVAL#, SDATA[63:0]#, SDATAINCLK[3:0]#, SDATAOUTCLK[3:0]#, SCHECK[7:0]#, CLKFWDRST, PROCRDY, CONNECT	See "AMD Athlon™ System Bus AC and DC Characteristics" on page 31, and "CLKFWDRST Pin" on page 60.

Table 2. Interface Signal Groupings (Continued)

Signal Group	Signals	Notes
Southbridge	RESET#, INTR, NMI, SMI#, INIT#, A20M#, FERR, IGNNE#, STPCLK#, FLUSH#	See "General AC and DC Characteristics" on page 33, "INTR Pin" on page 63, "NMI Pin" on page 63, "SMI# Pin" on page 64, "INIT# Pin" on page 63, "A20M# Pin" on page 60, "FERR Pin" on page 61, "IGNNE# Pin" on page 62, "STPCLK# Pin" on page 64, and "FLUSH# Pin" on page 62.
JTAG	TMS, TCK, TRST#, TDI, TDO	See "General AC and DC Characteristics" on page 33.
Test	PLLBYPASS#, PLLTEST#, PLLMON1, PLLMON2, SCANCLK1, SCANCLK2, SCANSHIFTEN, SCANINTEVAL, ANALOG	See "General AC and DC Characteristics" on page 33, "PLL Bypass and Test Pins" on page 63, "Scan Pins" on page 64, "Analog Pin" on page 60.
Miscellaneous	DBREQ#, DBRDY, PWROK	See "General AC and DC Characteristics" on page 33, "DBRDY and DBREQ# Pins" on page 61, "PWROK Pin" on page 64.
APIC	PICD[1:0]#, PICCLK	See "APIC Pins AC and DC Characteristics" on page 36, and See "APIC Pins, PICCLK, PICD[1:0]#" on page 60.
Thermal	THERMDA, THERMDC	Table 14, "Thermal Diode Characteristics," on page 35, and "THDA and THDC Pins" on page 64.

7.3 Voltage Identification (VID[4:0])

Table 3 shows the VID[4:0] DC Characteristics. For more information on VID[4:0] DC Characteristics, see "VID[4:0] Pins" on page 65.

Table 3. VID[4:0] DC Characteristics

Parameter	Description	Min	Max
I_{OL}	Output Current Low	16 mA	
V_{OH}	Output High Voltage	-	2.625 V*

Note:

* *The VID pins must not be pulled above this voltage by an external pullup resistor.*

7.4 Frequency Identification (FID[3:0])

Table 4 shows the FID[3:0] DC characteristics. For more information, see “FID[3:0] Pins” on page 61.

Table 4. FID[3:0] DC Characteristics

Parameter	Description	Min	Max
I_{OL}	Output Current Low	16 mA	
V_{OH}	Output High Voltage	–	2.625V *

Note:
* *The FID pins must not be pulled above this voltage by an external pullup resistor.*

7.5 VCCA AC and DC Characteristics

Table 5 shows the AC and DC characteristics for VCCA. For more information, see “VCCA Pin” on page 65.

Table 5. VCCA AC and DC Characteristics

Symbol	Parameter	Min	Nominal	Max	Units	Notes
V_{VCCA}	VCCA Pin Voltage	2.25	2.5	2.75	V	1
I_{VCCA}	VCCA Pin Current	0		50	mA/GHz	2

Notes:
1. *Minimum and Maximum voltages are absolute. No transients below minimum nor above maximum voltages are permitted.*
2. *.Measured at 2.5 V.*

7.6 Decoupling

See the *AMD Athlon™ Processor Based Motherboard Design Guide*, order# 24363, or contact your local AMD office for information about the decoupling required on the motherboard for use with the AMD Athlon MP processor model 6.

7.7 VCC_CORE Characteristics

The AMD Athlon MP processor model 6 is designed to provide functional operation if the voltage and temperature parameters are within the limits defined in Table 6, which also shows the AC and DC characteristics for VCC_CORE. See Figure 7 on page 27 for a graphical representation of the VCC_CORE waveform.

Table 6. VCC_CORE Characteristics

Parameter	Description	Min[1]		Nominal[1]	Max[1]		Units
		AC	DC		DC	AC	
VCC_CORE@ 1.75 V	Processor core supply	1.65	1.70	1.75	1.80	1.90	V
VCC_CORE_{SLEEP}[2]	Processor core supply in sleep state	1.65	1.70	1.75	1.80	1.90	V
t_{MAX_AC}[3]	Positive excursion time for AC transients					10	µs
t_{MIN_AC}[3]	Negative excursion time for AC transients					5	µs
T_{DIE}	Temperature of processor die				95		°C

Notes:
1. *All voltage measurements are taken differentially at the COREFB/COREFB# pins.*
2. *Sleep voltage can be used for the S1 sleep state.*
3. *Excursion time is defined as the length of time a signal exceeds the DC threshold level.*

Figure 7 shows the processor core voltage (VCC_CORE) waveform response to perturbation. The t_{MIN_AC} (negative AC transient excursion time) and t_{MAX_AC} (positive AC transient excursion time) represent the maximum allowable time below or above the DC tolerance thresholds.

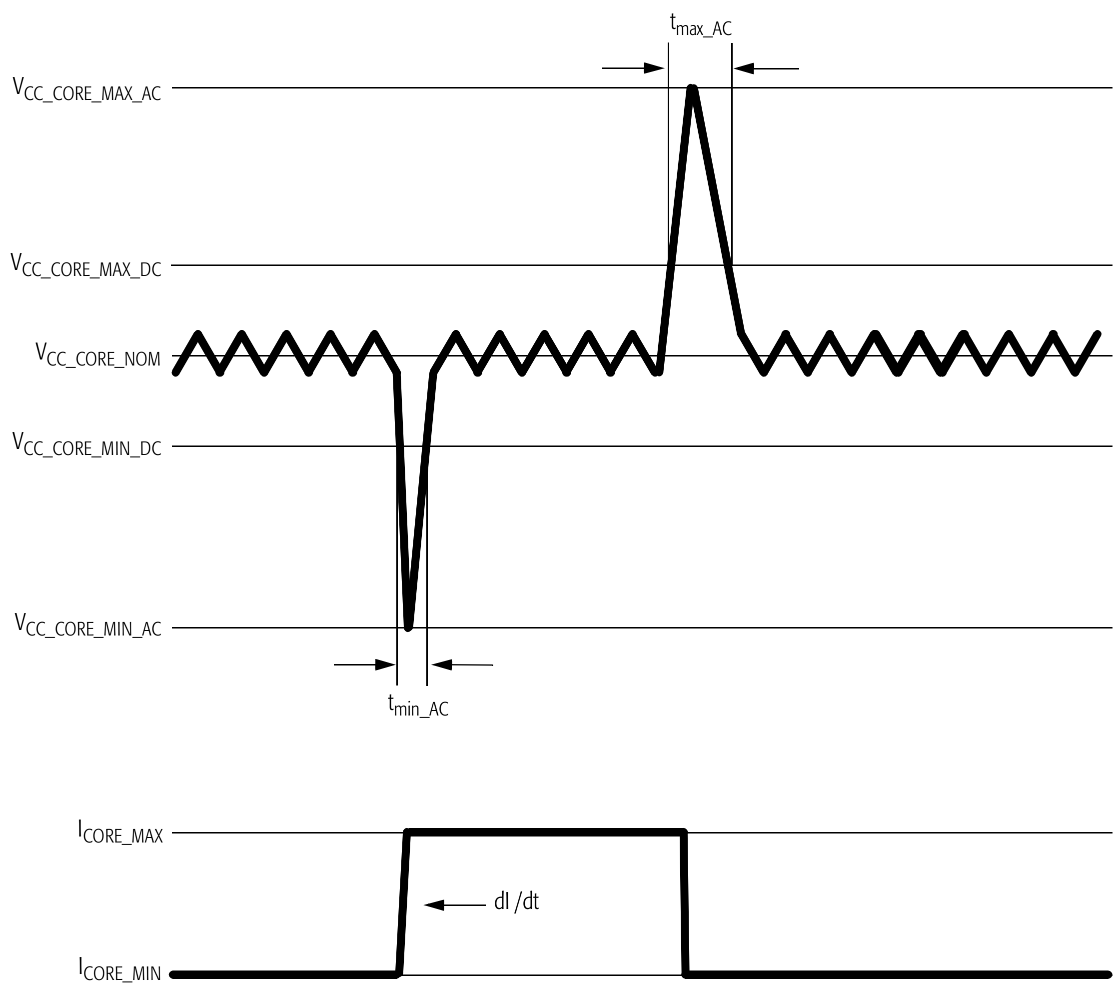


Figure 7. VCC_CORE Voltage Waveform

7.8 Absolute Ratings

The AMD Athlon MP processor model 6 should not be subjected to conditions exceeding the absolute ratings, as such conditions can adversely affect long-term reliability or result in functional damage.

Table 7 lists the maximum absolute ratings of operation for the AMD Athlon MP processor.

Table 7. Absolute Ratings

Parameter	Description	Min	Max
VCC_CORE	AMD Athlon™ MP Processor Model 6 core supply	–0.5 V	VCC_CORE Max + 0.5 V
VCCA	AMD Athlon MP processor model 6 PLL supply	–0.5 V	VCCA Max + 0.5 V
V_{PIN}	Voltage on any signal pin	–0.5 V	VCC_CORE Max + 0.5 V
$T_{STORAGE}$	Storage temperature of processor	–40° C	100° C

7.9 VCC_CORE Voltage and Current

Table 8 shows the power and current for the AMD Athlon MP processor model 6 during normal and reduced power states.

Table 8. VCC_CORE Voltage and Current

Frequency (MHz)	Nominal Voltage	Stop Grant (Maximum)	Maximum I_{CC} (Power Supply Current)[1]	Die Temperature
1000	1.75 V	5 W	26.3 A	95°C
1200	1.75 V	5 W	31.3 A	95°C

Notes:
1. *Measured at Nominal voltage of 1.75 V.*

7.10 SYSCLK and SYSCLK# AC and DC Characteristics

Table 9 shows the DC characteristics of the SYSCLK and SYSCLK# differential clocks. The SYSCLK signal represents CLKIN and RSTCLK tied together while the SYSCLK# signal represents CLKIN# and RSTCLK# tied together.

Table 9. SYSCLK and SYSCLK# DC Characteristics

Symbol	Description	Min	Max	Units
$V_{Threshold-DC}$	Crossing before transition is detected (DC)	400		mV
$V_{Threshold-AC}$	Crossing before transition is detected (AC)	450		mV
I_{LEAK_P}	Leakage current through P-channel pullup to VCC_CORE	−1		mA
I_{LEAK_N}	Leakage current through N-channel pulldown to VSS (Ground)		1	mA
V_{CROSS}	Differential signal crossover		VCC_CORE/2 ±100	mV
C_{PIN}	Capacitance	4	12	pF

Figure 8 shows the DC characteristics of the SYSCLK and SYSCLK# signals.

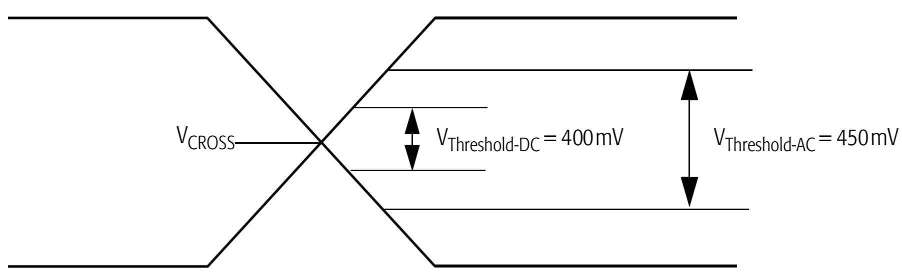


Figure 8. SYSCLK and SYSCLK# Differential Clock Signals

Table 10 shows the SYSCLK/SYSCLK# differential clock AC characteristics of the AMD Athlon MP processor model 6.

Table 10. SYSCLK and SYSCLK# AC Characteristics

Symbol	Parameter Description	Min @		Max @		Units	Notes
	Clock Frequency	100	133	100	133	MHz	3
	Duty Cycle	30%	30%	70%	70%		
t_1	Period	10	7.5			ns	1, 2
t_2	High Time	1.8	1.05			ns	
t_3	Low Time	1.8	1.05			ns	
t_4	Fall Time			2	2	ps	
t_5	Rise Time			2	2	ps	
	Period Stability			± 300	± 300	ps	

Notes:

1. *Circuitry driving the AMD Athlon system bus clock inputs must exhibit a suitably low closed-loop jitter bandwidth to allow the PLL to track the jitter. The –20dB attenuation point, as measured into a 10- or 20-pF load must be less than 500 kHz.*
2. *Circuitry driving the AMD Athlon system bus clock inputs may purposely alter the AMD Athlon system bus clock period (spread spectrum clock generators). In no cases can the AMD Athlon system bus period violate the minimum specification above. AMD Athlon system bus clock inputs can vary from 100% of the specified period to 99% of the specified period at a maximum rate of 100 kHz.*
3. *Minimum Clock Frequency is 50 MHz*

Figure 9 shows a sample waveform of the SYSCLK signal.

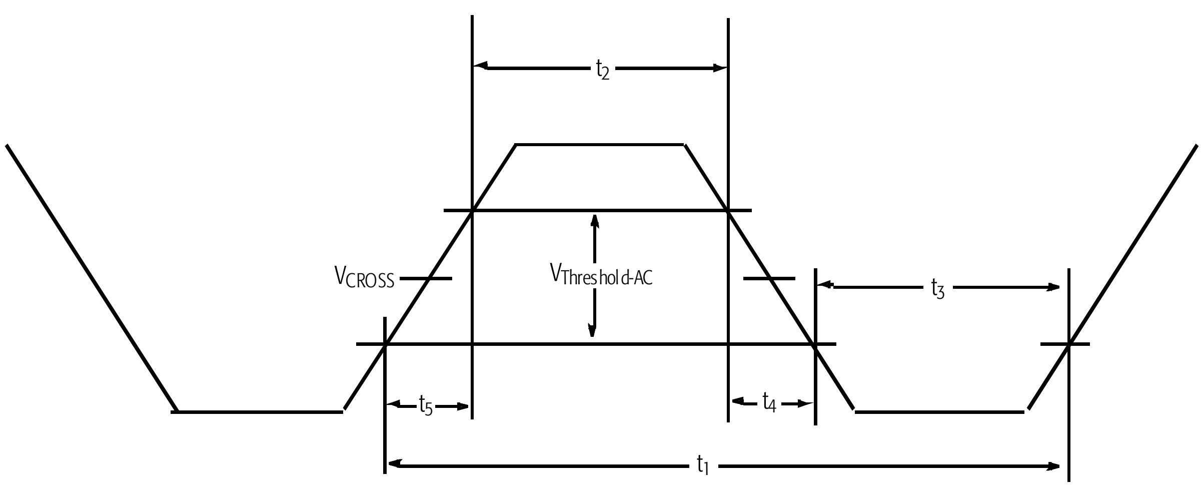


Figure 9. SYSCLK Waveform

7.11 AMD Athlon™ System Bus AC and DC Characteristics

Table 11 shows the DC characteristics of the AMD Athlon system bus used by the AMD Athlon MP processor model 6. See Table 6, "VCC_CORE Characteristics," on page 26 for information on T_{DIE} and VCC_CORE. For information about SYSCLK and SYSCLK#, see "SYSCLK and SYSCLK#" on page 64 and Table 17, "Pin Name Abbreviations," on page 46.

Table 11. AMD Athlon™ System Bus DC Characteristics

Symbol	Parameter	Condition	Min	Max	Units	Notes
V_{REF}	DC Input Reference Voltage		(0.5*VCC_CORE) –50	(0.5*VCC_CORE) +50	mV	1
$I_{VREF\_LEAK\_P}$	V_{REF} Tristate Leakage Pullup	$V_{IN} = V_{REF}$ Nominal	–100		µA	
$I_{VREF\_LEAK\_N}$	V_{REF} Tristate Leakage Pulldown	$V_{IN} = V_{REF}$ Nominal		+100	µA	
V_{IH}	Input High Voltage		V_{REF} + 200	VCC_CORE + 500	mV	
V_{IL}	Input Low Voltage		–500	V_{REF} – 200	mV	
V_{OH}	Output High Voltage	I_{OUT} = –200 µA	0.85 VCC_CORE	VCC_CORE+500	mV	2
V_{OL}	Output Low Voltage	I_{OUT} = 1 mA	–500	400	mV	2
I_{LEAK_P}	Tristate Leakage Pullup	V_{IN} = VSS (Ground)	–1		mA	
I_{LEAK_N}	Tristate Leakage Pulldown	V_{IN} = VCC_CORE Nominal		+1	mA	
C_{IN}	Input Pin Capacitance		4	12	pF	3

Notes:

1. *V_{REF} is nominally set to 50% of VCC_CORE with actual values that are specific to motherboard design implementation. V_{REF} must be created with a sufficiently accurate DC source and a sufficiently quiet AC response to adhere to the ± 50 mV specification listed above.*
2. *Specified at the T_{DIE} and VCC_CORE specifications in this document.*
3. *The following processor inputs have twice the listed capacitance because they connect to two input pads–SYSCLK, and SYSCLK#. SYSCLK connects to CLKIN/RSTCLK. SYSCLK# connects to CLKIN#/RSTCLK#. .*

The AC characteristics of the AMD Athlon system bus are shown in Table 12 on page 32. The parameters are grouped based on the source or destination of the signals involved.

Table 12. AMD Athlon™ System Bus AC Characteristics

Group	Symbol	Parameter	Min	Max	Units	Notes
All Signals	T_{RISE}	Output Rise Slew Rate	1	3	V/ns	1
	T_{FALL}	Output Fall Slew Rate	1	3	V/ns	1
Forward Clocks	$T_{SKEW-SAMEEDGE}$	Output skew with respect to the same clock edge	–	385	ps	2
	$T_{SKEW-DIFFEDGE}$	Output skew with respect to a different clock edge	–	770	ps	2
	T_{SU}	Input Data Setup Time	300		ps	3
	T_{HD}	Input Data Hold Time	300		ps	3
	C_{IN}	Capacitance on input Clocks	4	12	pF	
	C_{OUT}	Capacitance on output Clocks	4	12	pF	
Sync	T_{VAL}	RSTCLK to Output Valid	250	2000	ps	4,5
	T_{SU}	Setup to RSTCLK	500		ps	4,6
	T_{HD}	Hold from RSTCLK	1000		ps	4,6

Notes:

1. *Rise and fall time ranges are guidelines over which the I/O has been characterized.*
2. *$T_{SKEW-SAMEEDGE}$ is the maximum skew within a clock forwarded group between any two signals or between any signal and its forward clock, as measured at the package, with respect to the same clock edge.*
   $T_{SKEW-DIFFEDGE}$ is the maximum skew within a clock forwarded group between any two signals or between any signal and its forward clock, as measured at the package, with respect to different clock edges.
3. *Input SU and HD times are with respect to the appropriate Clock Forward Group input clock.*
4. *The synchronous signals include PROCRDY, CONNECT, CLKFWDRST.*
5. *T_{VAL} is RSTCLK rising edge to output valid for PROCRDY. Test Load is 25 pF.*
6. *T_{SU} is setup of CONNECT/CLKFWDRST to rising edge of RSTCLK. T_{HD} is hold of CONNECT/CLKFWDRST from rising edge of RSTCLK.*

7.12 General AC and DC Characteristics

Table 13 shows the AMD Athlon MP processor model 6 AC and DC characteristics of the Southbridge, JTAG, test, and miscellaneous pins.

Table 13. General AC and DC Characteristics

Symbol	Parameter Description	Condition	Min	Max	Units	Notes
V_{IH}	Input High Voltage		(VCC_CORE/2) + 200 mV	VCC_CORE + 300 mV	V	1,2
V_{IL}	Input Low Voltage		–300	350	mV	1,2
V_{OH}	Output High Voltage		VCC_CORE – 400	VCC_CORE + 300	mV	
V_{OL}	Output Low Voltage		–300	400	mV	
I_{LEAK_P}	Tristate Leakage Pullup	V_{IN} = VSS (Ground)	–1		mA	
I_{LEAK_N}	Tristate Leakage Pulldown	V_{IN} = VCC_CORE Nominal		600	µA	
I_{OH}	Output High Current			–16	mA	3
I_{OL}	Output Low Current		16		mA	3
T_{SU}	Sync Input Setup Time		2.0		ns	4, 5
T_{HD}	Sync Input Hold Time		0.0		ps	4, 5
T_{DELAY}	Output Delay with respect to RSTCLK		0.0	6.1	ns	5
T_{BIT}	Input Time to Acquire		20.0		ns	7,8
T_{RPT}	Input Time to Reacquire		40.0		ns	9-13

Notes:

1. *Characterized across DC supply voltage range.*
2. *Values specified at nominal VCC_CORE. Scale parameters between VCC_CORE minimum and VCC_CORE maximum.*
3. I_{OL} *and* I_{OH} *are measured at* V_{OL} *max and* V_{OH} *min, respectively.*
4. *Synchronous inputs/outputs are specified with respect to RSTCLK and RSTCK# at the pins.*
5. *These are aggregate numbers.*
6. *Edge rates indicate the range over which inputs were characterized.*
7. *In asynchronous operation, the signal must persist for this time to guarantee capture.*
8. *This value assumes RSTCLK frequency is 10 ns ==> TBIT = 2*fRST.*
9. *The approximate value for standard case in normal mode operation.*
10. *This value is dependent on RSTCLK frequency, divisors, Low Power mode, and core frequency.*
11. *Reassertions of the signal within this time are not guaranteed to be seen by the core.*
12. *This value assumes that the skew between RSTCLK and K7CLKOUT is much less than one phase.*
13. *This value assumes RSTCLK and K7CLKOUT are running at the same frequency, though the processor is capable of other configurations.*

Table 13. General AC and DC Characteristics (Continued)

Symbol	Parameter Description	Condition	Min	Max	Units	Notes
T_{RISE}	Signal Rise Time		1.0	3.0	V/ns	6
T_{FALL}	Signal Fall Time		1.0	3.0	V/ns	6
C_{PIN}	Pin Capacitance		4	12	pF	

Notes:

1. *Characterized across DC supply voltage range.*
2. *Values specified at nominal VCC_CORE. Scale parameters between VCC_CORE minimum and VCC_CORE maximum.*
3. *I_{OL} and I_{OH} are measured at V_{OL} max and V_{OH} min, respectively.*
4. *Synchronous inputs/outputs are specified with respect to RSTCLK and RSTCK# at the pins.*
5. *These are aggregate numbers.*
6. *Edge rates indicate the range over which inputs were characterized.*
7. *In asynchronous operation, the signal must persist for this time to guarantee capture.*
8. *This value assumes RSTCLK frequency is 10 ns ==> TBIT = 2*fRST.*
9. *The approximate value for standard case in normal mode operation.*
10. *This value is dependent on RSTCLK frequency, divisors, Low Power mode, and core frequency.*
11. *Reassertions of the signal within this time are not guaranteed to be seen by the core.*
12. *This value assumes that the skew between RSTCLK and K7CLKOUT is much less than one phase.*
13. *This value assumes RSTCLK and K7CLKOUT are running at the same frequency, though the processor is capable of other configurations.*

7.13 Thermal Diode Characteristics

Table 14 shows the AMD Athlon MP processor model 6 characteristics of the on–board thermal diode

Table 14. Thermal Diode Characteristics

Symbol	Parameter Description	Min	Nom	Max	Units	Notes
I_{fw}	Forward bias current	5		300	µA	1
n	Diode ideality factor	1.002	1.008	1.016		2, 3, 4, 5

Notes:

1. *The sourcing current should always be used in forward bias only.*
2. *Characterized at 95°C with a forward bias current pair of 10 µA and 100 µA.*
3. *Not 100% tested. Specified by design and limited characterization.*
4. *The diode ideality factor, n, is a correction factor to the ideal diode equation.*

   For the following equations, use the following variables and constants:

   n diode ideality factor
   k Boltzmann constant
   q electron charge constant
   T diode temperature (Kelvin)
   V_{BE} Voltage from base to emitter
   I_C Collector current
   I_S Saturation current
   N Ratio of collector currents

   The equation for V_{BE} is:

   $$V_{BE} = \frac{nkT}{q} \cdot \ln\left(\frac{I_C}{I_S}\right)$$

   By sourcing two currents and using the above equation, a difference in base emitter voltage can be found which leads to the following equation for temperature:

   $$T = \frac{\Delta V_{BE}}{n \cdot \ln(N) \cdot \frac{k}{q}}$$

5. *If a different sourcing current pair is used other than 10 µA and 100 µA, the following equation should be used to correct the temperature. Subtract this offset from the temperature measured by the temperature sensor.*

   For the following equations, use the following variables and constants:

   I_{high} High sourcing current
   I_{low} Low sourcing current

   T_{offset} (in °C) can be found using the following equation:

   $$T_{offset} = (6.0 \cdot 10^4) \cdot \frac{(I_{high} - I_{low})}{\ln\left(\frac{I_{high}}{I_{low}}\right)} - 2.34$$

7.14 APIC Pins AC and DC Characteristics

Table 15 shows the AMD Athlon MP processor model 6 AC and DC characteristics of the APIC pins.

Table 15. APIC Pins AC and DC Characteristics

Symbol	Parameter Description	Condition	Min	Max	Units	Notes
V_{IH}	Input High Voltage		1.7	2.625	V	1, 3
V_{IL}	Input Low Voltage		–300	700	mV	1, 2
V_{OH}	Output High Voltage			2.625	V	3
V_{OL}	Output Low Voltage		–300	400	mV	
I_{LEAK_P}	Tristate Leakage Pullup	V_{IN} = VSS (Ground)	–1		mA	
I_{LEAK_N}	Tristate Leakage Pulldown	V_{IN} = 2.5 V		1	mA	
I_{OL}	Output Low Current	V_{OL} Max	12		mA	
T_{RISE}	Signal Rise Time		1.0	3.0	V/ns	4
T_{FALL}	Signal Fall Time		1.0	3.0	V/ns	4
C_{PIN}	Pin Capacitance		4	12	pF	

Notes:

1. *Characterized across DC supply voltage range*
2. *Values specified at nominal VDD (1.5 V). Scale parameters with VDD*
3. *2.625 V = 2.5 V + 5% maximum*
4. *Edge rates indicate the range over which inputs were characterized*

8 Signal and Power-Up Requirements

This chapter describes the AMD Athlon™ MP processor model 6 power-up requirements during system power-up and warm resets.

8.1 Power-Up Requirements

Signal Sequence and Timing Description

Figure 10 shows the relationship between key signals in the system during a power-up sequence. This figure details the requirements of the processor.

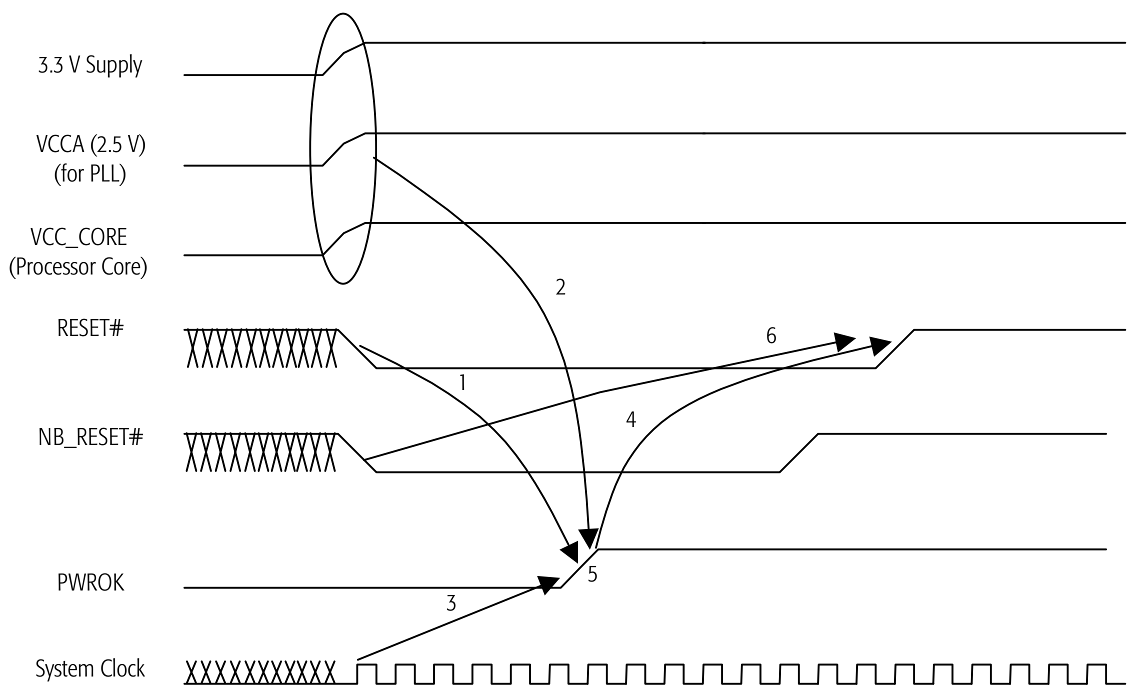


Figure 10. Signal Relationship Requirements During Power-Up Sequence

Notes: *1. Figure 10 represents several signals generically by using names not necessarily consistent with any pin lists or schematics.*

2. Requirements 1-6 in Figure 10 are described in "Power-Up Requirements" on page 37

Power-Up Timing Requirements. The signal timing requirements are as follows:

1. RESET# must be asserted before PWROK is asserted

   The AMD Athlon MP processor model 6 does not set the correct clock multiplier if PWROK is asserted prior to a RESET# assertion. It is recommended that RESET# be asserted at least **10 nanoseconds** prior to the assertion of PWROK.

   In practice, Southbridges assert RESET# milliseconds before PWROK is deasserted.

2. All motherboard voltage planes must be within specification before PWROK is asserted.

   PWROK is an output of the voltage regulation circuit on the motherboard. PWROK indicates that VCC_CORE and all other voltage planes in the system are within specification.

   The motherboard is required to delay PWROK assertion for a minimum of three milliseconds from the 3.3 V supply being within specification. This ensures that the system clock (SYSCLK/SYSCLK#) is operating within specification when PWROK is asserted.

   The processor core voltage, VCC_CORE, must be within specification as dictated by the VID[4:0] pins driven by the processor before PWROK is asserted. Before PWROK assertion, the AMD Athlon MP processor is clocked by a ring oscillator.

   The AMD Athlon MP processor PLL is powered by VCCA. The processor PLL does not lock if VCCA is not high enough for the processor logic to switch for some period before PWROK is asserted. VCCA must be within specification at least five microseconds before PWROK is asserted.

   In practice VCCA, VCC_CORE, and all other voltage planes must be within specification be for several milliseconds before PWROK is asserted.

After PWROK is asserted, the processor PLL locks to its operational frequency.

3. The system clock (SYSCLK/SYSCLK#) must be running within specification before PWROK is asserted.

   When PWROK is asserted, the processor switches from driving the internal processor clock grid from the ring oscillator to driving from the PLL. The reference system clock should be valid at this time. The system clocks are guaranteed to be running after 3.3 V has been within specification for three milliseconds.

4. PWROK assertion to deassertion of RESET#.

   The duration of RESET# assertion during cold boots is intended to satisfy the time it takes for the PLL to lock with a less than 1–ns phase error. The processor PLL begins to run after PWROK is asserted and the internal clock grid is switched from the ring oscillator to the PLL. The PLL lock time can take from hundreds of nanoseconds to tens of microseconds. It is recommended that the minimum time between PWROK assertion to the deassertion of RESET# be at least **1.0 milliseconds**. The AMD Southbridge enforces a delay of 1.5 to 2.0 milliseconds between PWRGD (Southbridge version of PWROK) assertion and NB_RESET# deassertion.

5. PWROK must be monotonic.

   The processor should not switch between the ring oscillator and the PLL after the initial assertion of PWROK.

6. NB_RESET# must be asserted (causing CONNECT to also assert) before RESET# is deasserted. In practice all Southbridges enforce this requirement.

   If NB_RESET# does not assert until after RESET# has deasserted, the processor misinterprets the CONNECT assertion (due to NB_RESET# being asserted) as the beginning of the SIP transfer (See “Serial Initialization Packet (SIP) Protocol” on page 40). There must be sufficient overlap in the resets to ensure that CONNECT is sampled asserted by the processor before RESET# is deasserted.

Clock Multiplier Selection (FID[3:0])

When RESET# is deasserted, the Northbridge samples the FID[3:0] frequency ID from the processor in a chipset-specific manner. For more information, see “FID[3:0] Pins” on page 61.

The Northbridge uses this FID information and other information sampled at the deassertion of RESET# to determine the correct Serial Initialization Packet (SIP) to send to the processor for configuration of the AMD Athlon system bus for the clock multiplier processor frequency indicated by the FID[3:0] code. The SIP is sent to the processor using the SIP protocol. This protocol uses the PROCRDY, CONNECT, and CLKFWDRST signals, which are synchronous to SYSCLK.

Serial Initialization Packet (SIP) Protocol. Refer to the *AMD Athlon™ and AMD Duron™ System Bus Specification*, order# 21902 for details of the SIP protocol.

8.2 Processor Warm Reset Requirements

Northbridge Reset Pins

RESET cannot be asserted to the processor without also being asserted to the Northbridge. RESET# to the Northbridge is the same in as PCI RESET#. The minimum assertion for PCI RESET# is one millisecond. The AMD Southbridge enforces a minimum assertion of RESET# to the processor, Northbridge, or PCI of 1.5 to 2.0 milliseconds.

9 Mechanical Data

9.1 Introduction

The AMD Athlon™ MP processor model 6 connects to the motherboard through a PGA socket named Socket A. For more information, see the *AMD Athlon™ Processor Based Motherboard Design Guide*, order# 24363.

9.2 Die Loading

The processor die is exposed at the top of the package. This feature facilitates heat transfer from the die to a heat sink. It is critical that the mechanical loading of the heat sink does not exceed the limits shown in Table 16. Any heat sink design should avoid loads on corners and edges of die. The CPGA package has compliant pads that serve to bring surfaces in planar contact.

Table 16. CPGA Mechanical Loading

Location	Dynamic (MAX)	Static (MAX)	Units	Note
Die Surface	100	30	lbf	2
Die Edge	10	10	lbf	3

Notes:

1. *Tool–assisted zero insertion force sockets should be designed such that no load is placed on the ceramic substrate of the package.*
2. *Load specified for coplanar contact to die surface.*
3. *Load defined for a surface at no more than a two degree angle of inclination to die surface.*

9.3 Package Description

Figure 11 on page 42 shows the mechanical drawing of the CPGA processor package. The relevant dimensions and locations of the processor die are shown for reference purposes.

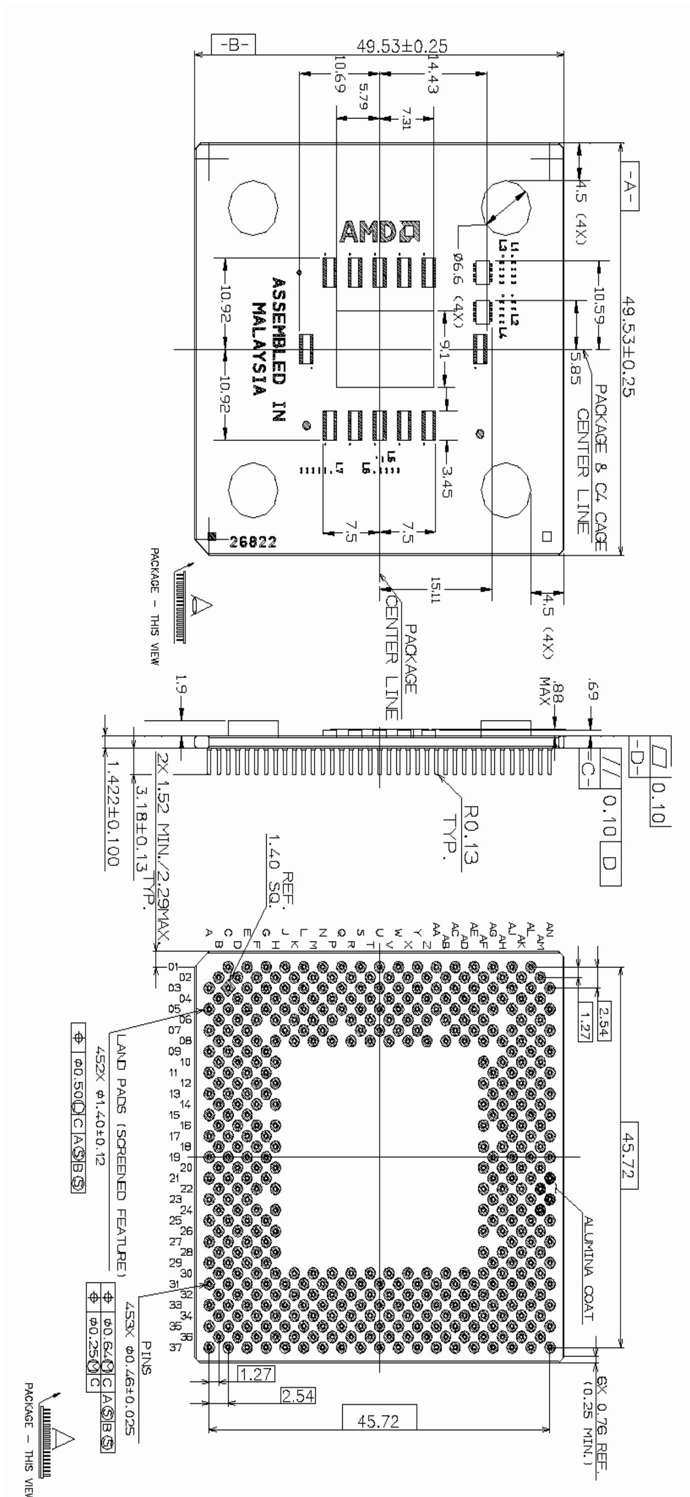


Figure 11. AMD Athlon™ MP Processor Model 6 PGA Package Top View

10 Pin Descriptions

10.1 Pin Diagram and Pin Name Abbreviations

Figure 12 on page 44 shows the staggered Ceramic Pin Grid Array (CPGA) for the AMD Athlon™ MP Processor Model 6. Because some of the pin names are too long to fit in the grid, they are abbreviated. Figure 13 on page 45 shows the bottomside view of the array. Table 17 on page 46 lists all the pins in alphabetical order by pin name, along with the abbreviation where necessary.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
A			SAO#12		SAO#5		SAO#3		SD#55		SD#61		SD#53		SD#63		SD#62		SCK#7
B		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS	
C	SAO#7		SAO#9		SAO#8		SAO#2		SD#54		SDOC#3		SCK#6		SD#51		SD#60		SD#59
D		VCC		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS	
E	SAO#11		SAOC#		SAO#4		SAO#6		SD#52		SD#50		SD#49		SDIC#3		SD#48		SD#58
F		VSS		VSS		VSS		NC		VSS		VCC		VSS		VCC		VSS	
G	SAO#10		SAO#14		SAO#13		KEY		KEY		NC		NC		KEY		KEY		NC
H		VCC		VCC		NC		NC		NC		VCC		VSS		VCC		VSS	
J	SAO#0		SAO#1		NC		VID[4]												
K		VSS		VSS		VSS		NC											
L	VID[0]		VID[1]		VID[2]		VID[3]												
M		VCC		VCC		VCC		VCC											
N	PICCLK		PICD#0		PICD#1		KEY												
P		VSS		VSS		VSS		VSS											
Q	TCK		TMS		SCNSN		KEY												
R		VCC		VCC		VCC		VCC											
S	SCNCK1		SCNINV		SCNCK2		THDA												
T		VSS		VSS		VSS		VSS											
U	TDI		TRST#		TDO		THDC												
V		VCC		VCC		VCC		VCC											
W	FID[0]		FID[1]		VREF_S		NC												
X		VSS		VSS		VSS		VSS											
Y	FID[2]		FID[3]		NC		KEY												
Z		VCC		VCC		VCC		VCC											
AA	DBRDY		DBREQ#		NC		KEY												
AB		VSS		VSS		VSS		VSS											
AC	STPC#		PLTST#		ZN		NC												
AD		VCC		VCC		VCC		NC											
AE	A20M#		PWROK		ZP		NC												
AF		VSS		VSS		NC		NC		NC		VSS		VCC		VSS		VCC	
AG	FERR		RESET#		NC		KEY		KEY		COREFB		COREFB#		KEY		KEY		NC
AH		VCC		VCC		AMD		NC		VCC		VSS		VCC		VSS		VCC	
AJ	IGNNE#		INIT#		VCC		NC		NC		NC		ANLOG		NC		NC		NC
AK		VSS		VSS		CPR#		NC		VCC		VSS		VCC		VSS		VCC	
AL	INTR		FLUSH#		VCC		NC		NC		NC		PLMN2		PLBYC#		CLKIN#		RCLK#
AM		VCC		VSS		VSS		NC		VCC		VSS		VCC		VSS		VCC	
AN			NMI		SMI#		NC		NC		NC		PLMN1		PLBYC		CLKIN		RCLK

	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	
A		SD#57		SD#39		SD#35		SD#34		SD#44		SCK#5		SDOC#2		SD#40		SD#30	A
B	VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		B
C		SD#56		SD#37		SD#47		SD#38		SD#45		SD#43		SD#42		SD#41		SDOC#1	C
D	VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VSS		D
E		SD#36		SD#46		SCK#4		SDIC#2		SD#33		SD#32		SCK#3		SD#31		SD#22	E
F	VCC		VSS		VCC		VSS		VCC		NC		VCC		VCC		VCC		F
G		NC		KEY		KEY		NC		NC		NC		SD#20		SD#23		SD#21	G
H	VCC		VSS		VCC		VSS		NC		NC		NC		VSS		VSS		H
J												NC		SD#19		SDIC#1		SD#29	J
K											NC		VCC		VCC		VCC		K
L												NC		SD#26		SCK#2		SD#28	L
M											VSS		VSS		VSS		VSS		M
N												NC		SD#25		SD#27		SD#18	N
P											VCC		VCC		VCC		VCC		P
Q												NC		SD#24		SD#17		SD#16	Q
R											VSS		VSS		VSS		VSS		R
S												NC		SD#7		SD#15		SD#6	S
T											VCC		VCC		VCC		VCC		T
U												NC		SD#5		SD#4		SCK#0	U
V											VSS		VSS		VSS		VSS		V
W												NC		SDIC#0		SD#2		SD#1	W
X											VCC		VCC		VCC		VCC		X
Y												NC		SCK#1		SD#3		SD#12	Y
Z											VSS		VSS		VSS		VSS		Z
AA												NC		SD#8		SD#0		SD#13	AA
AB											VCC		VCC		VCC		VCC		AB
AC												NC		SD#10		SD#14		SD#11	AC
AD											NC		VSS		VSS		VSS		AD
AE												NC		SAI#5		SDOC#0		SD#9	AE
AF	VSS		VCC		VSS		VCC		NC		NC		NC		VCC		VCC		AF
AG		NC		NC		NC		KEY		KEY		NC		SAI#2		SAI#11		SAI#7	AG
AH	VSS		VCC		VSS		VCC		VSS		NC		VSS		VSS		VSS		AH
AJ		CLKFR		VCCA		PLBYP#		NC		SAI#0		SFILLV#		SAIC#		SAI#6		SAI#3	AJ
AK	VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VCC		AK
AL		K7CO		CNNCT		NC		NC		SAI#1		SDOV#		SAI#8		SAI#4		SAI#10	AL
AM	VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		AM
AN		K7CO#		PRCRDY		NC		NC		SAI#12		SAI#14		SDINV#		SAI#13		SAI#9	AN

AMD Athlon™ MP Processor
Model 6
Topside View

Figure 12. AMD Athlon™ MP Processor Model 6 Pin Diagram—Topside View

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T	U	V	W	X	Y	Z	AA	AB	AC	AD	AE	AF	AG	AH	AJ	AK	AL	AM	AN	
1			SAO#7		SAO#11		SAO#10		SAO#0		VID[0]		PICCLK		TCK		SCNCK1		TDI		FID[0]		FID[2]		DBRDY		STPC#		A20M#		FERR		IGNNE#		INTR			1
2		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		2
3	SAO#12		SAO#9		SAOC#		SAO#14		SAO#1		VID[1]		PICD#0		TMS		SCNINV		TRST#		FID[1]		FID[3]		DBREQ#		PLTST#		PWROK		RESET#		INIT#		FLUSH#		NMI	3
4		VCC		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VSS		4
5	SAO#5		SAO#8		SAO#4		SAO#13		NC		VID[2]		PICD#1		SCNSN		SCNCK2		TDO		VREF_S		NC		NC		ZN		ZP		NC		VCC		VCC		SMI#	5
6		VSS		VSS		VSS		NC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		NC		AMD		CPR#		VSS		6
7	SAO#3		SAO#2		SAO#6		KEY		VID[4]		VID[3]		KEY		KEY		THDA		THDC		NC		KEY		KEY		NC		NC		KEY		NC		NC		NC	7
8		VCC		VCC		NC		NC		NC		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		NC		NC		NC		NC		NC		8
9	SD#55		SD#54		SD#52		KEY																								KEY		NC		NC		NC	9
10		VSS		VSS		VSS		NC																						NC		VCC		VCC		VCC		10
11	SD#61		SDOC#3		SD#50		NC																								COREFB		NC		NC		NC	11
12		VCC		VCC		VCC		VCC																						VSS		VSS		VSS		VSS		12
13	SD#53		SCK#6		SD#49		NC																								COREFB#		ANLOG		PLMN2		PLMN1	13
14		VSS		VSS		VSS		VSS																						VCC		VCC		VCC		VCC		14
15	SD#63		SD#51		SDIC#3		KEY																								KEY		NC		PLBYC#		PLBYC	15
16		VCC		VCC		VCC		VCC																						VSS		VSS		VSS		VSS		16
17	SD#62		SD#60		SD#48		KEY																								KEY		NC		CLKIN#		CLKIN	17
18		VSS		VSS		VSS		VSS																						VCC		VCC		VCC		VCC		18
19	SCK#7		SD#59		SD#58		NC																								NC		NC		RCLK#		RCLK	19
20		VCC		VCC		VCC		VCC																						VSS		VSS		VSS		VSS		20
21	SD#57		SD#56		SD#36		NC																								NC		CLKFR		K7CO		K7CO#	21
22		VSS		VSS		VSS		VSS																						VCC		VCC		VCC		VCC		22
23	SD#39		SD#37		SD#46		KEY																								NC		VCCA		CNNCT		PRCRDY	23
24		VCC		VCC		VCC		VCC																						VSS		VSS		VSS		VSS		24
25	SD#35		SD#47		SCK#4		KEY																								NC		PLBYP#		NC		NC	25
26		VSS		VSS		VSS		VSS																						VCC		VCC		VCC		VCC		26
27	SD#34		SD#38		SDIC#2		NC																								KEY		NC		NC		NC	27
28		VCC		VCC		VCC		NC																						NC		VSS		VSS		VSS		28
29	SD#44		SD#45		SD#33		NC																								KEY		SAI#0		SAI#1		SAI#12	29
30		VSS		VSS		NC		NC		NC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		NC		NC		NC		VCC		VCC		30
31	SCK#5		SD#43		SD#32		NC		NC		NC		NC		NC		NC		NC		NC		NC		NC		NC		NC		NC		SFILLV#		SDOV#		SAI#14	31
32		VCC		VCC		VCC		NC		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		NC		VSS		VSS		VSS		32
33	SDOC#2		SD#42		SCK#3		SD#20		SD#19		SD#26		SD#25		SD#24		SD#7		SD#5		SDIC#0		SCK#1		SD#8		SD#10		SAI#5		SAI#2		SAIC#		SAI#8		SDINV#	33
34		VSS		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VCC		34
35	SD#40		SD#41		SD#31		SD#23		SDIC#1		SCK#2		SD#27		SD#17		SD#15		SD#4		SD#2		SD#3		SD#0		SD#14		SDOC#0		SAI#11		SAI#6		SAI#4		SAI#13	35
36		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		VCC		VSS		36
37	SD#30		SDOC#1		SD#22		SD#21		SD#29		SD#28		SD#18		SD#16		SD#6		SCK#0		SD#1		SD#12		SD#13		SD#11		SD#9		SAI#7		SAI#3		SAI#10		SAI#9	37
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T	U	V	W	X	Y	Z	AA	AB	AC	AD	AE	AF	AG	AH	AJ	AK	AL	AM	AN	

AMD Athlon™ MP Processor
Model 6
Bottomside View

Figure 13. AMD Athlon™ MP Processor Model 6 Pin Diagram—Bottomside View

Table 17. Pin Name Abbreviations

Abbreviation	Full Name	Pin
	A20M#	AE1
	AMD	AH6
ANLOG	ANALOG	AJ13
CLKFR	CLKFWDRST	AJ21
	CLKIN	AN17
	CLKIN#	AL17
CNNCT	CONNECT	AL23
	COREFB	AG11
	COREFB#	AG13
CPR#	CPU_PRESENCE#	AK6
	DBRDY	AA1
	DBREQ#	AA3
	FERR	AG1
	FID[0]	W1
	FID[1]	W3
	FID[2]	Y1
	FID[3]	Y3
	FLUSH#	AL3
	IGNNE#	AJ1
	INIT#	AJ3
	INTR	AL1
K7CO	K7CLKOUT	AL21
K7CO#	K7CLKOUT#	AN21
	KEY	G7
	KEY	G9
	KEY	G15
	KEY	G17
	KEY	G23
	KEY	G25
	KEY	N7
	KEY	Q7
	KEY	Y7
	KEY	AA7
	KEY	AG7
	KEY	AG9
	KEY	AG15
	KEY	AG17
	KEY	AG27
	KEY	AG29
	NC	F8
	NC	F30
	NC	G11
	NC	G13
	NC	G19
	NC	G21
	NC	G27
	NC	G29
	NC	G31
	NC	H6
	NC	H8
	NC	H10
	NC	H28
	NC	H30
	NC	H32
	NC	J5
	NC	J31
	NC	K8
	NC	K30
	NC	L31
	NC	N31
	NC	Q31
	NC	S31
	NC	U31
	NC	W7
	NC	W31
	NC	Y5
	NC	Y31
	NC	AA5
	NC	AA31
	NC	AC7
	NC	AC31
	NC	AD8
	NC	AD30
	NC	AE7
	NC	AE31
	NC	AF6
	NC	AF8
	NC	AF10

Table 17. Pin Name Abbreviations (Continued)

Abbreviation	Full Name	Pin	Abbreviation	Full Name	Pin
	NC	AF28	PLTST#	PLLTEST#	AC3
	NC	AF30	PRCRDY	PROCREADY	AN23
	NC	AF32		PWROK	AE3
	NC	AG5		RESET#	AG3
	NC	AG19	RCLK	RSTCLK	AN19
	NC	AG21	RCLK#	RSTCLK#	AL19
	NC	AG23	SAI#0	SADDIN[0]#	AJ29
	NC	AG25	SAI#1	SADDIN[1]#	AL29
	NC	AG31	SAI#2	SADDIN[2]#	AG33
	NC	AH8	SAI#3	SADDIN[3]#	AJ37
	NC	AH30	SAI#4	SADDIN[4]#	AL35
	NC	AJ7	SAI#5	SADDIN[5]#	AE33
	NC	AJ9	SAI#6	SADDIN[6]#	AJ35
	NC	AJ11	SAI#7	SADDIN[7]#	AG37
	NC	AJ15	SAI#8	SADDIN[8]#	AL33
	NC	AJ17	SAI#9	SADDIN[9]#	AN37
	NC	AJ19	SAI#10	SADDIN[10]#	AL37
	NC	AJ27	SAI#11	SADDIN[11]#	AG35
	NC	AK8	SAI#12	SADDIN[12]#	AN29
	NC	AL7	SAI#13	SADDIN[13]#	AN35
	NC	AL9	SAI#14	SADDIN[14]#	AN31
	NC	AL11	SAIC#	SADDINCLK#	AJ33
	NC	AL25	SAO#0	SADDOUT[0]#	J1
	NC	AL27	SAO#1	SADDOUT[1]#	J3
	NC	AM8	SAO#2	SADDOUT[2]#	C7
	NC	AN7	SAO#3	SADDOUT[3]#	A7
	NC	AN9	SAO#4	SADDOUT[4]#	E5
	NC	AN11	SAO#5	SADDOUT[5]#	A5
	NC	AN25	SAO#6	SADDOUT[6]#	E7
	NC	AN27	SAO#7	SADDOUT[7]#	C1
	NMI	AN3	SAO#8	SADDOUT[8]#	C5
	PICCLK	N1	SAO#9	SADDOUT[9]#	C3
PICD#0	PICD[0]#	N3	SAO#10	SADDOUT[10]#	G1
PICD#1	PICD[1]#	N5	SAO#11	SADDOUT[11]#	E1
PLBYP#	PLLBYPASS#	AJ25	SAO#12	SADDOUT[12]#	A3
PLBYC	PLLBYPASSCLK	AN15	SAO#13	SADDOUT[13]#	G5
PLBYC#	PLLBYPASSCLK#	AL15	SAO#14	SADDOUT[14]#	G3
PLMN1	PLLMON1	AN13	SAOC#	SADDOUTCLK#	E3
PLMN2	PLLMON2	AL13	SCNCK1	SCANCLK1	S1

Table 17. Pin Name Abbreviations (Continued)

Abbreviation	Full Name	Pin	Abbreviation	Full Name	Pin
SCNCK2	SCANCLK2	S5	SD#28	SDATA[28]#	L37
SCNINV	SCANINTEVAL	S3	SD#29	SDATA[29]#	J37
SCNSN	SCANSHIFTEN	Q5	SD#30	SDATA[30]#	A37
SCK#0	SCHECK[0]#	U37	SD#31	SDATA[31]#	E35
SCK#1	SCHECK[1]#	Y33	SD#32	SDATA[32]#	E31
SCK#2	SCHECK[2]#	L35	SD#33	SDATA[33]#	E29
SCK#3	SCHECK[3]#	E33	SD#34	SDATA[34]#	A27
SCK#4	SCHECK[4]#	E25	SD#35	SDATA[35]#	A25
SCK#5	SCHECK[5]#	A31	SD#36	SDATA[36]#	E21
SCK#6	SCHECK[6]#	C13	SD#37	SDATA[37]#	C23
SCK#7	SCHECK[7]#	A19	SD#38	SDATA[38]#	C27
SD#0	SDATA[0]#	AA35	SD#39	SDATA[39]#	A23
SD#1	SDATA[1]#	W37	SD#40	SDATA[40]#	A35
SD#2	SDATA[2]#	W35	SD#41	SDATA[41]#	C35
SD#3	SDATA[3]#	Y35	SD#42	SDATA[42]#	C33
SD#4	SDATA[4]#	U35	SD#43	SDATA[43]#	C31
SD#5	SDATA[5]#	U33	SD#44	SDATA[44]#	A29
SD#6	SDATA[6]#	S37	SD#45	SDATA[45]#	C29
SD#7	SDATA[7]#	S33	SD#46	SDATA[46]#	E23
SD#8	SDATA[8]#	AA33	SD#47	SDATA[47]#	C25
SD#9	SDATA[9]#	AE37	SD#48	SDATA[48]#	E17
SD#10	SDATA[10]#	AC33	SD#49	SDATA[49]#	E13
SD#11	SDATA[11]#	AC37	SD#50	SDATA[50]#	E11
SD#12	SDATA[12]#	Y37	SD#51	SDATA[51]#	C15
SD#13	SDATA[13]#	AA37	SD#52	SDATA[52]#	E9
SD#14	SDATA[14]#	AC35	SD#53	SDATA[53]#	A13
SD#15	SDATA[15]#	S35	SD#54	SDATA[54]#	C9
SD#16	SDATA[16]#	Q37	SD#55	SDATA[55]#	A9
SD#17	SDATA[17]#	Q35	SD#56	SDATA[56]#	C21
SD#18	SDATA[18]#	N37	SD#57	SDATA[57]#	A21
SD#19	SDATA[19]#	J33	SD#58	SDATA[58]#	E19
SD#20	SDATA[20]#	G33	SD#59	SDATA[59]#	C19
SD#21	SDATA[21]#	G37	SD#60	SDATA[60]#	C17
SD#22	SDATA[22]#	E37	SD#61	SDATA[61]#	A11
SD#23	SDATA[23]#	G35	SD#62	SDATA[62]#	A17
SD#24	SDATA[24]#	Q33	SD#63	SDATA[63]#	A15
SD#25	SDATA[25]#	N33	SDIC#0	SDATAINCLK[0]#	W33
SD#26	SDATA[26]#	L33	SDIC#1	SDATAINCLK[1]#	J35
SD#27	SDATA[27]#	N35	SDIC#2	SDATAINCLK[2]#	E27

Table 17. Pin Name Abbreviations (Continued)

Abbreviation	Full Name	Pin	Abbreviation	Full Name	Pin
SDIC#3	SDATAINCLK[3]#	E15	VCC	VCC_CORE	F28
SDINV#	SDATAINVALID#	AN33	VCC	VCC_CORE	F32
SDOC#0	SDATAOUTCLK[0]#	AE35	VCC	VCC_CORE	F34
SDOC#1	SDATAOUTCLK[1]#	C37	VCC	VCC_CORE	F36
SDOC#2	SDATAOUTCLK[2]#	A33	VCC	VCC_CORE	H2
SDOC#3	SDATAOUTCLK[3]#	C11	VCC	VCC_CORE	H4
SDOV#	SDATAOUTVALID#	AL31	VCC	VCC_CORE	H12
SFILLV#	SFILLVALID#	AJ31	VCC	VCC_CORE	H16
	SMI#	AN5	VCC	VCC_CORE	H20
STPC#	STPCLK#	AC1	VCC	VCC_CORE	H24
	TCK	Q1	VCC	VCC_CORE	K32
	TDI	U1	VCC	VCC_CORE	K34
	TDO	U5	VCC	VCC_CORE	K36
THDA	THERMDA	S7	VCC	VCC_CORE	M2
THDC	THERMDC	U7	VCC	VCC_CORE	M4
	TMS	Q3	VCC	VCC_CORE	M6
	TRST#	U3	VCC	VCC_CORE	M8
VCC	VCC_CORE	B4	VCC	VCC_CORE	P30
VCC	VCC_CORE	B8	VCC	VCC_CORE	P32
VCC	VCC_CORE	B12	VCC	VCC_CORE	P34
VCC	VCC_CORE	B16	VCC	VCC_CORE	P36
VCC	VCC_CORE	B20	VCC	VCC_CORE	R2
VCC	VCC_CORE	B24	VCC	VCC_CORE	R4
VCC	VCC_CORE	B28	VCC	VCC_CORE	R6
VCC	VCC_CORE	B32	VCC	VCC_CORE	R8
VCC	VCC_CORE	B36	VCC	VCC_CORE	T30
VCC	VCC_CORE	D2	VCC	VCC_CORE	T32
VCC	VCC_CORE	D4	VCC	VCC_CORE	T34
VCC	VCC_CORE	D8	VCC	VCC_CORE	T36
VCC	VCC_CORE	D12	VCC	VCC_CORE	V2
VCC	VCC_CORE	D16	VCC	VCC_CORE	V4
VCC	VCC_CORE	D20	VCC	VCC_CORE	V6
VCC	VCC_CORE	D24	VCC	VCC_CORE	V8
VCC	VCC_CORE	D28	VCC	VCC_CORE	X30
VCC	VCC_CORE	D32	VCC	VCC_CORE	X32
VCC	VCC_CORE	F12	VCC	VCC_CORE	X34
VCC	VCC_CORE	F16	VCC	VCC_CORE	X36
VCC	VCC_CORE	F20	VCC	VCC_CORE	Z2
VCC	VCC_CORE	F24	VCC	VCC_CORE	Z4

Table 17. Pin Name Abbreviations (Continued)

Abbreviation	Full Name	Pin	Abbreviation	Full Name	Pin
VCC	VCC_CORE	Z6	VCC	VCC_CORE	AM26
VCC	VCC_CORE	Z8	VCC	VCC_CORE	AM30
VCC	VCC_CORE	AB30	VCC	VCC_CORE	AM34
VCC	VCC_CORE	AB32		VCCA	AJ23
VCC	VCC_CORE	AB34		VID[0]	L1
VCC	VCC_CORE	AB36		VID[1]	L3
VCC	VCC_CORE	AD2		VID[2]	L5
VCC	VCC_CORE	AD4		VID[3]	L7
VCC	VCC_CORE	AD6		VID[4]	J7
VCC	VCC_CORE	AF14	VREF_S	VREF_SYS	W5
VCC	VCC_CORE	AF18		VSS	B2
VCC	VCC_CORE	AF22		VSS	B6
VCC	VCC_CORE	AF26		VSS	B10
VCC	VCC_CORE	AF34		VSS	B14
VCC	VCC_CORE	AF36		VSS	B18
VCC	VCC_CORE	AH2		VSS	B22
VCC	VCC_CORE	AH4		VSS	B26
VCC	VCC_CORE	AH10		VSS	B30
VCC	VCC_CORE	AH14		VSS	B34
VCC	VCC_CORE	AH18		VSS	D6
VCC	VCC_CORE	AH22		VSS	D10
VCC	VCC_CORE	AH26		VSS	D14
VCC	VCC_CORE	AK10		VSS	D18
VCC	VCC_CORE	AK14		VSS	D22
VCC	VCC_CORE	AK18		VSS	D26
VCC	VCC_CORE	AK22		VSS	D30
VCC	VCC_CORE	AK26		VSS	D34
VCC	VCC_CORE	AK30		VSS	D36
VCC	VCC_CORE	AK34		VSS	F2
VCC	VCC_CORE	AK36		VSS	F4
VCC	VCC_CORE	AJ5		VSS	F6
VCC	VCC_CORE	AL5		VSS	F10
VCC	VCC_CORE	AM2		VSS	F14
VCC	VCC_CORE	AM10		VSS	F18
VCC	VCC_CORE	AM14		VSS	F22
VCC	VCC_CORE	AM18		VSS	F26
VCC	VCC_CORE	AM22		VSS	H14
VCC	VCC_CORE	AM26		VSS	H18
VCC	VCC_CORE	AM22		VSS	H22

Table 17. Pin Name Abbreviations (Continued)

Abbreviation	Full Name	Pin
	VSS	H26
	VSS	H34
	VSS	H36
	VSS	K2
	VSS	K4
	VSS	K6
	VSS	M30
	VSS	M32
	VSS	M34
	VSS	M36
	VSS	P2
	VSS	P4
	VSS	P6
	VSS	P8
	VSS	R30
	VSS	R32
	VSS	R34
	VSS	R36
	VSS	T2
	VSS	T4
	VSS	T6
	VSS	T8
	VSS	V30
	VSS	V32
	VSS	V34
	VSS	V36
	VSS	X2
	VSS	X4
	VSS	X6
	VSS	X8
	VSS	Z30
	VSS	Z32
	VSS	Z34
	VSS	Z36
	VSS	AB2
	VSS	AB8
	VSS	AB4
	VSS	AB6
	VSS	AD32
	VSS	AD34
	VSS	AD36
	VSS	AF2
	VSS	AF4
	VSS	AF12
	VSS	AF16
	VSS	AH12
	VSS	AH16
	VSS	AH20
	VSS	AH24
	VSS	AH28
	VSS	AH32
	VSS	AH34
	VSS	AH36
	VSS	AK2
	VSS	AK4
	VSS	AK12
	VSS	AK16
	VSS	AK20
	VSS	AK24
	VSS	AK28
	VSS	AK32
	VSS	AM4
	VSS	AM6
	VSS	AM12
	VSS	AM16
	VSS	AM20
	VSS	AM24
	VSS	AM28
	VSS	AM32
	VSS	AM36
	ZN	AC5
	ZP	AE5

10.2 Pin List

Table 18 cross-references Socket A pin location to signal name.

The "L" (Level) column shows the electrical specification for this pin. "P" indicates a push-pull mode driven by a single source. "O" indicates open-drain mode that allows devices to share the pin.

Note: *The Socket A AMD Athlon MP processor supports push-pull drivers. For more information, see "Push–Pull (PP) Drivers" on page 6.*

The "P" (Port) column indicates if this signal is an input (I), output (O), or bidirectional (B) signal. The "R" (Reference) column indicates if this signal should be referenced to VSS (G) or VCC_CORE (P) planes for the purpose of signal routing with respect to the current return paths.

Table 18. Cross-Reference by Pin Location

Pin	Name	Description	L	P	R
A1	No Pin	page 63	-	-	-
A3	SADDOUT[12]#		P	O	G
A5	SADDOUT[5]#		P	O	G
A7	SADDOUT[3]#		P	O	G
A9	SDATA[55]#		P	B	P
A11	SDATA[61]#		P	B	P
A13	SDATA[53]#		P	B	G
A15	SDATA[63]#		P	B	G
A17	SDATA[62]#		P	B	G
A19	SCHECK[7]#	page 64	P	B	G
A21	SDATA[57]#		P	B	G
A23	SDATA[39]#		P	B	G
A25	SDATA[35]#		P	B	P
A27	SDATA[34]#		P	B	P
A29	SDATA[44]#		P	B	G
A31	SCHECK[5]#	page 64	P	B	G
A33	SDATAOUTCLK[2]#		P	O	P
A35	SDATA[40]#		P	B	G
A37	SDATA[30]#		P	B	P
B2	VSS		-	-	-
B4	VCC_CORE		-	-	-
B6	VSS		-	-	-
B8	VCC_CORE		-	-	-
B10	VSS		-	-	-
B12	VCC_CORE		-	-	-
B14	VSS		-	-	-
B16	VCC_CORE		-	-	-
B18	VSS		-	-	-
B20	VCC_CORE		-	-	-
B22	VSS		-	-	-
B24	VCC_CORE		-	-	-
B26	VSS		-	-	-
B28	VCC_CORE		-	-	-
B30	VSS		-	-	-
B32	VCC_CORE		-	-	-
B34	VSS		-	-	-

Table 18. Cross-Reference by Pin Location (continued)

Pin	Name	Description	L	P	R	Pin	Name	Description	L	P	R
B36	VCC_CORE		-	-	-	D30	VSS		-	-	-
C1	SADDOUT[7]#		P	O	G	D32	VCC_CORE		-	-	-
C3	SADDOUT[9]#		P	O	G	D34	VSS		-	-	-
C5	SADDOUT[8]#		P	O	G	D36	VSS		-	-	-
C7	SADDOUT[2]#		P	O	G	E1	SADDOUT[11]#		P	O	P
C9	SDATA[54]#		P	B	P	E3	SADDOUTCLK#		P	O	G
C11	SDATAOUTCLK[3]#		P	O	G	E5	SADDOUT[4]#		P	O	P
C13	SCHECK[6]#	page 64	P	B	G	E7	SADDOUT[6]#		P	O	G
C15	SDATA[51]#		P	B	P	E9	SDATA[52]#		P	B	P
C17	SDATA[60]#		P	B	G	E11	SDATA[50]#		P	B	P
C19	SDATA[59]#		P	B	G	E13	SDATA[49]#		P	B	G
C21	SDATA[56]#		P	B	G	E15	SDATAINCLK[3]#		P	I	G
C23	SDATA[37]#		P	B	P	E17	SDATA[48]#		P	B	P
C25	SDATA[47]#		P	B	G	E19	SDATA[58]#		P	B	G
C27	SDATA[38]#		P	B	G	E21	SDATA[36]#		P	B	P
C29	SDATA[45]#		P	B	G	E23	SDATA[46]#		P	B	P
C31	SDATA[43]#		P	B	G	E25	SCHECK[4]#	page 64	P	B	P
C33	SDATA[42]#		P	B	G	E27	SDATAINCLK[2]#		P	I	G
C35	SDATA[41]#		P	B	G	E29	SDATA[33]#		P	B	P
C37	SDATAOUTCLK[1]#		P	O	G	E31	SDATA[32]#		P	B	P
D2	VCC_CORE		-	-	-	E33	SCHECK[3]#	page 64	P	B	P
D4	VCC_CORE		-	-	-	E35	SDATA[31]#		P	B	P
D6	VSS		-	-	-	E37	SDATA[22]#		P	B	G
D8	VCC_CORE		-	-	-	F2	VSS		-	-	-
D10	VSS		-	-	-	F4	VSS		-	-	-
D12	VCC_CORE		-	-	-	F6	VSS		-	-	-
D14	VSS		-	-	-	F8	NC Pin	page 63	-	-	-
D16	VCC_CORE		-	-	-	F10	VSS		-	-	-
D18	VSS		-	-	-	F12	VCC_CORE		-	-	-
D20	VCC_CORE		-	-	-	F14	VSS		-	-	-
D22	VSS		-	-	-	F16	VCC_CORE		-	-	-
D24	VCC_CORE		-	-	-	F18	VSS		-	-	-
D26	VSS		-	-	-	F20	VCC_CORE		-	-	-
D28	VCC_CORE		-	-	-	F22	VSS		-	-	-

Table 18. Cross-Reference by Pin Location (continued)

Pin	Name	Description	L	P	R
F24	VCC_CORE		-	-	-
F26	VSS		-	-	-
F28	VCC_CORE		-	-	-
F30	NC Pin	page 63	-	-	-
F32	VCC_CORE		-	-	-
F34	VCC_CORE		-	-	-
F36	VCC_CORE		-	-	-
G1	SADDOUT[10]#		P	O	P
G3	SADDOUT[14]#		P	O	G
G5	SADDOUT[13]#		P	O	G
G7	Key Pin	page 63	-	-	-
G9	Key Pin	page 63	-	-	-
G11	NC Pin	page 63	-	-	-
G13	NC Pin	page 63	-	-	-
G15	Key Pin	page 63	-	-	-
G17	Key Pin	page 63	-	-	-
G19	NC Pin	page 63	-	-	-
G21	NC Pin	page 63	-	-	-
G23	Key Pin	page 63	-	-	-
G25	Key Pin	page 63	-	-	-
G27	NC Pin	page 63	-	-	-
G29	NC Pin	page 63	-	-	-
G31	NC Pin	page 63	-	-	-
G33	SDATA[20]#		P	B	G
G35	SDATA[23]#		P	B	G
G37	SDATA[21]#		P	B	G
H2	VCC_CORE		-	-	-
H4	VCC_CORE		-	-	-
H6	NC Pin	page 63	-	-	-
H8	NC Pin	page 63	-	-	-
H10	NC Pin	page 63	-	-	-
H12	VCC_CORE		-	-	-
H14	VSS		-	-	-
H16	VCC_CORE		-	-	-
H18	VSS		-	-	-
H20	VCC_CORE		-	-	-
H22	VSS		-	-	-
H24	VCC_CORE		-	-	-
H26	VSS		-	-	-
H28	NC Pin	page 63	-	-	-
H30	NC Pin	page 63	-	-	-
H32	NC Pin	page 63	-	-	-
H34	VSS		-	-	-
H36	VSS		-	-	-
J1	SADDOUT[0]#	page 64	P	O	-
J3	SADDOUT[1]#	page 64	P	O	-
J5	NC Pin	page 63	-	-	-
J7	VID[4]	page 65	O	O	-
J31	NC Pin	page 63	-	-	-
J33	SDATA[19]#		P	B	G
J35	SDATAINCLK[1]#		P	I	P
J37	SDATA[29]#		P	B	P
K2	VSS		-	-	-
K4	VSS		-	-	-
K6	VSS		-	-	-
K8	NC Pin	page 63	-	-	-
K30	NC Pin	page 63	-	-	-
K32	VCC_CORE		-	-	-
K34	VCC_CORE		-	-	-
K36	VCC_CORE		-	-	-
L1	VID[0]	page 65	O	O	-
L3	VID[1]	page 65	O	O	-
L5	VID[2]	page 65	O	O	-
L7	VID[3]	page 65	O	O	-
L31	NC Pin	page 63	-	-	-
L33	SDATA[26]#		P	B	P
L35	SCHECK[2]#	page 64	P	B	G
L37	SDATA[28]#		P	B	P

Table 18. Cross-Reference by Pin Location (continued)

Pin	Name	Description	L	P	R	Pin	Name	Description	L	P	R
M2	VCC_CORE		-	-	-	R6	VCC_CORE		-	-	-
M4	VCC_CORE		-	-	-	R8	VCC_CORE		-	-	-
M6	VCC_CORE		-	-	-	R30	VSS		-	-	-
M8	VCC_CORE		-	-	-	R32	VSS		-	-	-
M30	VSS		-	-	-	R34	VSS		-	-	-
M32	VSS		-	-	-	R36	VSS		-	-	-
M34	VSS		-	-	-	S1	SCANCLK1	page 64	P	I	-
M36	VSS		-	-	-	S3	SCANINTEVAL	page 64	P	I	-
N1	PICCLK	page 60	O	I	-	S5	SCANCLK2	page 64	P	I	-
N3	PICD#[0]	page 60	O	B	-	S7	THERMDA	page 64	-	-	-
N5	PICD#[1]	page 60	O	B	-	S31	NC Pin	page 63	-	-	-
N7	Key Pin	page 63	-	-	-	S33	SDATA[7]#		P	B	G
N31	NC Pin	page 63	-	-	-	S35	SDATA[15]#		P	B	P
N33	SDATA[25]#		P	B	P	S37	SDATA[6]#		P	B	G
N35	SDATA[27]#		P	B	P	T2	VSS		-	-	-
N37	SDATA[18]#		P	B	G	T4	VSS		-	-	-
P2	VSS		-	-	-	T6	VSS		-	-	-
P4	VSS		-	-	-	T8	VSS		-	-	-
P6	VSS		-	-	-	T30	VCC_CORE		-	-	-
P8	VSS		-	-	-	T32	VCC_CORE		-	-	-
P30	VCC_CORE		-	-	-	T34	VCC_CORE		-	-	-
P32	VCC_CORE		-	-	-	T36	VCC_CORE		-	-	-
P34	VCC_CORE		-	-	-	U1	TDI	page 63	P	I	-
P36	VCC_CORE		-	-	-	U3	TRST#	page 63	P	I	-
Q1	TCK	page 63	P	I	-	U5	TDO	page 63	P	O	-
Q3	TMS	page 63	P	I	-	U7	THERMDC	page 64	-	-	-
Q5	SCANSHIFTEN	page 64	P	I	-	U31	NC Pin	page 63	-	-	-
Q7	Key Pin	page 63	-	-	-	U33	SDATA[5]#		P	B	G
Q31	NC Pin	page 63	-	-	-	U35	SDATA[4]#		P	B	G
Q33	SDATA[24]#		P	B	P	U37	SCHECK[0]#	page 64	P	B	G
Q35	SDATA[17]#		P	B	G	V2	VCC_CORE		-	-	-
Q37	SDATA[16]#		P	B	G	V4	VCC_CORE		-	-	-
R2	VCC_CORE		-	-	-	V6	VCC_CORE		-	-	-
R4	VCC_CORE		-	-	-	V8	VCC_CORE		-	-	-

Table 18. Cross-Reference by Pin Location (continued)

Pin	Name	Description	L	P	R	Pin	Name	Description	L	P	R
V30	VSS		-	-	-	Z34	VSS		-	-	-
V32	VSS		-	-	-	Z36	VSS		-	-	-
V34	VSS		-	-	-	AA1	DBRDY	page 61	P	O	-
V36	VSS		-	-	-	AA3	DBREQ#	page 61	P	I	-
W1	FID[0]	page 61	O	O	-	AA5	NC		-	-	-
W3	FID[1]	page 61	O	O	-	AA7	Key Pin	page 63	-	-	-
W5	VREFSYS	page 65	P	-	-	AA31	NC Pin	page 63	-	-	-
W7	NC Pin	page 63	-	-	-	AA33	SDATA[8]#		P	B	P
W31	NC Pin	page 63	-	-	-	AA35	SDATA[0]#		P	B	G
W33	SDATAINCLK[0]#		P	I	G	AA37	SDATA[13]#		P	B	G
W35	SDATA[2]#		P	B	G	AB2	VSS		-	-	-
W37	SDATA[1]#		P	B	P	AB4	VSS		-	-	-
X2	VSS		-	-	-	AB6	VSS		-	-	-
X4	VSS		-	-	-	AB8	VSS		-	-	-
X6	VSS		-	-	-	AB30	VCC_CORE		-	-	-
X8	VSS		-	-	-	AB32	VCC_CORE		-	-	-
X30	VCC_CORE		-	-	-	AB34	VCC_CORE		-	-	-
X32	VCC_CORE		-	-	-	AB36	VCC_CORE		-	-	-
X34	VCC_CORE		-	-	-	AC1	STPCLK#	page 64	P	I	-
X36	VCC_CORE		-	-	-	AC3	PLLTEST#	page 63	P	I	-
Y1	FID[2]	page 61	O	O	-	AC5	ZN	page 66	P	-	-
Y3	FID[3]	page 61	O	O	-	AC7	NC		-	-	-
Y5	NC Pin	page 63	-	-	-	AC31	NC Pin	page 63	-	-	-
Y7	Key Pin	page 63	-	-	-	AC33	SDATA[10]#		P	B	P
Y31	NC Pin	page 63	-	-	-	AC35	SDATA[14]#		P	B	G
Y33	SCHECK[1]#	page 64	P	B	P	AC37	SDATA[11]#		P	B	G
Y35	SDATA[3]#		P	B	G	AD2	VCC_CORE		-	-	-
Y37	SDATA[12]#		P	B	P	AD4	VCC_CORE		-	-	-
Z2	VCC_CORE		-	-	-	AD6	VCC_CORE		-	-	-
Z4	VCC_CORE		-	-	-	AD8	NC Pin	page 63	-	-	-
Z6	VCC_CORE		-	-	-	AD30	NC Pin	page 63	-	-	-
Z8	VCC_CORE		-	-	-	AD32	VSS		-	-	-
Z30	VSS		-	-	-	AD34	VSS		-	-	-
Z32	VSS		-	-	-	AD36	VSS		-	-	-

Table 18. Cross-Reference by Pin Location (continued)

Pin	Name	Description	L	P	R	Pin	Name	Description	L	P	R
AE1	A20M#		P	I	-	AG17	Key Pin	page 63	-	-	-
AE3	PWROK		P	I	-	AG19	NC Pin	page 63	-	-	-
AE5	ZP	page 66	P	-	-	AG21	NC Pin	page 63	-	-	-
AE7	NC		-	-	-	AG23	NC Pin	page 63	-	-	-
AE31	NC Pin	page 63	-	-	-	AG25	NC Pin	page 63	-	-	-
AE33	SADDIN[5]#		P	I	G	AG27	Key Pin	page 63	-	-	-
AE35	SDATAOUTCLK[0]#		P	O	P	AG29	Key Pin	page 63	-	-	-
AE37	SDATA[9]#		P	B	G	AG31	NC Pin	page 63	-	-	-
AF2	VSS		-	-	-	AG33	SADDIN[2]#		P	I	G
AF4	VSS		-	-	-	AG35	SADDIN[11]#		P	I	G
AF6	NC Pin	page 63	-	-	-	AG37	SADDIN[7]#		P	I	P
AF8	NC Pin	page 63	-	-	-	AH2	VCC_CORE		-	-	-
AF10	NC Pin	page 63	-	-	-	AH4	VCC_CORE		-	-	-
AF12	VSS		-	-	-	AH6	AMD Pin	page 60	-	-	-
AF14	VCC_CORE		-	-	-	AH8	NC Pin	page 63	-	-	-
AF16	VSS		-	-	-	AH10	VCC_CORE		-	-	-
AF18	VCC_CORE		-	-	-	AH12	VSS		-	-	-
AF20	VSS		-	-	-	AH14	VCC_CORE		-	-	-
AF22	VCC_CORE		-	-	-	AH16	VSS		-	-	-
AF24	VSS		-	-	-	AH18	VCC_CORE		-	-	-
AF26	VCC_CORE		-	-	-	AH20	VSS		-	-	-
AF28	NC Pin	page 63	-	-	-	AH22	VCC_CORE		-	-	-
AF30	NC Pin	page 63	-	-	-	AH24	VSS		-	-	-
AF32	NC Pin	page 63	-	-	-	AH26	VCC_CORE		-	-	-
AF34	VCC_CORE		-	-	-	AH28	VSS		-	-	-
AF36	VCC_CORE		-	-	-	AH30	NC Pin	page 63	-	-	-
AG1	FERR	page 61	P	O	-	AH32	VSS		-	-	-
AG3	RESET#		-	I	-	AH34	VSS		-	-	-
AG5	NC Pin	page 63	-	-	-	AH36	VSS		-	-	-
AG7	Key Pin	page 63	-	-	-	AJ1	IGNNE#	page 62	P	I	-
AG9	Key Pin	page 63	-	-	-	AJ3	INIT#	page 63	P	I	-
AG11	COREFB	page 61	-	-	-	AJ5	VCC_CORE		-	-	-
AG13	COREFB#	page 61	-	-	-	AJ7	NC Pin	page 63	-	-	-
AG15	Key Pin	page 63	-	-	-	AJ9	NC Pin	page 63	-	-	-

Table 18. Cross-Reference by Pin Location (continued)

Pin	Name	Description	L	P	R
AJ11	NC Pin	page 63	-	-	-
AJ13	Analog	page 60	-	-	-
AJ15	NC Pin	page 63	-	-	-
AJ17	NC Pin	page 63	-	-	-
AJ19	NC Pin	page 63	-	-	-
AJ21	CLKFWDRST	page 60	P	I	P
AJ23	VCCA	page 65	-	-	-
AJ25	PLLBYPASS#	page 63	P	I	-
AJ27	NC Pin	page 63	-	-	-
AJ29	SADDIN[0]#	page 64	P	I	-
AJ31	SFILLVALID#		P	I	G
AJ33	SADDINCLK#		P	I	G
AJ35	SADDIN[6]#		P	I	P
AJ37	SADDIN[3]#		P	I	G
AK2	VSS		-	-	-
AK4	VSS		-	-	-
AK6	CPU_PRESENCE#	page 61	-	-	-
AK8	NC Pin	page 63	-	-	-
AK10	VCC_CORE		-	-	-
AK12	VSS		-	-	-
AK14	VCC_CORE		-	-	-
AK16	VSS		-	-	-
AK18	VCC_CORE		-	-	-
AK20	VSS		-	-	-
AK22	VCC_CORE		-	-	-
AK24	VSS		-	-	-
AK26	VCC_CORE		-	-	-
AK28	VSS		-	-	-
AK30	VCC_CORE		-	-	-
AK32	VSS		-	-	-
AK34	VCC_CORE		-	-	-
AK36	VCC_CORE		-	-	-
AL1	INTR	page 63	P	I	-
AL3	FLUSH#	page 62	P	I	-

Pin	Name	Description	L	P	R
AL5	VCC_CORE		-	-	-
AL7	NC Pin	page 63	-	-	-
AL9	NC Pin	page 63	-	-	-
AL11	NC Pin	page 63	-	-	-
AL13	PLLMON2	page 63	O	O	-
AL15	PLLBYPASSCLK#	page 63	P	I	-
AL17	CLKIN#	page 60	P	I	P
AL19	RSTCLK#	page 60	P	I	P
AL21	K7CLKOUT	page 63	P	O	-
AL23	CONNECT	page 61	P	I	P
AL25	NC Pin	page 63	-	-	-
AL27	NC Pin	page 63	-	-	-
AL29	SADDIN[1]#	page 64	P	I	-
AL31	SDATAOUTVALID#		P	O	P
AL33	SADDIN[8]#		P	I	P
AL35	SADDIN[4]#		P	I	G
AL37	SADDIN[10]#		P	I	G
AM2	VCC_CORE		-	-	-
AM4	VSS		-	-	-
AM6	VSS		-	-	-
AM8	NC Pin	page 63	-	-	-
AM10	VCC_CORE		-	-	-
AM12	VSS		-	-	-
AM14	VCC_CORE		-	-	-
AM16	VSS		-	-	-
AM18	VCC_CORE		-	-	-
AM20	VSS		-	-	-
AM22	VCC_CORE		-	-	-
AM24	VSS		-	-	-
AM26	VCC_CORE		-	-	-
AM28	VSS		-	-	-
AM30	VCC_CORE		-	-	-
AM32	VSS		-	-	-
AM34	VCC_CORE		-	-	-

Table 18. Cross-Reference by Pin Location (continued)

Pin	Name	Description	L	P	R
AM36	VSS		-	-	-
AN1	No Pin	page 63	-	-	-
AN3	NMI		P	I	-
AN5	SMI#		P	I	-
AN7	NC Pin	page 63	-	-	-
AN9	NC Pin	page 63	-	-	-
AN11	NC Pin	page 63	-	-	-
AN13	PLLMON1	page 63	O	B	-
AN15	PLLBYPASSCLK	page 63	P	I	-
AN17	CLKIN	page 60	P	I	P
AN19	RSTCLK	page 60	P	I	P
AN21	K7CLKOUT#	page 63	P	O	-
AN23	PROCRDY		P	O	P
AN25	NC Pin	page 63	-	-	-
AN27	NC Pin	page 63	-	-	-
AN29	SADDIN[12]#		P	I	G
AN31	SADDIN[14]#		P	I	G
AN33	SDATAINVALID#		P	I	P
AN35	SADDIN[13]#		P	I	G
AN37	SADDIN[9]#		P	I	G

10.3 Detailed Pin Descriptions

The information in this section pertains to Table 18 on page 52.

A20M# Pin

A20M# is an input from the system used to simulate address wrap-around in the 20-bit 8086.

AMD Pin

AMD Socket A processors do not implement a pin at location AH6. All Socket A designs must have a top plate or cover that blocks this pin location. When the cover plate blocks this location, a non-AMD part (e.g., PGA370) does not fit into the socket. However, socket manufacturers are allowed to have a contact loaded in the AH6 position. Therefore, motherboard socket design should account for the possibility that a contact could be loaded in this position.

AMD Athlon™ System Bus Pins

See the *AMD Athlon™ and AMD Duron™ System Bus Specification*, order# 21902 for information about the system bus pins—PROCRDY, PWROK, RESET#, SADDIN[14:2]#, SADDINCLK#, SADDOUT[14:2]#, SADDOUTCLK#, SCHECK[7:0]#, SDATA[63:0]#, SDATAINCLK[3:0]#, SDATAINVALID#, SDATAOUTCLK[3:0]#, SDATAOUTVALID#, SFILLVALID#.

Analog Pin

Treat this pin as a NC.

APIC Pins, PICCLK, PICD[1:0]#

The Advanced Programmable Interrupt Controller (APIC) is a feature that provides a flexible and expandable means of delivering interrupts in a system using an AMD processor. The pins, PICD[1:0], are the bi-directional message-passing signals used for the APIC and are driven to the Southbridge, a dedicated I/O APIC, or another multiprocessing-enabled AMD Athlon MP processor model 6. The pin, PICCLK, must be driven with a valid clock input.

For more information, see Table 15, “APIC Pins AC and DC Characteristics,” on page 36.

CLKFWDRST Pin

CLKFWDRST resets clock-forward circuitry for both the system and processor.

CLKIN, RSTCLK (SYSCLK) Pins

Connect CLKIN (AN17) with RSTCLK (AN19) and name it SYSCLK. Connect CLKIN# (AL17) with RSTCLK# (AL19) and name it SYSCLK#. Length match the clocks from the clock generator to the Northbridge and processor.

See “SYSCLK and SYSCLK#” on page 64 for more information.

CONNECT Pin

CONNECT is an input from the system used for power management and clock-forward initialization at reset.

COREFB and COREFB# Pins

COREFB and COREFB# are outputs to the system that provide processor core voltage feedback to the system.

CPU_PRESENCE# Pin

CPU_PRESENCE# is connected to VSS on the processor package. If pulled-up on the motherboard, CPU_PRESENCE# may be used to detect the presence or absence of a processor in the Socket A-style socket.

DBRDY and DBREQ# Pins

DBRDY (AA1) and DBREQ# (AA3) are routed to the debug connector. DBREQ# is tied to VCC_CORE with a pullup resistor.

FERR Pin

FERR is an output to the system that is asserted for any unmasked numerical exception independent of the NE bit in CR0. FERR is a push-pull active High signal that must be inverted and level shifted to an active Low signal. For more information about FERR and FERR#, see the “Required Circuits” chapter of the *Socket A Motherboard Design Guide*, order# 24363.

FID[3:0] Pins

FID[3] (Y3), FID[2] (Y1), FID[1] (W3), and FID[0] (W1) are the 4-bit processor clock-to-SYSCLK ratio.

Table 19 on page 61 describes the encodings of the clock multipliers on FID[3:0].

Table 19. FID[3:0] Clock Multiplier Encodings

FID[3]	FID[2]	FID[1]	FID[0]	Processor Clock to SYSCLK Frequency Ratio
0	0	0	0	11
0	0	0	1	11.5
0	0	1	0	12
0	0	1	1	≥ 12.5*
0	1	0	0	5
0	1	0	1	5.5
0	1	1	0	6
0	1	1	1	6.5

Table 19. FID[3:0] Clock Multiplier Encodings (Continued)

FID[3]	FID[2]	FID[1]	FID[0]	Processor Clock to SYSCLK Frequency Ratio
1	0	0	0	7
1	0	0	1	7.5
1	0	1	0	8
1	0	1	1	8.5
1	1	0	0	9
1	1	0	1	9.5
1	1	1	0	10
1	1	1	1	10.5

Note:

**All ratios greater than or equal to 12.5x have the same FID[3:0] code of 0011, which causes the SIP configuration for all ratios of 12.5x or greater to be the same.*

The FID[3:0] signals are open drain processor outputs that are pulled High on the motherboard and sampled by the Northbridge at the deassertion of RESET# to determine the SIP (serialization initialization packet) that gets sent to the processor. See the *AMD Athlon™ and AMD Duron™ System Bus Specification*, order#21902 for more information about the SIP and SIP protocol.

The processor FID[3:0] outputs are open drain and 2.5V tolerant. **To prevent damage to the processor, if these signals are pulled High to above 2.5 V, they must be electrically isolated from the processor.** For information about the FID[3:0] isolation circuit, see the *AMD Athlon™ Processor Based Motherboard Design Guide*, order# 24363.

See "Frequency Identification (FID[3:0])" on page 25 for the AC and DC characteristics for FID[3:0].

FLUSH# Pin

FLUSH# must be tied to VCC_CORE with a pullup resistor. If a debug connector is implemented, FLUSH# is routed to the debug connector.

IGNNE# Pin

IGNNE# is an input from the system that tells the processor to ignore numeric errors.

INIT# Pin

INIT# is an input from the system that resets the integer registers without affecting the floating-point registers or the internal caches. Execution starts at 0FFFF FFF0h.

INTR Pin

INTR is an input from the system that causes the processor to start an interrupt acknowledge transaction that fetches the 8-bit interrupt vector and starts execution at that location.

JTAG Pins

TCK (Q1), TMS (Q3), TDI (U1), TRST# (U3), and TDO (U5) are the JTAG interface. Connect these pins directly to the motherboard debug connector. Pullup TDI, TCK, TMS, and TRST# to VCC_CORE with pullup resistors.

K7CLKOUT and K7CLKOUT# Pins

K7CLKOUT (AL21) and K7CLKOUT# (AN21) are each run for 2 to 3 inches and then terminated with a resistor pair, 100 ohms to VCC_CORE and 100 ohms to VSS. The effective termination resistance and voltage are 50 ohms and VCC_CORE/2.

Key Pins

These 16 locations are for processor type keying for forwards and backwards compatibility (G7, G9, G15, G17, G23, G25, N7, Q7, Y7, AA7, AG7, AG9, AG15, AG17, AG27, and AG29). Motherboard designers should treat key pins like NC (no connect) pins. A socket designer has the option of creating a top mold piece that allows PGA key pins only where designated. However, sockets that populate all 16 key pins must be allowed, so the motherboard must always provide for pins at all key pin locations.

NC Pins

The motherboard should provide a plated hole for an NC pin. The pin hole should not be electrically connected to anything.

NMI Pin

NMI is an input from the system that causes a non-maskable interrupt.

PGA Orientation Pins

No pin is present at pin locations A1 and AN1. Motherboard designers should not allow for a PGA socket pin at these locations.

For more information, see the *Socket A Motherboard Design Guide for Desktop and Mobile Systems*, order# 24363.

PLL Bypass and Test Pins

PLLTEST# (AC3), PLLBYPASS# (AJ25), PLLMON1 (AN13), PLLMON2 (AL13), PLLBYPASSCLK (AN15), and PLLBYPASSCLK# (AL15) are the PLL bypass and test interface. This interface is tied disabled on the motherboard.

All six pin signals are routed to the debug connector. All four processor inputs (PLLTEST#, PLLBYPASS#, PLLMON1, and PLLMON2) are tied to VCC_CORE with pullup resistors.

PWROK Pin

The PWROK input to the processor must not be asserted until all voltage planes in the system are within specification and all system clocks are running within specification.

For more information, See “Signal and Power-Up Requirements” on page 37.

SADDIN[1:0]# and SADDOUT[1:0]# Pins

The AMD Athlon MP processor model 6 does not support SADDIN[1:0]# or SADDOUT[1:0]#. SADDIN[1]# is tied to VCC with pullup resistors, if this bit is not supported by the Northbridge (future models can support SADDIN[1]#). SADDOUT[1:0]# are tied to VCC with pullup resistors if these pins are supported by the Northbridge. For more information, see the *AMD Athlon™ and AMD Duron™ System Bus Specification*, order# 21902.

Scan Pins

SCANSHIFTEN (Q5), SCANCLK1 (S1), SCANINTEVAL (S3), and SCANCLK2 (S5) are the scan interface. This interface is AMD internal and is tied disabled with pulldown resistors to ground on the motherboard.

SCHECK[7:0]# Pin

For systems that do not support ECC, SCHECK[7:0]# should be treated as NC pins.

SMI# Pin

SMI# is an input that causes the processor to enter the system management mode.

STPCLK# Pin

STPCLK# is an input that causes the processor to enter a lower power mode and issue a Stop Grant special cycle.

SYSCLK and SYSCLK#

SYSCLK and SYSCLK# are differential input clock signals provided to the processor’s PLL from a system-clock generator.

See “CLKIN, RSTCLK (SYSCLK) Pins” on page 60 for more information.

THDA and THDC Pins

Thermal Diode anode and cathode pins are used to monitor the actual temperature of the processor die, providing more accurate temperature control to the system.

VCCA Pin

VCCA is the processor PLL supply. For information about the VCCA pin, see Table 5, “VCCA AC and DC Characteristics,” on page 25 and the AMD Athlon™ Processor Based Motherboard Design Guide, order# 24363.

VID[4:0] Pins

The VID[4:0] (Voltage Identification) outputs are used to dictate the VCC_CORE voltage level. The VID[4:0] pins are strapped to ground or left unconnected on the processor’s package. The VID[4:0] pins are pulled-up on the motherboard and used by the VCC_CORE DC/DC converter.

Table 20. VID[4:0] Code to Voltage Definition

VID[4:0]	VCC_CORE(V)	VID[4:0]	VCC_CORE (V)
00000	1.850	10000	1.450
00001	1.825	10001	1.425
00010	1.800	10010	1.400
00011	1.775	10011	1.375
00100	1.750	10100	1.350
00101	1.725	10101	1.325
00111	1.675	10111	1.275
01000	1.650	11000	1.250
01001	1.625	11001	1.225
01010	1.600	11010	1.200
01011	1.575	11011	1.175
01100	1.550	11100	1.150
01101	1.525	11101	1.125
01110	1.500	11110	1.100
01111	1.475	11111	No CPU

For more information, see the “Required Circuits” chapter of the *AMD Athlon™ Processor Based Motherboard Design Guide*, order# 24363.

VREFSYS Pin

VREFSYS (W5) drives the threshold voltage for the system bus input receivers. The value of VREFSYS is system specific. In addition, to minimize VCC_CORE noise rejection from VREFSYS, include decoupling capacitors. For more information, see the *Socket A Motherboard Design Guide*, order# 24363.

ZN and ZP Pins

ZN (AC5), and ZP (AE5), are the push-pull compensation circuit pins. In Push-Pull mode (selected by the SIP parameter SysPushPull asserted), ZN is tied to VCC_CORE with a resistor that has a resistance matching the impedance Z_0 of the transmission line. ZP is tied to VSS with a resistor that has a resistance matching the impedance Z_0 of the transmission line.

11 Ordering Information

Standard AMD Athlon™ MP Processor Model 6 Products

AMD standard products are available in several operating ranges. The ordering part numbers (OPN) are formed by a combination of the elements, as shown in Figure 14.

OPN

A HX 1200 A M S 3 C

- **Max FSB:** C=266 MHz
- **Size of L2 Cache:** 3 =256 Kbytes
- **Case Temperature:** S=95°C
- **Operating Voltage:** M = 1.75 V
- **Package Type:** A = PGA
- **Speed:** 1000=1000 MHz, 1200=1200 MHz, etc.
- **Generation:** HX = High-Performance Processor for Multiprocessing Systems
- **Family/Architecture:** A = AMD Athlon Processor Architecture

Note: Spaces are added to the number shown above for viewing clarity only.

Figure 14. OPN Example for the AMD Athlon™ MP Processor Model 6

Appendix A

Conventions and Abbreviations

This section contains information about the conventions and abbreviations used in this document.

Signals and Bits

- Active-Low Signals—Signal names containing a pound sign, such as SFILL#, indicate active-Low signals. They are asserted in their Low-voltage state and negated in their High-voltage state. When used in this context, High and Low are written with an initial upper case letter.
- Signal Ranges—In a range of signals, the highest and lowest signal numbers are contained in brackets and separated by a colon (for example, D[63:0]).
- Reserved Bits and Signals—Signals or bus bits marked *reserved* must be driven inactive or left unconnected, as indicated in the signal descriptions. These bits and signals are reserved by AMD for future implementations. When software reads registers with reserved bits, the reserved bits must be masked. When software writes such registers, it must first read the register and change only the non-reserved bits before writing back to the register.
- Three-State—In timing diagrams, signal ranges that are high impedance are shown as a straight horizontal line half-way between the high and low levels.

- Invalid and Don't-Care—In timing diagrams, signal ranges that are invalid or don't-care are filled with a screen pattern.

Data Terminology

The following list defines data terminology:

- Quantities
  - A *word* is two bytes (16 bits)
  - A *doubleword* is four bytes (32 bits)
  - A *quadword* is eight bytes (64 bits)
- Addressing—Memory is addressed as a series of bytes on eight-byte (64-bit) boundaries in which each byte can be separately enabled.
- Abbreviations—The following notation is used for bits and bytes:
  - Kilo (K, as in 4-Kbyte page)
  - Mega (M, as in 4 Mbits/sec)
  - Giga (G, as in 4 Gbytes of memory space)

  See Table 21 on page 71 for more abbreviations.
- Little-Endian Convention—The byte with the address xx...xx00 is in the least-significant byte position (little end). In byte diagrams, bit positions are numbered from right to left—the little end is on the right and the big end is on the left. Data structure diagrams in memory show low addresses at the bottom and high addresses at the top. When data items are aligned, bit notation on a 64-bit data bus maps directly to bit notation in 64-bit-wide memory. Because byte addresses increase from right to left, strings appear in reverse order when illustrated.
- Bit Ranges—In text, bit ranges are shown with a dash (for example, bits 9–1). When accompanied by a signal or bus name, the highest and lowest bit numbers are contained in brackets and separated by a colon (for example, AD[31:0]).
- Bit Values—Bits can either be set to 1 or cleared to 0.
- Hexadecimal and Binary Numbers—Unless the context makes interpretation clear, hexadecimal numbers are followed by an h and binary numbers are followed by a b.

Abbreviations and Acronyms

Table 21 contains the definitions of abbreviations used in this document.

Table 21. Abbreviations

Abbreviation	Meaning
A	Ampere
F	Farad
G	Giga-
Gbit	Gigabit
Gbyte	Gigabyte
GHz	Gigahertz
H	Henry
h	Hexadecimal
K	Kilo-
Kbyte	Kilobyte
lbf	Foot-pound
M	Mega-
Mbit	Megabit
Mbyte	Megabyte
MHz	Megahertz
m	Milli-
ms	Millisecond
mW	Milliwatt
µ	Micro-
µA	Microampere
µF	Microfarad
µH	Microhenry
µs	Microsecond
µV	Microvolt
n	nano-
nA	nanoampere
nF	nanofarad
nH	nanohenry
ns	nanosecond
ohm	Ohm

Table 21. Abbreviations (Continued)

Abbreviation	Meaning
p	pico-
pA	picoampere
pF	picofarad
pH	picohenry
ps	picosecond
s	Second
V	Volt
W	Watt

Table 22 contains the definitions of acronyms used in this document.

Table 22. Acronyms

Abbreviation	Meaning
ACPI	Advanced Configuration and Power Interface
AGP	Accelerated Graphics Port
APCI	AGP Peripheral Component Interconnect
API	Application Programming Interface
APIC	Advanced Programmable Interrupt Controller
BIOS	Basic Input/Output System
BIST	Built-In Self-Test
BIU	Bus Interface Unit
DDR	Double-Data Rate
DIMM	Dual Inline Memory Module
DMA	Direct Memory Access
DRAM	Direct Random Access Memory
ECC	Error Correcting Code
EIDE	Enhanced Integrated Device Electronics
EISA	Extended Industry Standard Architecture
EPROM	Enhanced Programmable Read Only Memory
EV6	Digital™ Alpha™ Bus
FIFO	First In, First Out
GART	Graphics Address Remapping Table
HSTL	High-Speed Transistor Logic

Table 22. Acronyms (Continued)

Abbreviation	Meaning
IDE	Integrated Device Electronics
ISA	Industry Standard Architecture
JEDEC	Joint Electron Device Engineering Council
JTAG	Joint Test Action Group
LAN	Large Area Network
LRU	Least-Recently Used
LVTTL	Low Voltage Transistor Transistor Logic
MSB	Most Significant Bit
MTRR	Memory Type and Range Registers
MUX	Multiplexer
NMI	Non-Maskable Interrupt
OD	Open-Drain
PBGA	Plastic Ball Grid Array
PA	Physical Address
PCI	Peripheral Component Interconnect
PDE	Page Directory Entry
PDT	Page Directory Table
PLL	Phase Locked Loop
PMSM	Power Management State Machine
POS	Power-On Suspend
POST	Power-On Self-Test
RAM	Random Access Memory
ROM	Read Only Memory
RXA	Read Acknowledge Queue
SCSI	Small Computer System Interface
SDI	System DRAM Interface
SDRAM	Synchronous Direct Random Access Memory
SIMD	Single Instruction Multiple Data
SIP	Serial Initialization Packet
SMbus	System Management Bus
SPD	Serial Presence Detect
SRAM	Synchronous Random Access Memory
SROM	Serial Read Only Memory
TLB	Translation Lookaside Buffer

Table 22. Acronyms (Continued)

Abbreviation	Meaning
TOM	Top of Memory
TTL	Transistor Transistor Logic
VAS	Virtual Address Space
VPA	Virtual Page Address
VGA	Video Graphics Adapter
USB	Universal Serial Bus
ZDB	Zero Delay Buffer