VLSI TECHNOLOGY, INC.

VY86C060 DESIGN PARAMETERS

32-BIT SINGLE-CHIP MICROPROCESSOR

FEATURES

- Fully static operation
- 32-bit data bus
- 32-bit address bus
- Coprocessor interface for instruction set extension
- High-level language compiler support
- Fast interrupt response for real-time applications
- Big and Little Endian operating modes
- Boundary Scan for device and system testing
- Low power consumption

Note:
Additional information regarding the VY86C060 can be found in the VLSI document: "VY86C060 Architectural Overview".

DESCRIPTION

The VY86C060 microprocessor is based on the ARM™ processor core from Advanced RISC Machines, Ltd. The VY86C060 is a general-purpose 32-bit, single-chip microprocessor. The architecture is based on Reduced Instruction Set Computer (RISC) principles, and the instruction set and related decode mechanism are greatly simplified compared with microprogrammed Complex Instruction Set Computers (CISC). This simplification results in a high-instruction throughput and a real-time interrupt response from a small and cost-effective chip.

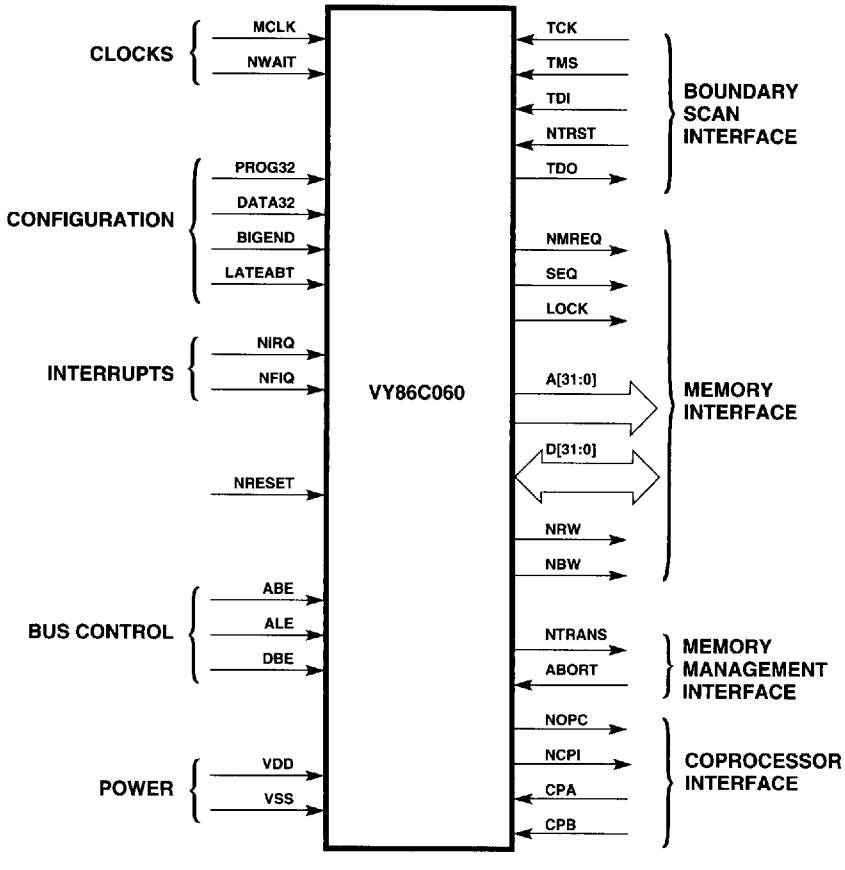
The instruction set comprises ten basic instruction types. Two of these make use of the on-chip arithmetic logic unit (ALU), barrel shifter and multiplier to perform high-speed operations on the data in a bank of 32-bit registers. Three instruction types control the transfer of data between main memory and the register bank. One is optimized for flexibility of addressing, another for rapid context switching, and the third for indivisible semaphore operations. Two instructions control the flow and privilege level of execution, and the remaining three types are dedicated to the control of external coprocessors, which allow the functionality of the instruction set to be extended off-chip in an open and uniform way.

The VY86C060 instruction set has proved to be a good target for compilers of many different high-level languages. Where required for critical code segments, assembly code programming is also straightforward, unlike some RISC processors that depend on sophisticated compiler technology to manage complicated instruction interdependencies.

Pipelining is employed allowing for all parts of the processing and memory systems to operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

The VY86C060 is based on the VY86C006 FSB™ library element, and is software compatible with the instruction set of earlier ARM processors (ARM2, ARM2aS, and ARM3). Unlike these processors, which have a 26-bit address bus, the VY86C060 has a 32-bit address bus. For backwards compatibility, it can also be configured to use a 26-bit address bus. It is a fully static implementation that allows the clock to be stopped in any part of the cycle with minimal residual power consumption and no loss of state.

FUNCTIONAL DIAGRAM

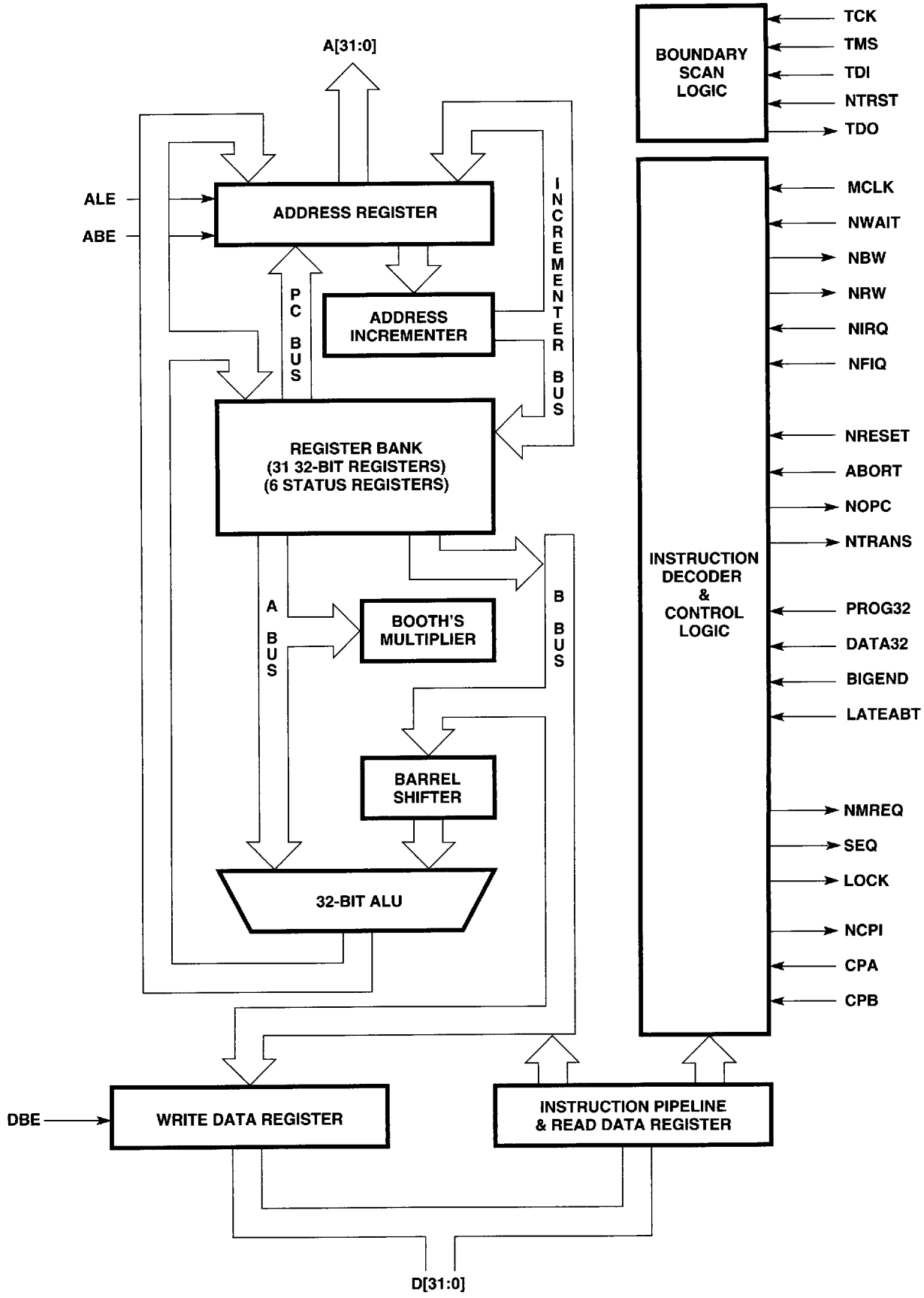


ORDER INFORMATION

Part Number	Description	Pkg.
VY86C06020FC-2	20-MHz RISC MPU 32-Bit Data/ Address Bus	100-Pin MQFP
VY86C060A	33-MHz RISC MPU 32-Bit Data/ Address Bus	144-Pin TQFP
VY86C06040	40-MHz RISC MPU 32-Bit Data/ Address Bus	100-Pin TQFP

VLSI Technology, Inc. • 1109 McKay Drive • San Jose, CA 95131 • 408-434-3100

BLOCK DIAGRAM



SIGNAL DESCRIPTIONS

Name	Type	Description
A[31:0]	OS8	Address Bus. If ALE is HIGH, the addresses become valid during phase 2 of the cycle before the one to which they refer and remain so during phase 1 of the referenced cycle. Their stable period may be controlled by ALE as described below.
ABE	I	Address bus enable. When this input is LOW, the address bus drivers (A[31:0]) are put into a high impedance state.
ABORT	I	Memory abort. This input allows the memory system to tell the processor that a requested access is not allowed. For ARM6x, the signal must be valid before the end of phase 1 of the cycle during which the memory transfer is attempted. On ARM7x and beyond, this signal must be valid before the end of phase 2.
ALE	I	Address latch enable. This input to the processor is used to control transparent latches on the address outputs. Normally the addresses change during phase 2 to the value required during the next cycle, but for direct interfacing to ROMs they are required to be stable to the end of phase 2. Taking ALE LOW until the end of phase 2 will ensure that this happens. If the system does not require address lines to be held in this way, ALE may be held permanently HIGH. The ALE latch is static, so ALE may be held LOW indefinitely.
BIGEND	I	Big Endian configuration. When this signal is HIGH, the processor treats words in memory as being in Big Endian format. When it is LOW, words in memory are treated as Little Endian.
CPA[1]	I	Coprocessor absent. A coprocessor which is capable of performing the operation that is requested, should take CPA LOW immediately. If CPA is high and NCPI is low at the rising edge of phase 2, then the VY86C060 will abort the coprocessor handshake, and take the undefined instruction trap. If CPA is LOW, the VY86C060 will busy-wait until CPB is LOW, and then complete the coprocessor instruction. If no coprocessors are fitted, CPA must be driven high.
CPB[2]	I	Coprocessor busy. A coprocessor which is capable of performing the operation that is requested, but cannot commit to starting it immediately, should indicate this by driving CPB HIGH. When the coprocessor is ready to start, it should drive CPB LOW. The VY86C060 samples CPB on the rising edge of phase 2 whenever NCPI is low. If no coprocessors are fitted, CPB must be driven HIGH.
D[31:0]	I/OS8	Data bus. These are bidirectional signal paths which are used for data transfers between the processor and external memory. During read cycles (when NRW is LOW), the input data must be valid before the end of phase 2 of the transfer cycle. During write cycles (when NRW is HIGH), the output data will become valid during phase 1 and remain valid throughout phase 2 of the transfer cycle.
DATA32	I	32-bit Data configuration. When this signal is HIGH, the processor can access data in a 32-bit address space using address lines A[31:0]. When it is LOW the processor can access data from a 26-bit address space using A[25:0]. In this latter configuration the address lines A[31:26] are not used. Before changing DATA32, ensure that the processor is not about to access an address greater than &3FFFFFF in the next cycle.
DBE	I	Data bus enable. When this input is LOW, the data bus drivers (D[31:0]) are put into a high impedance state. The drivers will always be high impedance except during write operations, and DBE may be tied HIGH in systems that do not require the data bus for DMA or similar activities.
LATEABT[3]	I	Late Abort. This signal controls the action of the processor on an ABORT exception. When it is HIGH (Late Abort), the modified base register of an aborted LDR, LDM, STR, or STM instruction is written back. This signal has no effect on when the ABORT signal is sampled. It is recommended that the Late Abort scheme be used where possible as only this scheme is used in ARM7x processors and beyond. However, ARM2, ARM2aS, and ARM3 support the Early Abort mechanism.
LOCK	OS8	Locked operation. When LOCK is HIGH, the processor is performing a "locked" memory access and the memory controller should wait until LOCK goes LOW before allowing another device to access the memory. LOCK changes during phase 2, and remains HIGH for the duration of the locked memory accesses. It is active only during the data swap instruction.
MCLK	I	Memory clock input. This clock times all memory accesses. The LOW (phase 1) or HIGH (phase 2) periods of MCLK may be stretched indefinitely when accessing slow peripherals; alternately, the NWAIT input may be used with a free-running MCLK to achieve the same effect.

Notes:

1. CPA must default HIGH when coprocessor cycles are not executed in order to enter the Undefined Instruction Exception.
2. CPB must default HIGH when coprocessor cycles are not executed in order to enter the Undefined Instruction Exception.
3. This pin only exists on the ARM6x processors, ARM7x processors and beyond are always configured for late abort.

SIGNAL DESCRIPTIONS (Cont.)

Name	Type	Description
NBW	OS8	NOT byte/word. This is an output signal used by the processor to indicate to the external memory system when a data transfer of a byte length is required. The signal is HIGH for word transfers and LOW for byte transfers and is valid for both read and write cycles. The signal will become valid during phase 2 of the cycle before the one during which the transfer will take place. It will remain stable throughout phase 1 of the transfer cycle.
NCPI	O4	NOT coprocessor instruction. When the VY86C060 executes a coprocessor instruction, it will take this output LOW. The action taken will depend on the CPA and CPB inputs.
NFIQ	I	NOT fast interrupt request. Same as NIRQ, but with higher priority. May be taken LOW asynchronously to interrupt the processor when the appropriate enable is active.
NIRQ	I	NOT interrupt request. An asynchronous interrupt request to the processor which causes it to be interrupted if taken LOW when the appropriate enable in the processor is active. The signal is level-sensitive and must be held LOW until a suitable response is received from the processor.
NMREQ	O4	NOT memory request. This signal, when LOW, indicates that the processor requires memory access during the following cycle. The signal becomes valid during phase 1, remaining valid through phase 2 of the cycle preceding that to which it refers.
NOPC	O4	NOT op-code fetch. When LOW, this signal indicates that the processor is fetching an instruction from memory. When HIGH, data is either being transferred or the VY86C060 is performing an internal cycle. The signal becomes valid during phase 2 of the previous cycle, remaining valid through phase 1 of the referenced cycle.
NRESET	I	NOT reset. This is a level-sensitive input signal that is used to start the processor from a known address. A LOW level will cause the instruction being executed to terminate abnormally. When NRESET becomes HIGH for at least one clock cycle, the processor will restart from address 0. NRESET must remain LOW (and NWAIT must remain HIGH) for at least two clock cycles. During the LOW period, the processor will perform dummy instruction fetches with the address incrementing from the point where reset was activated. The address value will overflow to zero if NRESET is held beyond the maximum address limit.
NRW	OS8	NOT read/write. When HIGH this signal indicates a processor write cycle; when LOW, a read cycle. It becomes valid during phase 2 of the cycle prior to the referenced cycle, and remains valid to the end of phase 1 of the referenced cycle.
NTRANS	OS8	NOT memory translate. When this signal is LOW, it indicates that the processor is in user mode. It may be used to tell memory management hardware when translation of the addresses should be turned on, or as an indicator of non-user mode activity.
NTRST	IP	NOT Test Reset. Active-low reset signal for the boundary scan logic. This input has an on-chip pull-up resistor to VDD. The timing of this and the following four boundary-scan signals are described in more detail later in this document.
NWAIT	I	NOT wait. When accessing slow peripherals, the VY86C060 can be made to wait for an integer number of MCLK cycles by driving NWAIT LOW. Internally, NWAIT is ANDed with the MCLK clock, and must only change when MCLK is LOW. If NWAIT is not used in a system, it may be tied HIGH.
PROG32	I	32-bit Program configuration. When this signal is HIGH, the processor can fetch instructions from a 32-bit address space using address lines A[31:0]. When it is LOW the processor fetches instructions from a 26-bit address space using A[25:0]. In this latter configuration the address lines A[31:26] are not used for instruction fetches. Before changing PROG32, ensure that the processor is in a 26-bit mode, and is not about to write to an address in the range 0 to &1F (inclusive) in the next cycle.
SEQ	O4	Sequential address. Will become HIGH when the address of the next memory cycle will be related to that of the last memory access. The new address will either be the same as, or four greater than the old one. The signal becomes valid during phase 1 and remains so through phase 2 of the cycle preceding that to which it refers. It may be used in combination with the low-order address lines to indicate that the next cycle can use a fast memory mode (for example DRAM page mode) and/or to bypass the address translation system.

SIGNAL DESCRIPTIONS (Cont.)

Name	Type	Description
TCK	IP	Test Clock. This input to the boundary-scan logic has an on-chip pull-up resistor to VDD.
TDI	IP	Test Data Input. This input to the boundary-scan logic has an on-chip pull-up resistor to VDD.
TDO	OS8	Test Data Output. Output from the boundary-scan logic.
TMS	IP	Test Mode Select. This input to the boundary-scan logic has an on-chip pull-up resistor to VDD.
VDD	P	Positive supply.
VSS	P	Supply ground.

Key to Signal Types

I	Input (TTL threshold)
IP	Input (TTL threshold) with pull-up resistor
O4	Output (4 mA drive) for VY86C06020FC-2/VY86C06040 and (8 mA drive) for VY86C060A
OS8	Output (8 mA slew-limited drive)
P	Power supply

AC PARAMETERS

The AC timing diagrams presented in this section assume that the outputs of the VY86C060 have been loaded with the capacitive loads shown in the 'Test Load' column of the table shown below.

The output drivers of the VY86C060 exhibit a propagation delay that increases linearly with the increase in load capacitance. A worst-case 'Output derating' figure is given for each output driver, showing the approximate rate of increase of output time with increasing loads.

AC TEST LOADS

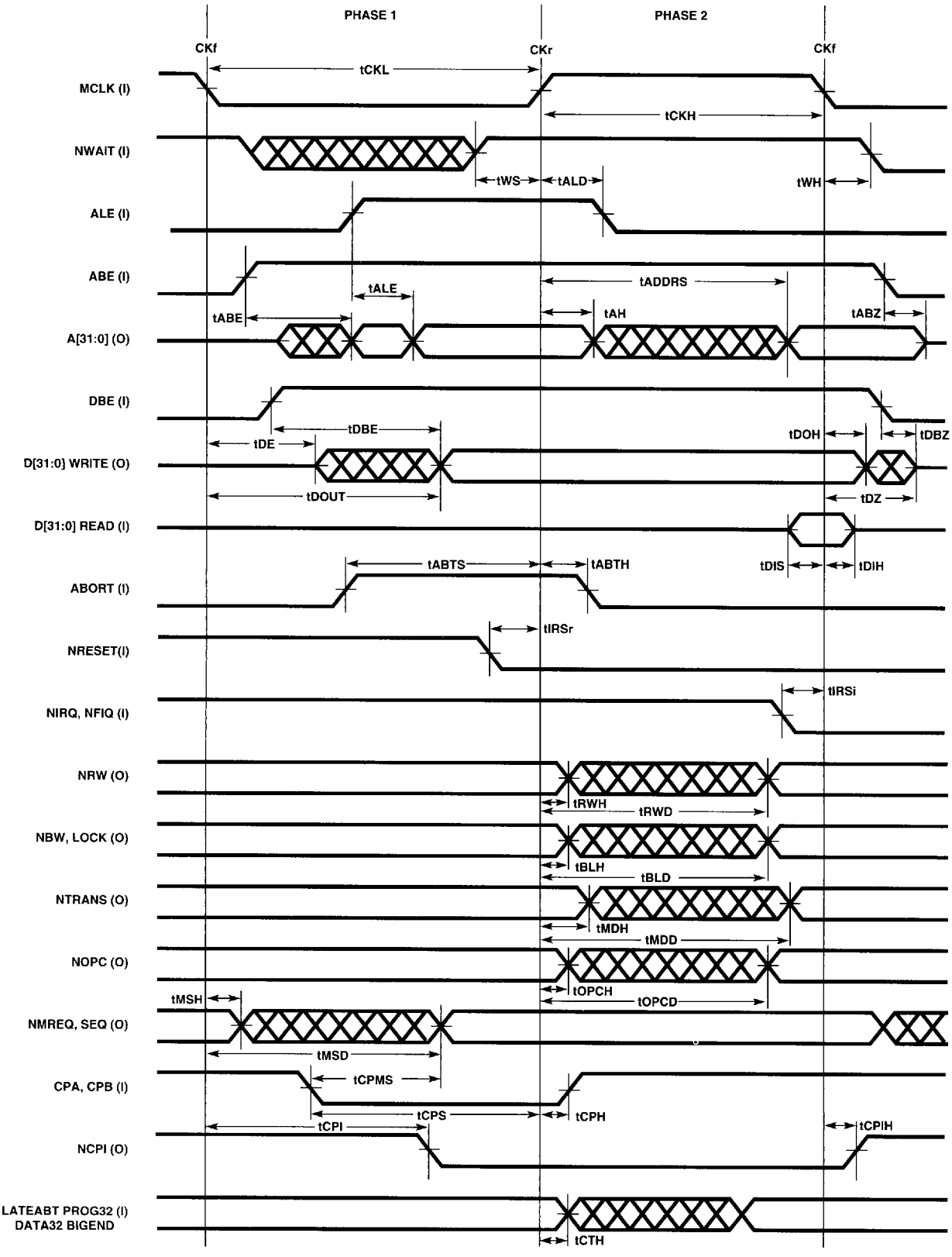
Output Signal	Test Load (pF)	VY86C06020FC-2 Output Derating (ns/pF)	VY86C060A Output Derating (ns/pF)	VY86C06040 Output Derating (ns/pF)
D[31:0]	50	.072	0.05	.069
A[31:0]	50	.072	0.05	.069
LOCK	25	.072	0.05	.069
NCPI	25	.093	0.05	.092
NMREQ	25	.093	0.05	.092
SEQ	25	.093	0.05	.092
NRW	25	.072	0.05	.069
NBW	25	.072	0.05	.069
NOPC	25	.093	0.05	.092
NTRANS	25	.072	0.05	.069
TDO	25	.072	0.05	.069

AC PARAMETERS

Symbol	Parameter	I/O	VY86C06020FC-2		VY86C060A		VY86C06040[2]		Units	Notes
			Min	Max	Min	Max	Min	Max		
tCKL	Clock low time	I	25.0		15.0		12.2		ns	
tCKH	Clock high time	I	25.0		15.0		11.6		ns	
tWS	NWAIT setup to CKr	I	1.0		1.0		0.0		ns	
tWH	NWAIT hold from CKf	I	2.0		2.0		0.0		ns	
tALD	CKr to address latch	I		1.5		1.5		3.4	ns	
tABE	Address bus enable	I		21.0		14.0		9.1	ns	
tALE	Address latch open	I		14.0		6.0		10.5	ns	
tAH	Address hold time	O	2.0		2.0		2.0		ns	
tADDRS	CKr to address valid	O		23.0		14.5		13.8	ns	
tABZ	Address bus disable	I		14.0		8.5		6.2	ns	
tDE	CKf to data enable	O	11.0		7.0		5.9		ns	
tDBE	Data bus enable	I		19.0		8.0		11.9	ns	
tDOUT	Data out delay	O		29.0		17.0		15.3	ns	
tDOH	Data out hold time	O	3.0		3.0		3.0		ns	
tDBZ	Data bus disable	O		21.0		12.0		9.3	ns	
tDZ	CKf to data disable	O		24.0		15.0		12.1	ns	
tDIS	Data in setup time	I	2.0		1.0		0.0		ns	
tDIH	Data in hold time	I	7.5		5.0		3.0		ns	
tABTS	Abort setup time	I	10.0		6.5		4.4		ns	
tABTH	Abort hold time	I	8.0		5.5		2.4		ns	
tIRSr	NRESET setup time	I	3.0		3.0		0		ns	1
tIRSi	NIRQ & NFIQ setup time	I	3.0		1.0		0		ns	1
tRWH	NRW hold time	O	2.0		2.0		2.0		ns	
tRWD	CKr to NBW valid	O		23.0		14.0		11.8	ns	
tBLH	NBW & Lock hold time	O	2.0		2.0		2.0		ns	
tBLD	CKr to NBW & LOCK	O		21.0		14.0		13.3	ns	
tMDH	NTRANS hold time	O	2.0		2.0		2.0		ns	
tMDD	CKr TO NTRANS	O		21.0		14.0		13.2	ns	
tOPCH	NOPC hold time	O	2.0		1.5		2.0		ns	
tOPCD	CKr TO NOPC valid	O		18.0		11.5		10.5	ns	
tMSH	NMREQ & SEQ hold time	O	2.0		2.0		2.0		ns	
tMSD	CKf to NMREQ & SEQ	O		25.0		14.5		11.6	ns	
tCPMS	CPA, CPB to NMREQ, SEQ	I		10.0		6.50		10.0	ns	
tCPS	CPA, CPB setup time	I	14.0		7.5		2.7		ns	
tCPH	CPA, CPB hold time	I	5.0		3.5		2.5		ns	
tCPI	CKf to NCPI delay	O		19.0		12.5		12.1	ns	
tCPIH	NCPI hold time	O	2.0		2.0		2.0		ns	
tCTH	Config hold time	I	4.0		2.5		5.2		ns	

Notes:
All figures assume that the VY86C060 is operated exclusively in 32-bit modes (User32, FIQ32, IRQ32, Supervisor32, Abort32 and Undefined32).
1. TIRS guarantees recognition of the interrupt (or reset) source by the corresponding clock edge. The interrupt and reset inputs may be applied fully asynchronously where the exact cycle of recognition is unimportant.
2. Preliminary timing values are provided based on worst-case simulations.

AC TIMING DIAGRAM



I - INPUT
O - OUTPUT

DC PARAMETERS

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only. Exceeding the absolute maximum ratings may permanently damage the device. Operating the device at absolute maximum ratings for extended periods may affect device reliability. Functional operation of the device at these or any other condition outside those specified is not implied.

		VY86C06020FC-2		VY86C060A		VY86C06040			
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Units	Note
VDD	Supply voltage	-0.5	6.0	-0.5	6.0	-0.5	6.0	V	
VIP	Voltage applied to input pin	-0.5	VDD +0.5	-0.5	VDD +0.5	-0.5	VDD +0.5	V	
TS	Storage temperature	-65	+150	-65	+150	-65	+150	°C	
TA	Ambient operating temperature	-10	+80	-10	+80	-10	+80	°C	
mA/MHz	Current/Frequency		3.6		3.2		2.6	mA/ MHz	

RECOMMENDED DC OPERATING CONDITIONS

		VY86C06020FC-2		VY86C060A		VY86C06040			
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Units	Note
VDD	Supply voltage	4.5	5.5	4.5	5.5	4.5	5.5	V	
VIH	Input HIGH voltage	0.7 x VDD	VDD +0.5	0.7 x VDD	VDD +0.5	0.7 x VDD	VDD +0.5	V	1
VIL	Input LOW voltage	-0.5	0.8	-0.5	0.8	-0.5	0.8	V	1
IO4	Output current (O4 outputs)		±4		±4		±4	mA	
IO8	Output current (OS8 outputs)		±8		±8		±8	mA	
TA	Ambient operating temperature	0	+70	0	+70	0	+70	°C	

DC CHARACTERISTICS, VDD = 5.0 V ± 5%, TA = 0 to +70 °C

		VY86C06020FC-2		VY86C060A		VY86C06040			
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Units	Note
IDD	Supply current		350		50		50	µA	
ILATCH	D.C. latch-up current at 125°C		100		100		100	mA	2
IIN	'I' input leakage current		±10		±10		±10	µA	
VOL	Output LOW voltage		0.4		0.4		0.4	V	
VOH	Output HIGH voltage	2.4		2.4		2.4		V	
RP	'IP' input pullup resistor	35k	150k	35k	100k	51k	124k	W	
CIN	Input capacitance		5		5		5	pF	

Notes:

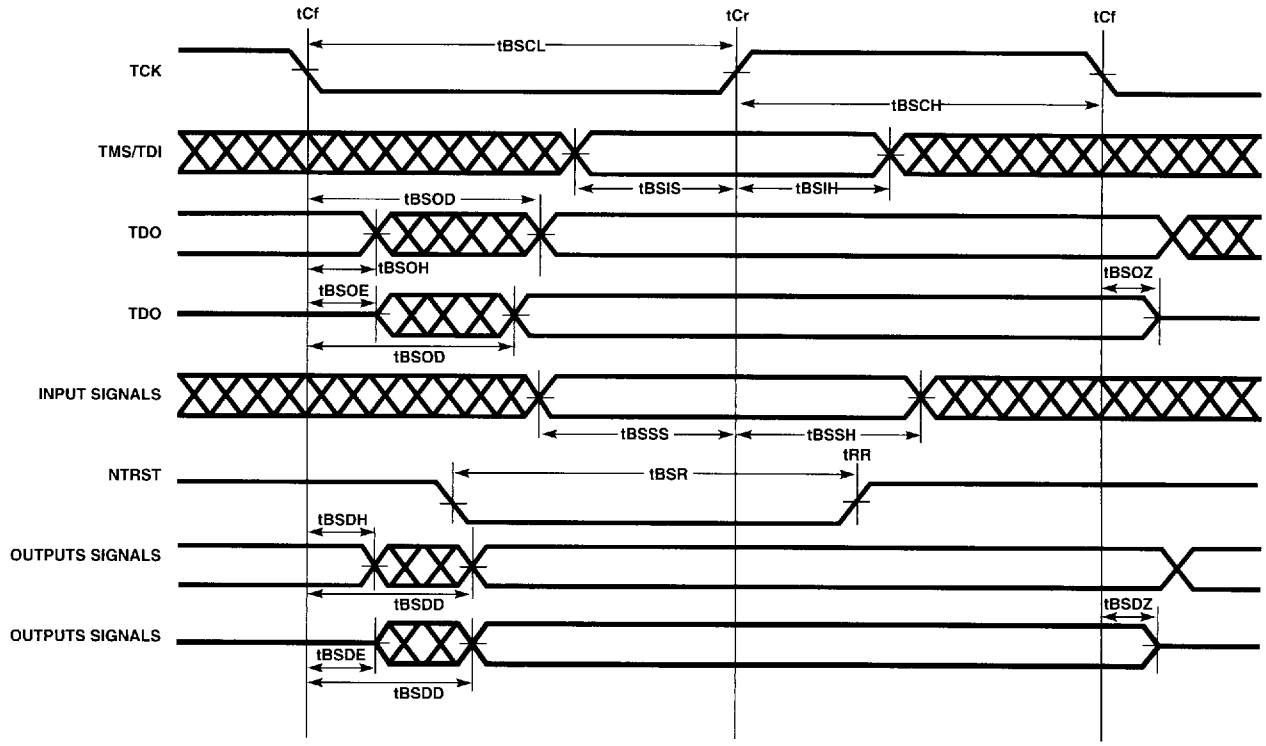
The device contains circuitry designed to provide protection from damage by static discharge. It is recommended that precautions be taken to avoid applying voltages outside the specified range.

All voltages are measured with respect to VSS.

1. All inputs are TTL compatible.
2. Latch-up testing using JEDEC test procedure Draft 3.2

BOUNDARY SCAN

TIMING DIAGRAM



AC PARAMETERS

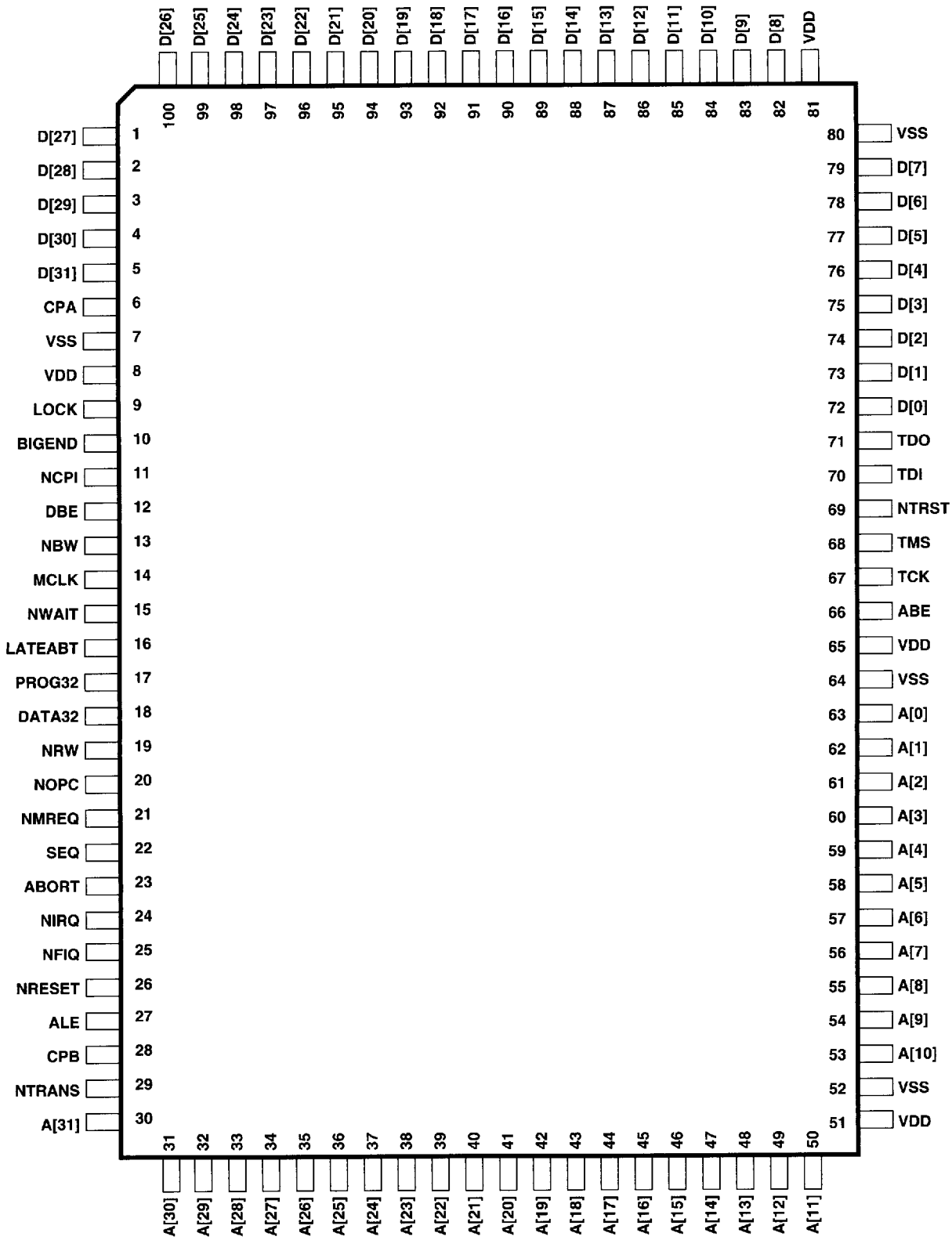
Symbol	Parameter	I/O	VY86C06020FC-2		VY86C060A		VY86C06040		Units	Notes
			Min	Max	Min	Max	Min	Max		
tBSOD	TCf to TDO valid	O		32.0		19.0		15.1	ns	
tBSDD	Data output disable time	O		40.0		25.0		15.3	ns	
tBSIS	TDI, TMS setup to TCr	I	5.0		3.0		0.0		ns	3
tBSSS	Signal setup to TCr	I	2.0		1.0		3.0		ns	2
tBSCL	TCK low period	I	25.0		15.0		10.9		ns	1
tBSCH	TCK high period	I	25.0		15.0		10.8		ns	1
tBSOE	TDO enable time	O	6.0		4.0		3.3		ns	
tBSOZ	TDO disable time	O		24.0		19.0		7.5	ns	
tBSDE	Data output enable time	O	15.0		9.0		4.8		ns	
tBSOH	TDO hold time	O	5.0		2.0		1.8		ns	
tBSDH	Data output hold time	O	6.0		2.0		3.30		ns	2
tBSIH	TDI, TMS hold time	I	5.0		3.00		.6		ns	3
tBSR	Reset period	I	18.0		16.0		4.5		ns	
tBSDZ	Data output disable time	O		36.0		25.0		14.0	ns	
tBSSH	Input Signal hold time	I	2.0		2.0		5.3		ns	

Notes:

1. TCK may be stopped indefinitely in either the low or high phase.
2. For correct data latching, the I/O signals (from the core and the pads) must be setup and held with respect to the rising edge of TCK in the CAPTURE-DR state of the SAMPLE/PRELOAD, INTEST and EXTEST instructions.
3. The TMS input must be held high as NTRST is taken high at the end of the boundary scan reset sequence.

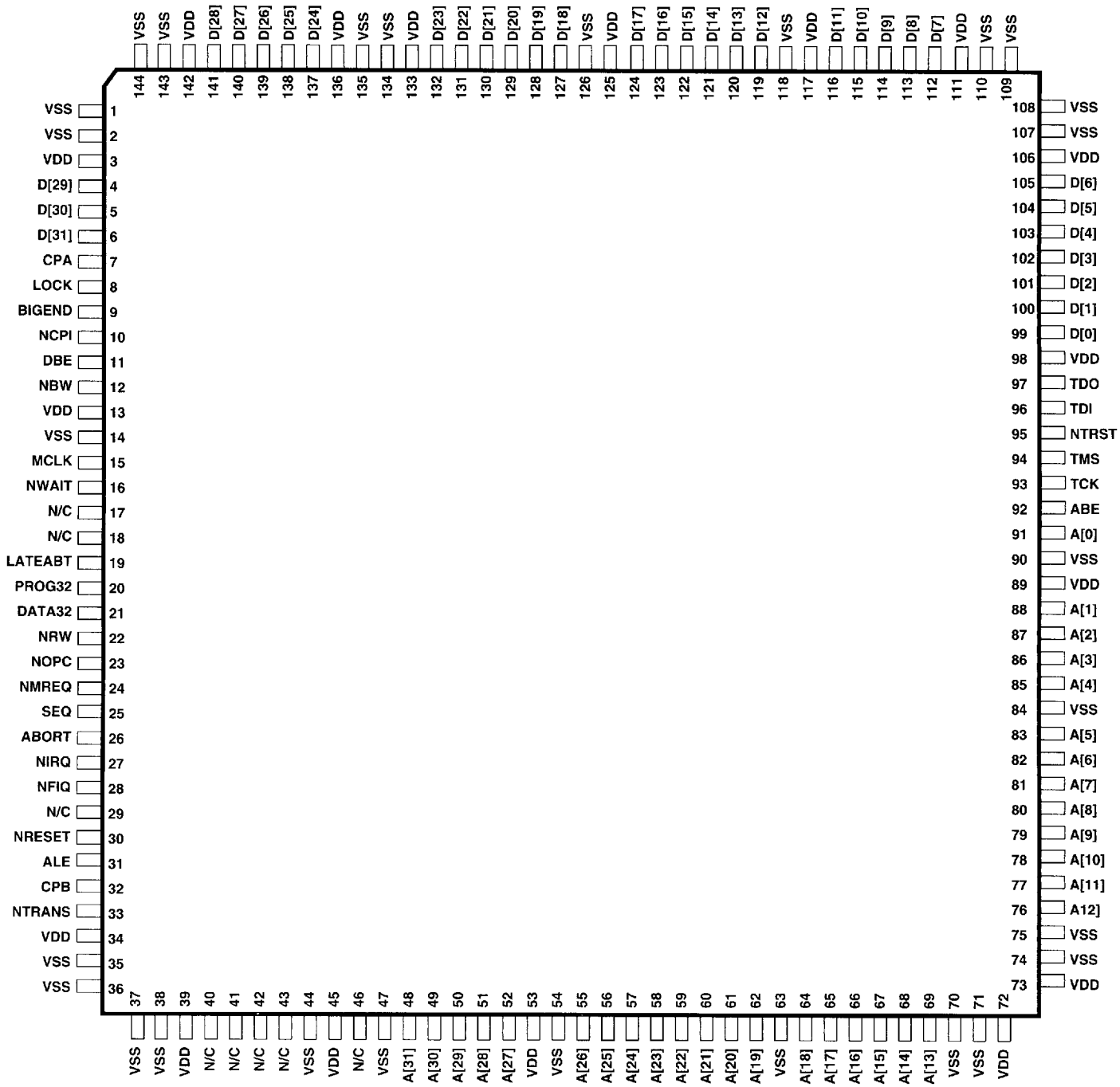
VY86C06020FC-2 PIN DIAGRAM

100-PIN MQFP



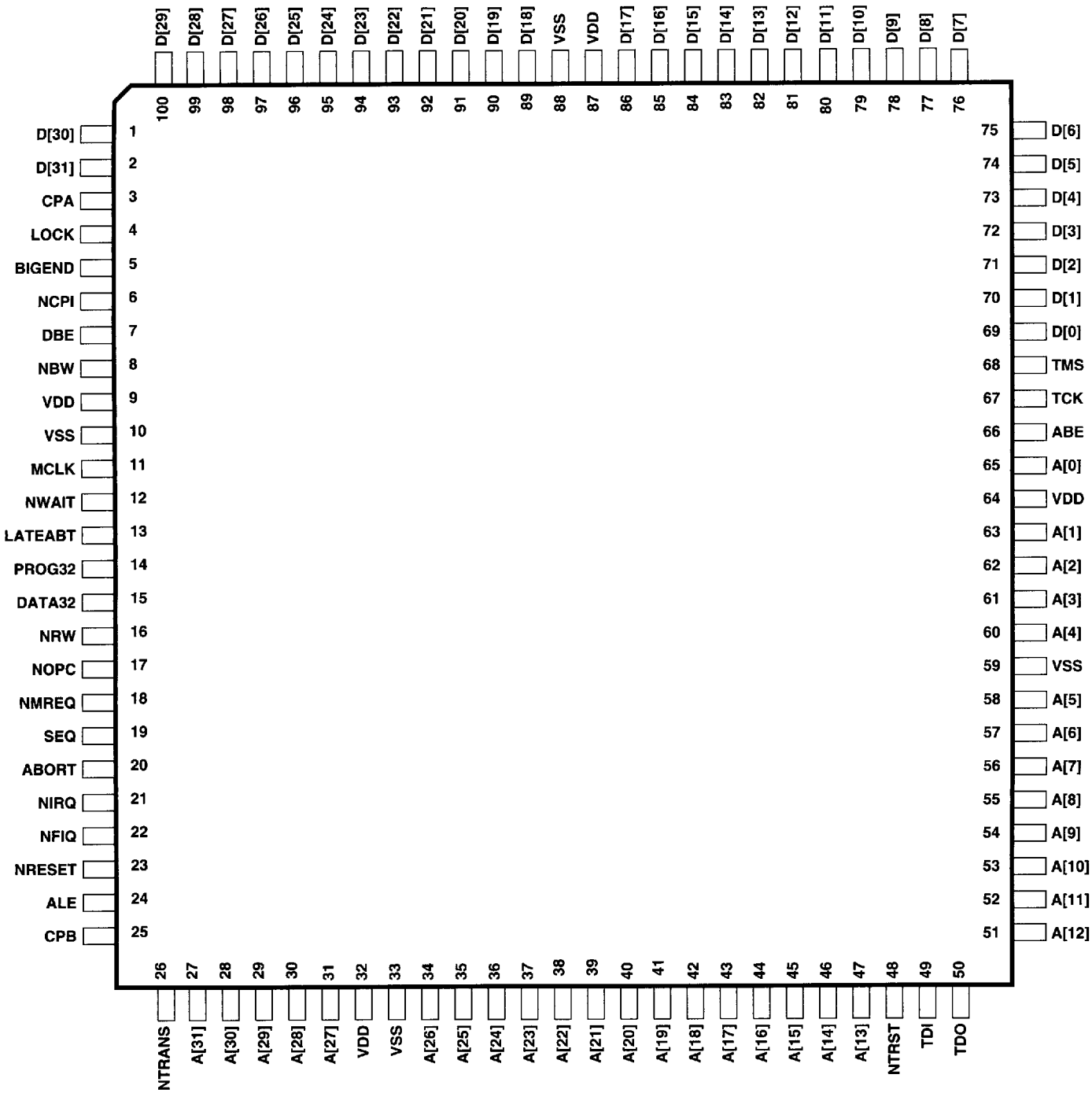
VY86C060A PIN DIAGRAM

144-PIN TQPF



VY86C06040 PIN DIAGRAM

100-PIN TQPF



ARM■ POWERED™

 1/94

130791-001 7.5M