FastMATH™/FastMIPS™ Evaluation Kit

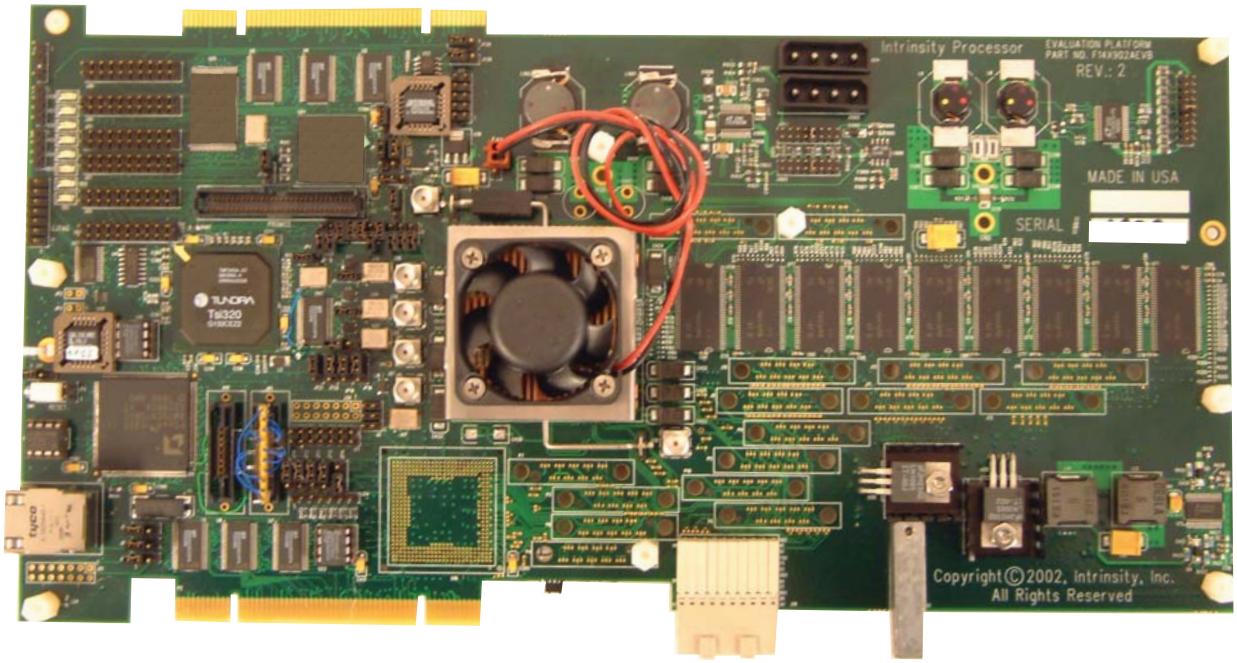

Figure 1: Intrinsity Evaluation Board

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Overview

The Intrinsity™ FastMATH™/FastMIPS™ evaluation platform has been developed to facilitate rapid analysis of the Intrinsity FastMATH/FastMIPS processors. The platform may be used to perform a variety of functions including:

- Processor functionality assessment
- Performance analysis
- Algorithm and software development
- Software and hardware tools evaluation
- Interfacing to PCI and RapidIO-based devices

Software tools provided include:

- C compiler

- Debugger
- Advanced matrix and vector math function libraries
- Power-on self-test diagnostics
- Evaluation software CD-ROMs from selected third-party vendors, including Green Hills Software
- Demo software

Extensive documentation is provided with the evaluation kit, including a user's guide and comprehensive processor documentation.

Modes of Operation

The evaluation platform supports three operational modes: standalone, RapidIO test and evaluation, and PCI application.

- Standalone mode
  - Evaluation platform is placed on a bench and connected to the external power supply
  - No connection is made to the external PCI interfaces
- RapidIO test and evaluation mode
  - Evaluation platform is inserted into a RapidIO HIP baseboard
- PCI application mode
  - Evaluation platform is inserted into a standard PCI slot and acts as a PCI target

Note: In each of the three operating modes, the board is powered by connecting it to a standard PC power supply using a hard drive power connector.

Evaluation Board Features

The evaluation board includes the following features:

- FastMATH processor configurable for emulation of a FastMIPS processor
- Full-length PCI card form factor
  - RapidIO™ host interoperability platform (HIP) compatible
  - Dual PCI connector support (top and bottom of printed circuit board)
  - Approximately two inches taller than PCI standard
- 32-bit, 3.3-volt, 5-volt tolerant, PCI 2.2-compatible interface operates at up to 33 MHz
- AMD™ Am79c973 10/100 PCI ethernet controller PCI 2.2-compatible interface
- 128-Mbytes of DDR-333 synchronous dynamic random-access memory (SDRAM) standard
- General purpose I/O (GPIO) subsystem
  - Field programmable gate array (FPGA) for miscellaneous system functions, including test registers, I^2C® interface, and universal asynchronous receiver/transmitter (UART)
  - 8-Mbytes of flash memory
  - PromICE® interface
  - 8 status light-emitting diodes (LEDs)
- MIPS® Extended Joint Test Action Group (EJTAG) revision 2.60-compliant debug interface connection
- Logic analyzer visibility and connection mechanism provided for all interfaces

Evaluation Kit Contents

The Intrinsity evaluation kit contains the following items:

- *Intrinsity Evaluation Kit Getting Started Guide*
- *Intrinsity Evaluation Board User's Guide*
- Evaluation board with processor and memory
- Intrinsity software and documentation CD-ROM
- Third-party evaluation software CD-ROM or CD-ROMs
- Extra jumpers
- Serial port dongle
- Gender changer
- DB-9–to–DB-9 serial cable
- Power supply

Additional Hardware and Software Requirements

To use the Intrinsity evaluation board, you will need to provide the following:

- Serial terminal emulation software or ethernet network with a host running telnet
- EJTAG debug probe (optional)

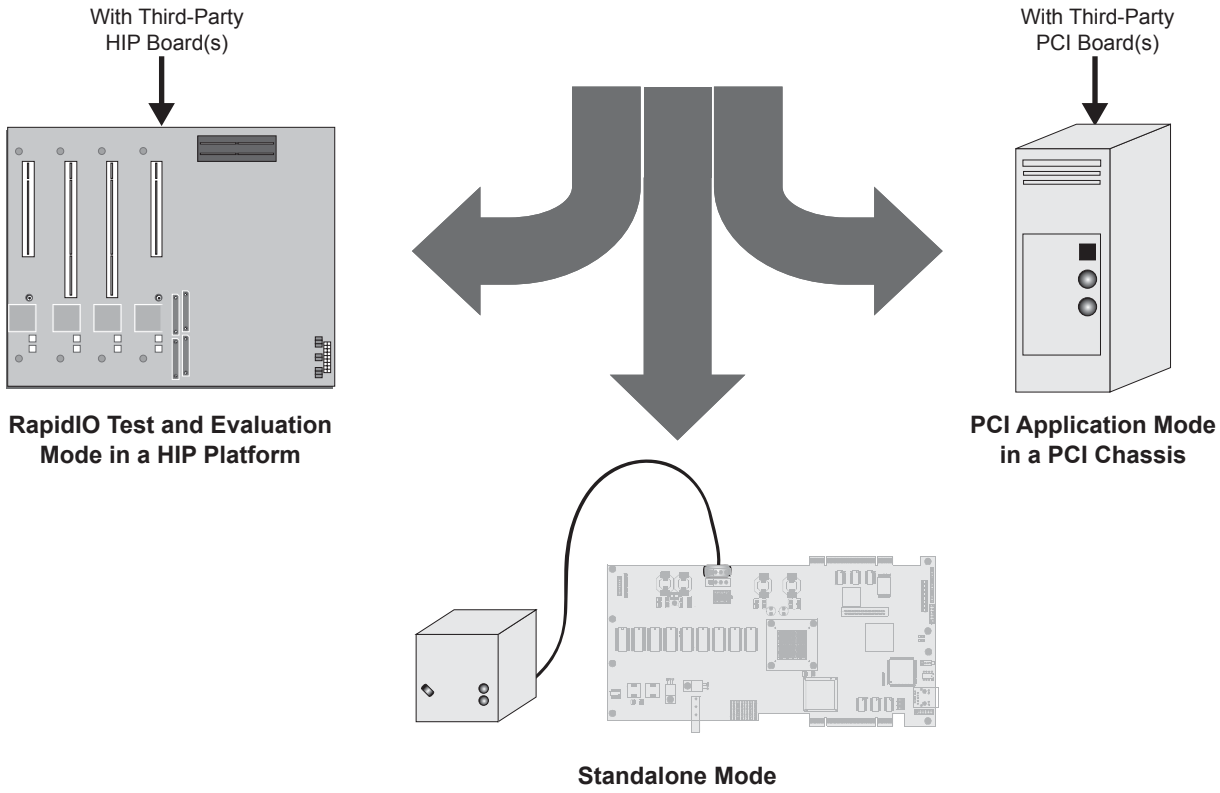

Figure 2: Evaluation platform modes of operation

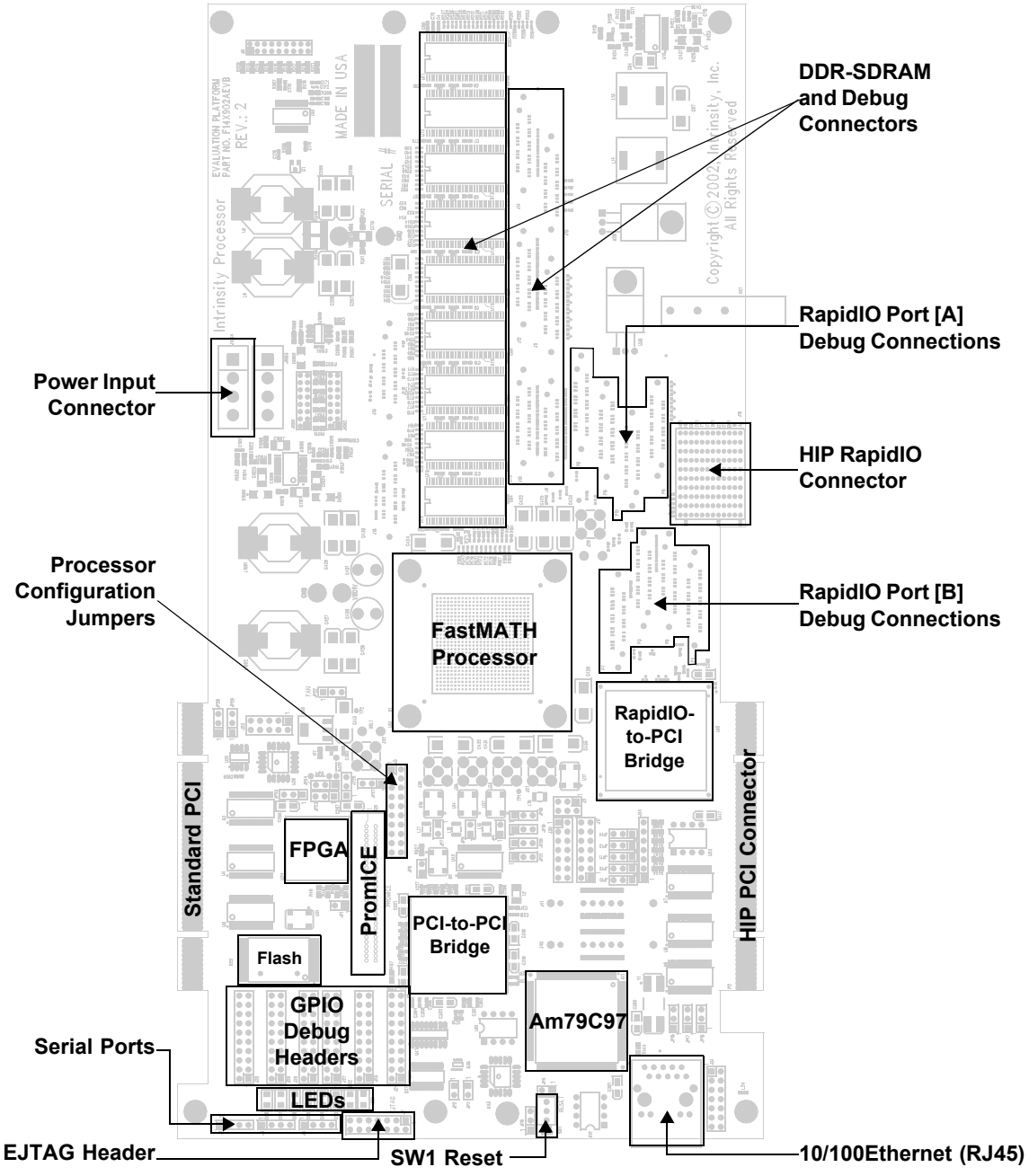

Figure 3: The FastMATH/FastMIPS evaluation platform

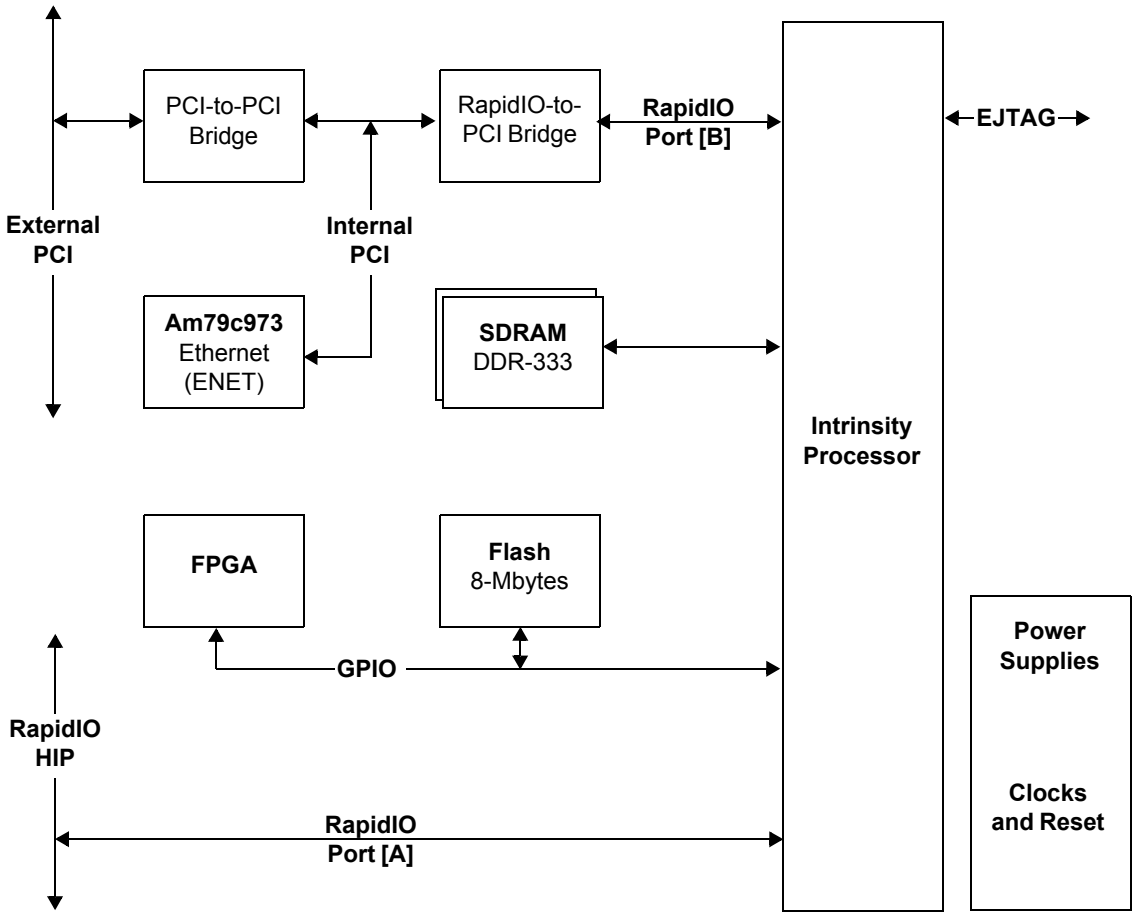

Figure 4: Evaluation platform block diagram

Board Form Factor

The format factor of the design is a dual-edged, long PCI card that includes the RapidIO HIP connectors along one side. The card is approximately 2-inches taller than a standard PCI card. Figure 3 on page 4 shows the physical outline of the board.

Including the HIP PCI connector, the evaluation board is 12.3-inches long by 6.4-inches wide.

External Interfaces

The evaluation platform includes five types of external interfaces: PCI, RapidIO HIP, serial ports, 10/100Base-T Ethernet, and flash ROM emulation.

- PCI interface

  There are two PCI interfaces in the evaluation platform to allow insertion in a standard PCI slot or RapidIO HIP platform slot. The PCI interfaces are 32 bits wide, operating at 33-MHz. The PCI interfaces are 5-volt tolerant and can plug into 5-volt or 3-volt PCI slots. When the standard PCI edge connector is used, most components are on the opposite side of the board from what the PCI specification recommends; thus, the board consumes more than one PCI slot.

- RapidIO HIP interface

  One of the processor's RapidIO ports is connected directly to a high-speed differential connector, located on the bottom of the evaluation board for use in a RapidIO hardware interoperability platform.

The design of the evaluation board and the HIP platform allow operation of both the RapidIO and one of the PCI interfaces when the evaluation board is plugged into the HIP baseboard.

- Serial ports

  The board includes a standard serial port interface. No hardware flow or modem control signals are provided. The signals are connected to standard Berg 4-pin headers. The evaluation kit includes a DB-9 serial port dongle that plugs into this header.

- 10/100Base-T ethernet interface

  A standard 10/100Base-T UTP Ethernet interface is provided on an RJ45 connector. The interface is wired as a transceiver port so that a direct connect Category 5 cable can be used to connect to a hub or to a switch port on a LAN. If the evaluation platform is to be connected directly to a computer, then a Category 5 crossover cable is required.

- Flash ROM emulation interface

  Flash emulation is accomplished using a 60-pin header that can be connected to a ROM emulator. Use of the ROM emulator is enabled via a jumper setting. The pinout conforms to the PromICE™ pin outs defined by Grammar Engine, Inc. (http://www.gei.com/).

Configuration Settings

There are options for setting the operational mode of the board, as well as processor-specific configuration. Most configuration is done with jumpers.

- Operational mode

  Standalone mode is jumper selectable. PCI or HIP modes are detected when the board is plugged in to a system. If the board is plugged into a HIP system that does not provide PCI slots, the user should enable standalone mode.

- Processor configuration

  The processor configuration is jumper selectable and includes the following modes of operation:
  - Force FastMIPS emulation mode
  - Big or little endian mode

SDRAM clock frequency is a derivative of the core processor frequency and is jumper selectable.

Test and Debug Interfaces

The board provides pre-defined connections to test equipment for debug and test.

- Processor interface

  All processor interface signals are visible to the user via logic analyzer connections provided on the evaluation platform. Many of these are accomplished by special land patterns designed specifically for the ***Tektronix TLA7xx series*** equipment.

- RapidIO interface

There are two RapidIO interfaces. Land patterns for the ***Tektronix P6880 high-density differential probes*** have been provided for each port. Each port consumes a single 136-channel module and requires probes. These connections are intended for use with the ***Tektronix RapidIO Support Package***.

- DDR-SDRAM

  The DDR-SDRAM interface can be instrumented by using ***Tektronix P6860*** probes. There are a total of 112 signal pins visible on this interface.

- General Purpose I/O (GPIO)

  The GPIO chip-select interface and FPGA signals have been brought out to several Berg style 0.1-inch headers. This allows the user maximum flexibility when assigning channels to the logic analyzer.

- Internal PCI

  The internal PCI bus may be monitored using a standard Mictor connector pin out as specified by Tektronix and New Wave (http://www.busboards.com/). The IDSEL field may be configured to point to the on-board Ethernet MAC, RapidIO-PCI Bridge, or PCI-PCI Bridge.

- Temperature Sensor

  A temperature sensor is connected to the FastMATH processor. This device, National LM86, has a two wire serial interface that may be accessed through one of two I^2C master interfaces: one in the RapidIO-to-PCI bridge chip and one in the FPGA.

JTAG/EJTAG Scan Support

JTAG headers are provided for direct access to the major scanable devices in the evaluation board.

Firmware

Included with the evaluation platform is a resident firmware package based on RedBoot firmware. It provides a complete bootstrap environment and includes facilities such as network downloading and debugging. RedBoot firmware provides a wide set of tools for downloading and executing programs on evaluation platform, as well as tools for manipulating the target system's environment. It can be used for both product development (debug support) and for end product deployment (flash and network booting).

Some highlights of the capabilities include:

- Simple command line interface accessible via serial port (terminal) or Ethernet (telnet)
- Integrated gdb stubs for connection to a host-based debugger via serial or Ethernet
- Power-on self-test
- Initialization of primary FastMATH/FastMIPS subsystems such as RapidIO, SDRAM, etc.
- Boot scripting support
- Configuration management of user control of aspects such as default flash image to boot from, default fail-safe image, static IP address, etc.
- Network bootstrap support including setup and download via BOOTP and TFTP
- X/YModem support for image download via serial port

The evaluation platform firmware is supplied in object form in the on-board flash memory. Source is available on request.

Acronyms & Abbreviations

DDR	double data-rate
FPGA	field-programmable gate array
GPIO	general purpose input/output
HIP	hardware interoperability platform
PCI	peripheral component interconnect
PLL	phase lock loop
SDRAM	synchronous dynamic random access memory
SMA	surface mount attach
UART	universal asynchronous receiver-transmitter
UTP	unshielded twisted pair

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