80C286

High-Speed CMOS 80286 Microprocessor

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

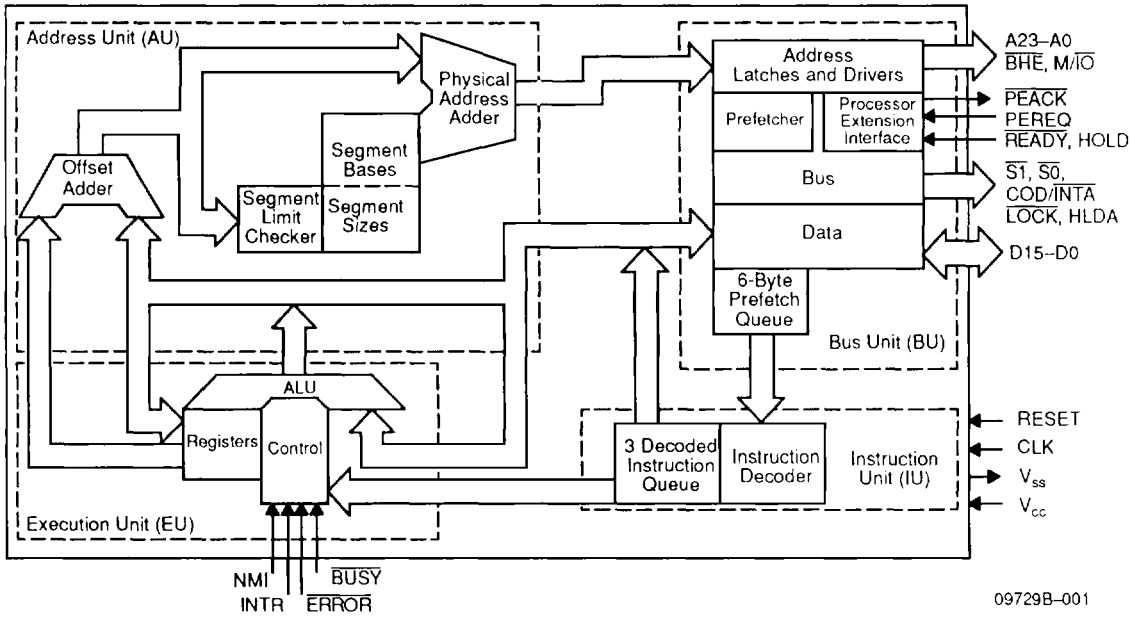
- **Ultra high-performance processor**
  - —Over 20 times the performance of the 8086
- **Wide range of clock rates**
  - —20 MHz (80C286-20)
  - —16 MHz (80C286-16)
  - —12.5 MHz (80C286-12)
- **100% functionally and pin compatible with NMOS 286**
- **Static CMOS design for low power operation**
  - —Standby mode Icc = 5 mA maximum
  - —Operating mode Icc
    - 220 mA max at 12.5 MHz
    - 260 mA max at 16 MHz
    - 310 mA max at 20 MHz
- **68-lead PLCC package**

GENERAL DESCRIPTION

The AMD 80C286 is a high-speed implementation of the industry standard 80286 microprocessor. It is 100% functionally compatible with the NMOS version and is a plug compatible replacement. AMD's high-speed CMOS process allows clock speeds much higher than those attainable with NMOS. The 80C286 operates at clock speeds up to 20 MHz.

This CMOS design is a static implementation which allows the processor to be clocked down to DC and still retain full register status. This is useful for designs where power consumption is a consideration as the 80C286 uses only 5 mA of supply current when in standby mode. The 80C286 also retains full functionality from its maximum clock frequency through very low frequencies down to DC. Since power consumption is proportional to clock speed, the 80C286 may be clocked at a slower rate to draw less current.

BLOCK DIAGRAM



09729B-001

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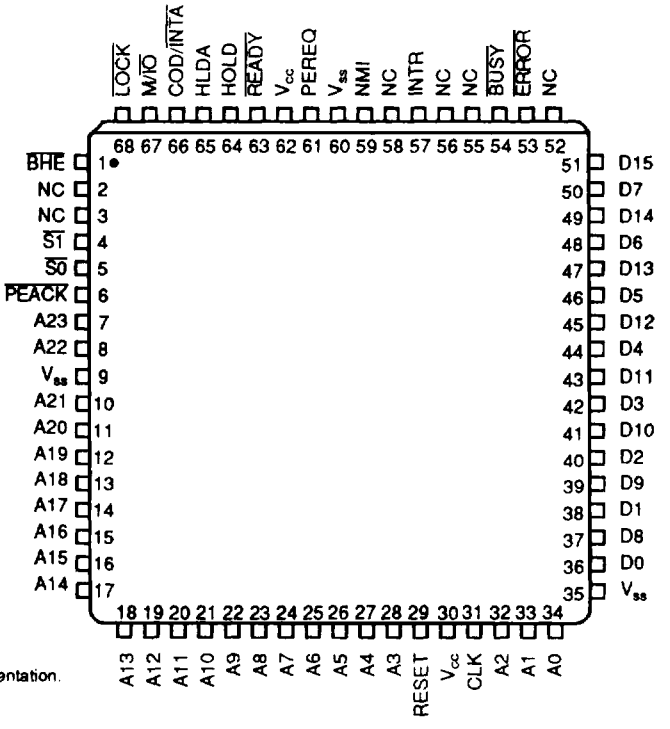
CONNECTION DIAGRAM

68-Pin PLCC

As viewed from top of package (PC side of component board).



Note: Pin 1 is marked for orientation.

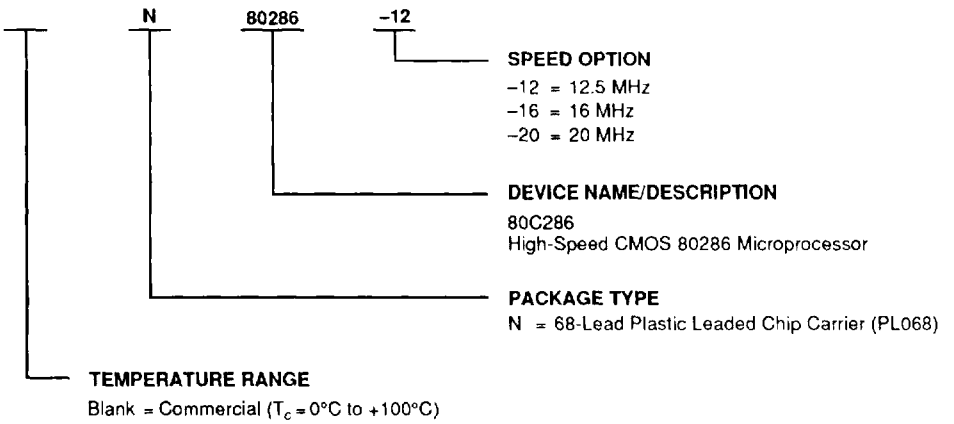
PIN DESIGNATIONS (sorted by pin number)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	$\overline{BHE}$	24	A7	47	D13
2	NC	25	A6	48	D6
3	NC	26	A5	49	D14
4	$\overline{ST}$	27	A4	50	D7
5	$\overline{S0}$	28	A3	51	D15
6	$\overline{PEACK}$	29	RESET	52	NC
7	A23	30	V_{cc}	53	$\overline{ERROR}$
8	A22	31	CLK	54	$\overline{BUSY}$
9	V_{ss}	32	A2	55	NC
10	A21	33	A1	56	NC
11	A20	34	A0	57	INTR
12	A19	35	V_{ss}	58	NC
13	A18	36	D0	59	NMI
14	A17	37	D8	60	V_{ss}
15	A16	38	D1	61	PEREQ
16	A15	39	D9	62	V_{cc}
17	A14	40	D2	63	$\overline{READY}$
18	A13	41	D10	64	HOLD
19	A12	42	D3	65	HLDA
20	A11	43	D11	66	COD/$\overline{INTA}$
21	A10	44	D4	67	M/$\overline{IO}$
22	A9	45	D12	68	$\overline{LOCK}$
23	A8	46	D5		

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations	
N	80C286-20 80C286-16 80C286-12

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

A23–A0

Address Bus (Outputs; Active High)

Address Bus outputs physical memory and I/O port addresses. A0 is Low when data is to be transferred on pins D7–D0. A23–A16 are Low during I/O transfers. The address bus is active High and floats to three-state Off during bus hold acknowledge.

$\overline{BHE}$

Bus High Enable (Output; Active Low)

Bus High Enable indicates transfer of data on the upper byte of the data bus D15–D8. Eight-bit oriented devices assigned to the upper byte of the data bus would normally use $\overline{BHE}$ to condition chip select functions. $\overline{BHE}$ is active Low and floats to three-state Off during bus hold acknowledge.

$\overline{BHE}$ and A_0 Encodings

$\overline{BHE}$ Value	A0 Value	Function
0	0	Word transfer
0	1	Byte transfer on upper half of data bus (D15–D8)
1	0	Byte transfer on lower half of data bus (D7–D0)
1	1	Reserved

$\overline{BUSY}$, $\overline{ERROR}$

Processor Extension Busy and Error (Inputs; Active Low)

Processor Extension Busy and Error indicate the operating condition of a processor extension to the 80C286. An active $\overline{BUSY}$ input stops 80C286 program execution on WAIT and some ESC instructions until $\overline{BUSY}$ becomes inactive (High). The 80C286 may be interrupted while waiting for $\overline{BUSY}$ to become inactive. An active $\overline{ERROR}$ input causes the 80C286 to perform a processor extension interrupt when executing WAIT or some ESC instructions. These inputs are active Low and may be asynchronous to the system clock.

CLK

System Clock (Input; Active High)

System Clock provides the fundamental timing for 80C286 systems. It is divided by two inside the 80C286 to generate the processor clock. The internal divide-by-two circuitry can be synchronized to an external clock generator by Low-to-High transition on the RESET input.

COD/$\overline{INTA}$

Code/Interrupt Acknowledge (Output)

Code/Interrupt Acknowledge distinguishes instruction fetch cycles from memory data read cycles. It also distinguishes interrupt acknowledge cycles from I/O cycles. COD/$\overline{INTA}$ is pulled up internally during bus hold.

D15–D0

Data Bus (Inputs/Outputs; Active High)

Data Bus inputs data during memory, I/O, and interrupt acknowledge read cycles; outputs data during memory and I/O write cycles. The data bus is active High and floats to three-state Off during bus hold acknowledge.

HOLD, HLDA

Bus Hold Request and Hold Acknowledge (Input/Output; Active High)

Bus Hold Request and Hold Acknowledge control ownership of the 80C286 local bus. The HOLD input allows another local bus master to request control of the local bus. When control is granted, the 80C286 will float its bus drivers to three-state Off and then active HLDA, thus entering the bus hold acknowledge condition. The local bus will remain granted to the requesting master until HOLD becomes inactive, which results in the 80C286 deactivating HLDA and regaining control of the local buys. This terminates the bus hold acknowledge condition. HOLD may be asynchronous to the system clock. These signals are active High.

INTR

Interrupt Request (Input; Active High)

Interrupt Request requests the 80C286 to suspend its current program execution and service a pending external request. Interrupt requests are masked whenever the interrupt enable bit in the flag word is cleared. When the 80C286 responds to an interrupt request, it performs two interrupt acknowledge bus cycles to read an 8-bit interrupt vector that identifies the source of the interrupt. To assure program interruption, INTR must remain active until the first interrupt acknowledge cycle is completed. INTR is sampled at the beginning of each processor cycle and must be active High at least two processor cycles before the current instruction ends in order to interrupt before the next instruction. INTR is level sensitive, active High, and may be asynchronous to the system clock.

$\overline{LOCK}$

Bus Lock (Output; Active Low)

Bus Lock indicates that other system bus masters are not to gain control of the system bus following the current bus cycle. The $\overline{LOCK}$ signal may be activated explicitly by the LOCK instruction prefix or automatically by 80C286 hardware during memory XCHG instructions, interrupt acknowledge, or descriptor table access. $\overline{LOCK}$ is active Low and floats to three-state Off during hold acknowledge.

M/$\overline{IO}$

Memory/IO Select (Output)

Memory/IO Select distinguishes memory access from I/O access. If High during Ts, a memory cycle or a halt/shutdown cycle is in progress. If Low, an I/O cycle or an

interrupt acknowledge cycle is in progress. M/$\overline{IO}$ is pulled up internally during bus hold.

NC
No Connect

No Connect pins should always remain unconnected.

NMI
Non-maskable Interrupt Request (Input; Active High)

Non-maskable Interrupt Request interrupts the 80C286 with an internally supplied vector value of 2. No interrupt acknowledge cycles are performed. The interrupt enable bit in the 80C286 flag word does not affect this input. The NMI input is active High, may be asynchronous to the system clock, and is edge-triggered after internal synchronization. For proper recognition, the input must have been previously Low for at least four system clock cycles and remain High for at least four system clock cycles.

PEREQ, $\overline{PEACK}$
Processor Extension Operand Request (Input; Active High)
Processor Extension Acknowledge (Output; Active Low)

Processor Extension Operand Request and Acknowledge extends the memory management and protection capabilities of the 80C286 to processor extensions. The PEREQ input requests the 80C286 to perform a data operand transfer for a processor extension. The $\overline{PEACK}$ output signals the processor extension when the requested operand is being transferred. PEREQ is active High and may be asynchronous to the system clock. $\overline{PEACK}$ is active Low.

$\overline{READY}$
Bus Ready (Input; Active Low)

Bus Ready terminates a bus cycle. Bus cycles are extended without limit until terminated by $\overline{READY}$ Low. Bus Ready requires that set-up and hold times relative to the system clock be met for correct operation. $\overline{READY}$ is ignored during bus hold acknowledge.

RESET
System Reset (Input; Active High)

System Reset clears the internal logic of the 80C286 and is active High. The 80C286 may be reinitialized at any time with a Low-to-High transition on RESET which remains active for more than 16 system clock cycles. During RESET active, the output pins of the 80C286 enter the state shown below:

80C286 Pin State during Reset

Pin Value	Pin Names
1 (High)	$\overline{S0}$, $\overline{S1}$, $\overline{PEACK}$, A23–A0, $\overline{BHE}$, $\overline{LOCK}$
0 (Low)	M/$\overline{IO}$, COD/$\overline{INTA}$, HLDA
Three-state Off	D15–D0

Operation of the 80C286 begins after a High-to-Low transition on RESET. The High-to-Low transition of RESET must be synchronous to the system clock. Approximately 50-system clock cycles are required by the 80C286 for internal initializations before the first bus cycle to fetch code from the power-on execution address is performed.

A Low-to-High transition of RESET synchronous to the system clock will begin a new processor cycle at the next High-to-Low transition of the system clock. The Low-to-High transition of RESET may be asynchronous to the system clock; however, in this case it cannot be predetermined which phase of the processor clock will occur during the next system period. Synchronous Low-to-High transitions of RESET are only required for systems where the processor clock must be phase-synchronous to another clock.

$\overline{S1}$, $\overline{S0}$
Bus Cycle Status (Outputs; Active Low)

Bus Cycle Status indicates initiation of a bus cycle and, along with M/$\overline{IO}$ and COD/$\overline{INTA}$, defines the type of bus cycle. The bus is in a Ts state whenever one or both are Low. $\overline{S1}$ and $\overline{S0}$ are active Low and are pulled up internally during bus hold.

80C286 Bus Cycle Status Definition

COD/$\overline{INTA}$	M/$\overline{IO}$	$\overline{S1}$	$\overline{S0}$	Bus cycle Initiated
0 (Low)	0	0	0	Interrupt acknowledge
0	0	0	1	Reserved
0	0	1	0	Reserved
0	0	1	1	None; not a status cycle
0	1	0	0	If A$_1$ = 1 then halt; else shutdown
0	1	0	1	Memory data read
0	1	1	0	Memory data write
0	1	1	1	None; not a status cycle
1 (High)	0	0	0	Reserved
1	0	0	1	I/O Read
1	0	1	0	I/O Write
1	0	1	1	None; not a status cycle
1	1	0	0	Reserved
1	1	0	1	Memory instruction read
1	1	1	0	Reserved
1	1	1	1	None; not a status cycle

V_{SS}
System Ground (Input)

System ground: 0 V.

V_{CC}
System Power (Input)

System power: +5-V power supply.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... +8.0 V
Input, Output or I/O
Voltage Applied GND ..... −1.0 V to V_{DD}+1.0 V
Power Dissipation/Speed
20 MHz ..... 1.7 W
16 MHz ..... 1.4 W
12.5 MHz ..... 1.2 W
Storage Temperature Range .... −65°C to +150°C
Junction Temperature ..... +165°C
Lead Temperature
(Soldering, Ten Seconds) ..... +275°C

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Operating Voltage Range ..... +4.5 V to +5.5 V
80C286-20 Only ..... +4.75 V to +5.25 V
Operating Temperature
Range ..... 0 to +100°C case temperature
(Meets laptop temperature requirements.)

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range

V_{CC} = +5 V ± 10% for 80C286-12 and 80C286-16; V_{CC} = +5 V ±5% for 80C286-20, T_C = 0°C to +100°C

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{IL}	Input Low Voltage		−0.5	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V
V_{ILC}	CLK Input Low Voltage		−0.5	1.0	V
V_{IHC}	CLK Input High Voltage		3.6	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = −2.0 mA	3.0	–	V
		I_{OH} = −100 mA	V_{CC} − 0.4		V
I_I	Input Leakage Current	V_{IN} = GND or V_{CC} Pins 29, 31, 57, 59, 61, 63–64	−10	10	µA
I_{SH}	Input Sustaining Current on $\overline{BUSY}$ and $\overline{ERROR}$ Pins	V_{IN} = GND (see Note 5)	−30	−500	µA
I_{BHL}	Input Sustaining Current High	V_{IN} = 1.0 V (see Note 1)	38	200	µA
I_{BHH}	Input Sustaining Current High	V_{IN} = 3.0 V (see Note 2)	−50	−400	µA
I_O	Output Leakage Current	V_O = GND or V_{CC} Pins 1, 7–8, 10–28, 32–34	−10	10	µA
I_{CCOP}	Active Power Supply Current	80C286-12 (see Note 4)	–	220	mA
		80C286-16 (see Note 4)	–	260	mA
		80C286-20 (see Note 4)	–	310	mA
I_{CCSB}	Standby Power Supply Current	(see Note 3)	–	5	mA

Notes: 1. I_{BHL} should be measured after lowering V_{IN} to GND and then raising to 1.0 V on the following pins: 36–51, 66, 67.
2. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering to 3.0 V on the following pins: 4–6, 36–51, 66–68.
3. I_{CCSB} tested with the clock stopped in phase two of the processor clock cycle. V_{IN} = V_{CC} or GND, V_{CC} = 5.5 V, outputs unloaded.
4. I_{CCOP} measured at 12.5 MHz for the 80C286-12, 16 MHz for the 80C286-16, and 20 MHz for the 80C286-20. V_{IN} = 2.4 V or 0.4 V, V_{CC} = 5.5 V, outputs unloaded.
5. I_{SH} should be measured after raising V_{IN} to V_{CC} and then lowering to GND on pins 53 and 54.

CAPACITANCE (T_A = +25°C; All Measurements Referenced to Device GND)

Parameter Symbol	Parameter Description	Typ	Unit	Test Conditions
C_{CLK}	CLK Input Capacitance	10	pF	FREQ = 1 MHz
C_{IN}	Other Input Capacitance	10	pF	
$C_{I/O}$	I/O Capacitance	10	pF	

SWITCHING CHARACTERISTICS over operating range

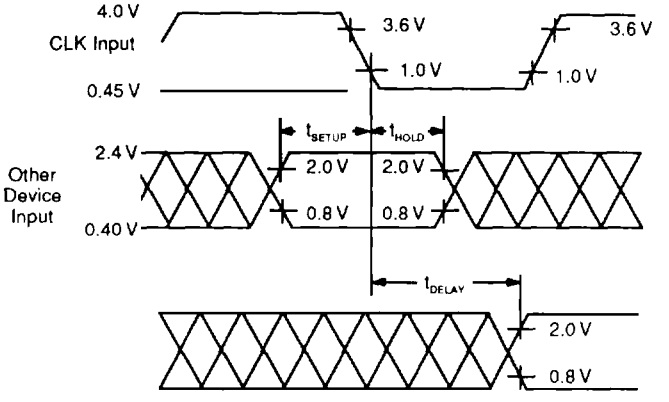
V_{CC} = +5 V ± 10% for 80C286-12 and 80C286-16; V_{CC} = +5 V ±5% for 80C286-20, T_C = 0°C to +100°C
AC Timings are referenced to 0.8 V and 2.0 V points of the signals as illustrated in datasheet waveforms, for 12.5 and 16 MHz, unless otherwise specified. For 20 MHz, AC timings are referenced to the 1.5 V point of the signals as illustrated in Data Sheet waveforms, unless otherwise specified.

Parameter		Test	12.5 MHz		16 MHz		20 MHz		
Symbol	Description	Conditions	Min	Max	Min	Max	Min	Max	Units
Timing Requirements									
1	System Clock (CLK) Period		40	–	31	–	25	–	ns
2	System Clock (CLK) Low Time	@ 1.0 V	11	–	7	–	6	–	ns
3	System Clock (CLK) High Time	@ 3.6 V	13	–	11	–	9	–	ns
17	System Clock (CLK) RISE Time	1.0 V to 3.6 V	–	8	–	5	–	4	ns
18	System Clock (CLK) FALL Time	3.6 V to 1.0 V	–	8	–	5	–	4	ns
4	Asynchronous Inputs SETUP Time	(Note 1)	15	–	5	–	4	–	ns
5	Asynchronous Inputs HOLD Time	(Note 1)	15	–	5	–	4	–	ns
6	RESET SETUP Time		10	–	10	–	10	–	ns
7	RESET HOLD Time		0	–	0	–	0	–	ns
8	Read Data SETUP Time		5	–	5	–	3	–	ns
9	Read Data HOLD Time		4	–	3	–	2	–	ns
10	$\overline{\text{READY}}$ SETUP Time		20	–	12	–	10	–	ns
11	$\overline{\text{READY}}$ HOLD Time		20	–	5	–	3	–	ns
20	Input RISE/FALL Times	0.8 V to 2.0 V	–	8	–	6	–	6	ns
Timing Responses									
12A	Status/$\overline{\text{PEACK}}$ Active Delay	1, (Notes 3, 6, 7)	1	21	1	18	1	15	ns
12B	Status/$\overline{\text{PEACK}}$ Inactive Delay	1, (Notes 3, 6)	1	24	1	20	1	16	ns
13	Address Valid Delay	1, (Notes 2, 3)	1	32	1	27	1	23	ns
14	Write Data Valid Delay	1, (Notes 2, 3)	0	31	0	28	0	27	ns
15	Address/Status/Data Float Delay	2, (Note 5)	0	32	0	29	0	25	ns
16	HLDA Valid Delay	1, (Notes 2, 3, 8)	0	25	0	25	0	20	ns
19	Address Valid–Status SETUP Time	1, (Notes 3, 4)	22	–	16	–	9	–	ns

Notes: 1. Asynchronous inputs are INTR, NMI, HOLD, PEREQ, $\overline{\text{ERROR}}$, and $\overline{\text{BUSY}}$. This specification is given only for testing purposes to assure recognition at a specific CLK edge.
2. Delay from 1.0 V on the CLK to 0.8 V or 2.0 V.
3. Output load: C_L = 100 pF.
4. Delay measured from address either reaching 0.8 V or 2.0 V (valid) to status going active reaching 0.8 V or status going inactive reaching 2.0 V.
5. Delay from 1.0 V on the CLK to Float (no current drive) condition.
6. Delay from 1.0 V on the CLK to 0.8 V for Min (HOLD time) and to 2.0 V for Max (inactive delay).
7. Delay from 1.0 V on the CLK to 2.0 V for Min (HOLD time) and to 0.8 V for Max (active delay).
8. Delay from 1.0 V on the CLK to 2.0 V.

Switching Test Conditions

Test Condition	IL (Constant Current Source	CL
1	| 2.0 mA|	100 pF
2	−6 mA (V_{OH} to Float) 8 mA (V_{OL} to Float)	100 pF



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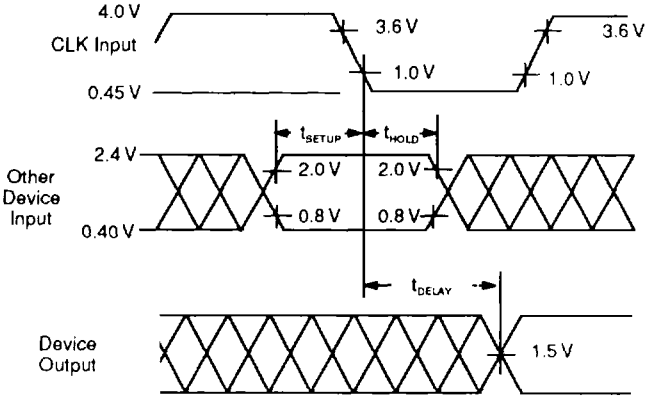
12.5 MHz and 16 MHz AC Setup, Hold and Delay Time Measurement



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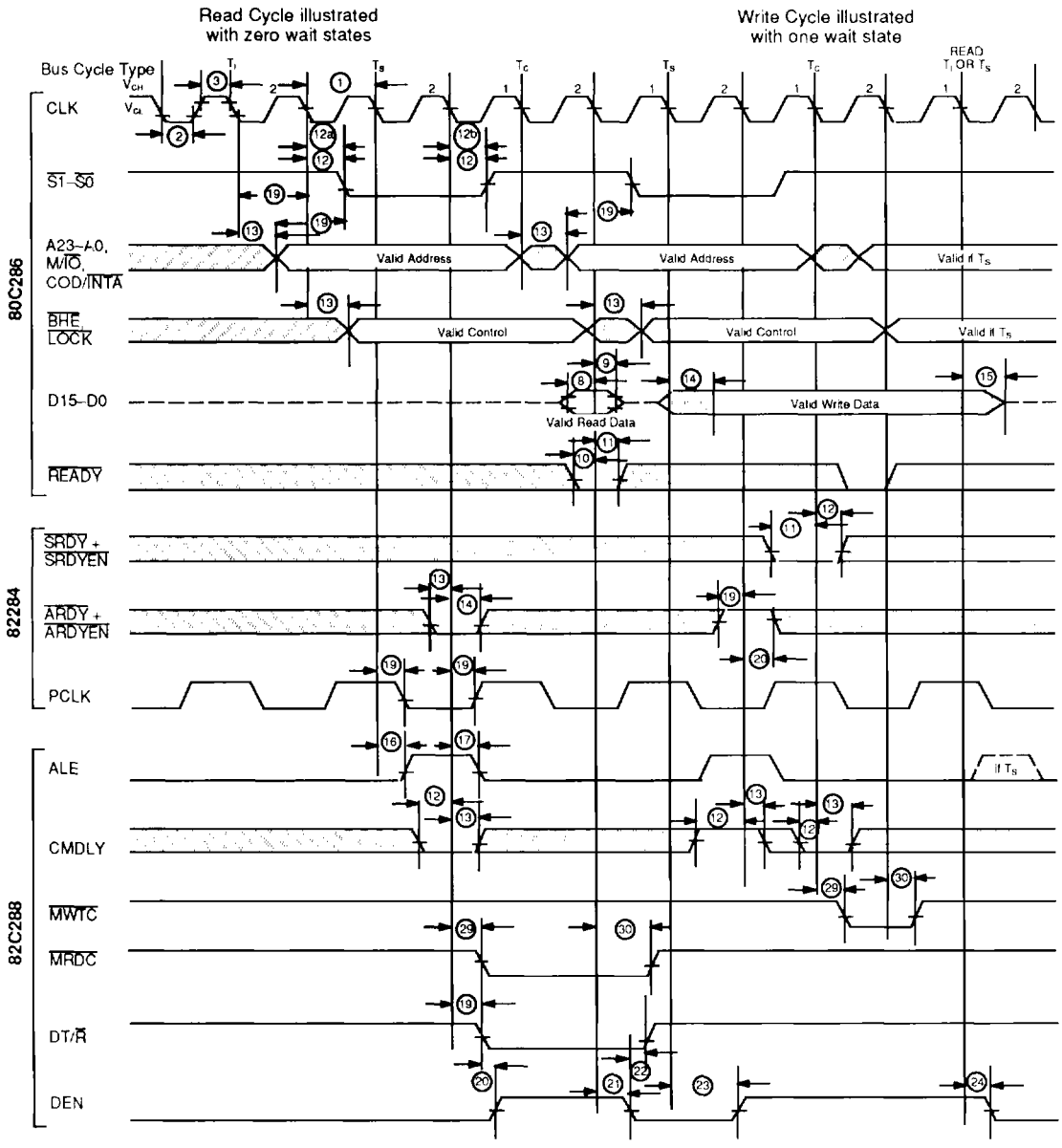
20 MHz AC Setup, Hold and Delay Time Measurement

SWITCHING WAVEFORMS

Major Cycle Timing



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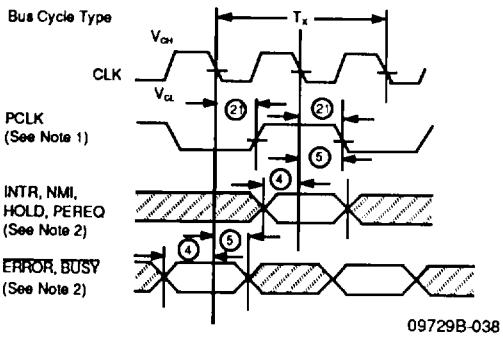
Note: The modified timing is due to the $\overline{CMDLY}$ signal being active.

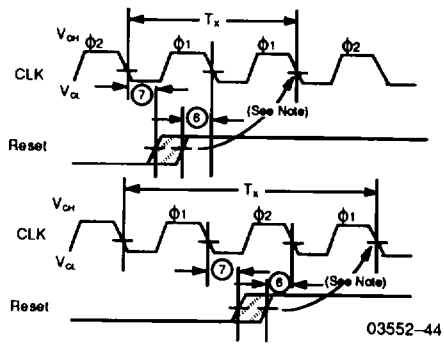
SWITCHING WAVEFORMS (continued)

80C286 Asynchronous Input Signal Timing



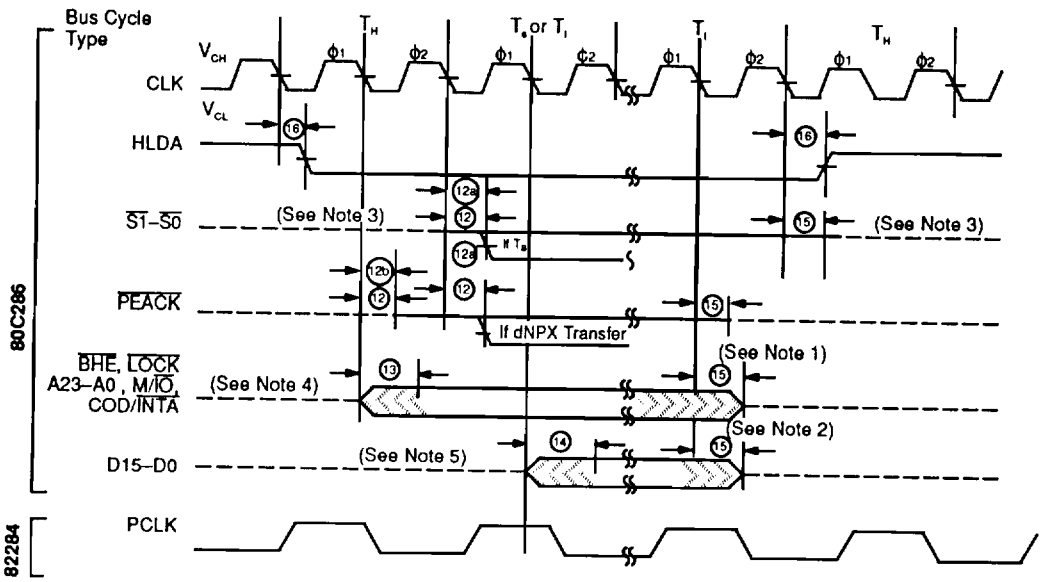
Notes: 1. PCLK indicates which processor cycle phase will occur on the next CLK. PCLK may not indicate the correct phase until the first bus cycle is performed.
2. These inputs are asynchronous. The setup and hold times shown assure recognition for testing purposes.

80C286 Reset Input Timing and Subsequent Processor Cycle Phase



Note: When Reset meets the set-up time shown, the next CLK will start or repeat $\phi 1$ of a processor cycle.

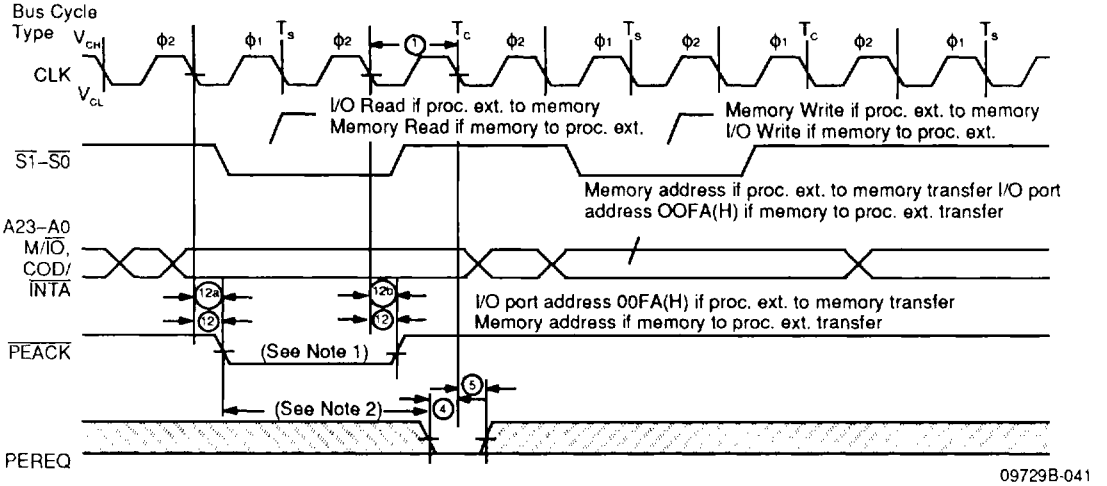
Exiting and Entering Hold



Notes: 1. These signals may not be driven by the 80C286 during the time shown. The worst case in terms of latest float time is shown.
2. The data bus will be driven as shown if the last cycle before T_i in the diagram was a write T_c.
3. The 80C286 puts its status pins in a high impedance logic one state during T_H.
4. $\overline{BHE}$ and $\overline{LOCK}$ are driven at this time but will not become valid until T_a.
5. The data bus will remain in three-state Off if a read cycle is performed.

SWITCHING WAVEFORMS (continued)

80C286 PEREQ/PEACK Timing Required PEREQ Timing for One Transfer Only



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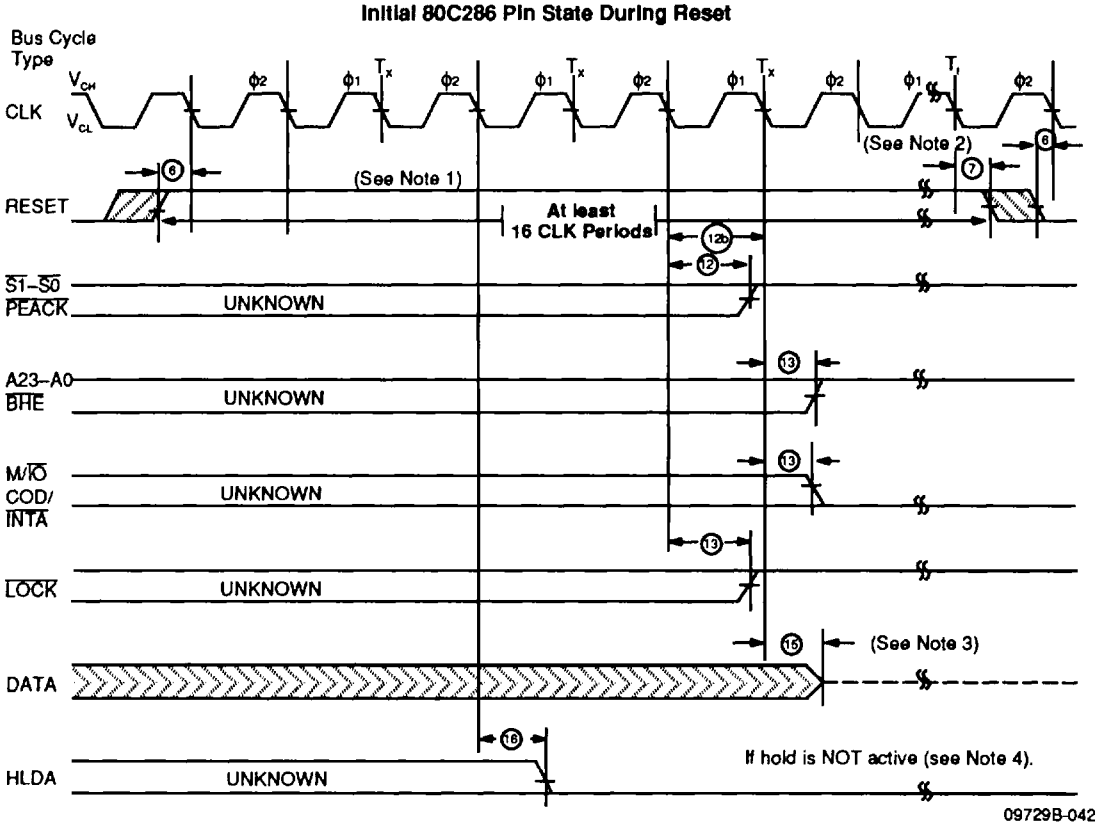
Notes: 1. PEACK always goes active during the first bus operation of a processor extension data operand transfer sequence. The first bus operation will be either a memory read at operand address or I/O read at port address 00FA(H).

2. To prevent a second processor extension data operand transfer, the worst case maximum time (shown above) is:
$3 \times 1 - 12a\ max - 4\ min$. The actual, configuration dependent, maximum time is: $3 \times 1 - 12a\ max - 4\ min + A \times 2 \times 1$.
A is the number of extra T_C states added to either the first or second bus operation of the processor extension data operand transfer sequence.

Initial 80C286 Pin State During Reset



Notes: 1. Set-up time for RESET ↑ may be violated with the consideration that $\phi 1$ of the processor clock may begin one system CLK period later.

2. Set-up and hold times for RESET ↓ must be met for proper operation, but RESET ↓ may occur during $\phi 1$ or $\phi 2$.
3. The data bus is only guaranteed to be in three-state Off at the time shown.
4. HOLD is acknowledged during RESET, causing HLDA to go active and the appropriate pins to float. If HOLD remains active while RESET goes inactive, the 80C286 remains in HOLD state and will not perform any bus accesses until HOLD is deactivated.