AMD

AMD Athlon™ Processor Module

Signal and Power-Up Requirements

Application Note

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Contents

Revision History

Date	Rev	Description
June 2000	B	Changed PLL power source signal name from VDDA to VCCA throughout document.
June 2000	A	Initial public release.

Application Note

AMD Athlon™ Processor Module Signal and Power-Up Requirements

Introduction

This document describes the AMD Athlon™ processor module power-up requirements during system turn-on and warm resets. These requirements can be adhered to with motherboard modifications and/or the use of a recommended system power supply for the specific motherboard. This document is applicable to all current Slot A motherboards.

Power-Up Requirements

Sequence

The AMD Athlon™ processor requires that the system clocks (SYSCLK/SYSCLK#) to the processor be running prior to PWROK. PWROK is an output of the voltage regulation circuit on the motherboard indicating that VCC_CORE is valid to the processor. Figure 1 shows the relationship between key signals in the system during a power-up sequence. This figure details the requirements of the processor.

Note: *Figure 1 represents several signals generically by using names not necessarily consistent with any pin lists or schematics.*

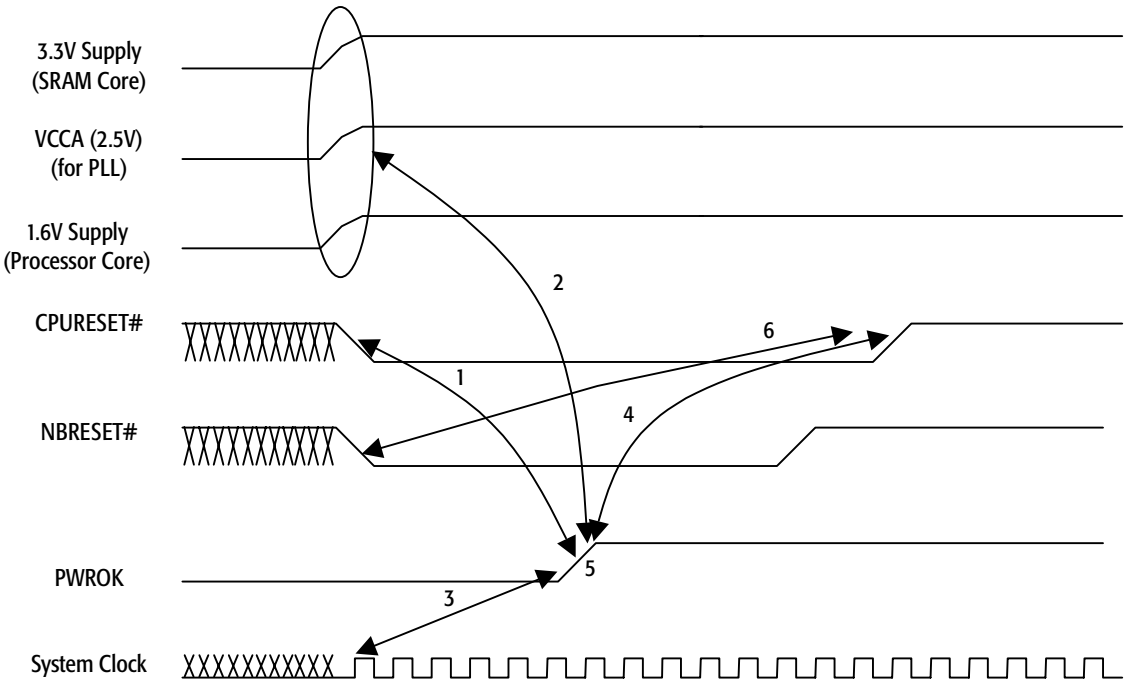

Figure 1. Signal Relationship during Power-Up Sequence

Requirements Sequence

Many peripheral controllers assert CPURESET# and NBRESET# (for example, PCIRESET#) as soon as possible after receiving power. The system clock generator produces a clock soon after it has valid power (see specific system clock data sheets for more information). System clock generators for

AMD Athlon processors generate system clocks **3ms** after receiving a valid power level (that is, 3.3V) from the motherboard. The AMD Athlon processor pulls the open-drain clocks (SYSCLK/SYSCLK#) to VCC_CORE on the module. Because the AMD ATX Power Supply Specification requires 3.3V to be valid prior to VCC_CORE, the motherboard must assert PWROK only after a valid system clock is generated. To accommodate a variety of system parameters, it is recommended that PWROK should assert only after at least **3ms** past a valid VCC_CORE (a valid system clock).

When PWROK asserts, the processor PLL turns on and begins to lock. After a specified period, to ensure the PLL has locked, the reset signals can be deasserted.

Timing Requirements

The signal timing requirements are as follows:

1. CPURESET# must be asserted before PWROK asserts

   The AMD Athlon processor does not set the correct clock multiplier if PWROK is asserted prior to a CPURESET# assertion. It is recommended that CPURESET# be asserted at least **10ns** prior to the assertion of PWROK.

2. All motherboard power supplies should be ramped before the assertion of PWROK.

   The processor core voltage, VCC_CORE, should have a stable voltage (for example, 1.6V) as indicated by the Voltage ID (VID) prior to PWROK assertion. Before PWROK assertion, the AMD Athlon processor is clocked by a ring oscillator. This minimum time is not specified.

   The AMD Athlon processor PLL is powered by VCCA on the processor module. VCCA is derived by a resistor divider powered by VCC_SRAM from the motherboard. The processor PLL does not lock if VCCA is not high enough for the processor logic to switch for some period of time before PWROK asserts. The recommended minimum time before PWROK assertion is 5µs.

3. The system clock (SYSCLK/SYSCLK#) should be running before PWROK asserts.

   When PWROK asserts, the AMD Athlon processor switches from driving the internal processor clock grid from the ring oscillator to driving from the PLL. The reference system clock should be valid at this time. If it is not valid, the

subsequent requirements may be undermined. It is recommended that PWROK be asserted **3ms** after the system clocks are running.

4. PWROK assertion to deassertion of CPURESET#

   The duration of reset during cold boots is intended to satisfy the time it takes for the PLL to lock with a less than 1-ns phase error. The AMD Athlon processor PLL begins to run after PWROK asserts and the internal clock grid is switched from the ring oscillator to the PLL. The PLL lock time may take from hundreds of nanoseconds to tens of microseconds. It is recommended that the minimum time between PWROK assertion to the deassertion of CPURESET# be at least **100us**.

5. PWROK should be monotonic.

   The processor should not switch between the ring oscillator and the PLL after the initial assertion of PWROK.

6. NBRESET# should be asserted before CPURESET# is deasserted.

   If NBRESET# does not deassert until after CPURESET# has deasserted, then when CONNECT asserts due to a NBRESET# assertion, the processor behavior is undefined. There must be sufficient overlap in the resets to ensure that CONNECT has a chance to be sampled asserted by the processor in advance of the processor coming out of reset.

PROCRDY and the CONNECT Signals

The SIP stream initialization process is documented in the *AMD Athlon™ System Bus Specification*, order# 21902. However, this section documents some implementation details.

The AMD Athlon processor asserts PROCRDY when CPURESET# is asserted and deasserts PROCRDY when CPURESET# deasserts.

The system controller asserts CONNECT during NBRESET# assertion and deasserts it when NBRESET# deasserts. At this point, when it samples PROCRDY deassert, the system controller begins sending the SIP stream (start bit first).

The AMD Athlon processor implementation interprets the beginning of a SIP stream when it deasserts PROCRDY (some

short time prior to the pin transitioning) and it sees a Low-to-High transition on CONNECT.

The system controller interprets the AMD Athlon processor as being ready to accept a SIP stream when it sees PROCRDY deasserted after NBRESET# deasserts.

Note: *Some system controllers, like the AMD-751™ system controller, may not look for an edge transition.*

However, current processor implementations do not impose requirements on the order of CPURESET# and NBRESET# deassertions.

Processor Warm Reset Requirements

The AMD Athlon™ Processor and System Controller Reset Pins

Warm resets are different from cold resets because the motherboard power supplies are already stable and the PLL is locked. Therefore, requirements are different for warm resets and because the AMD Athlon processor may be in a sleep state when CPURESET# asserts.

Duration of CPURESET# As a Function Of Low Power Ratio

Although the AMD Athlon processor PLL is already locked, the AMD Athlon processor requires that CPURESET# be asserted for some period of time to ensure that PROCRDY can assert without glitching.

The AMD Athlon processor clock grid is slowed down to a ratio of as little as 1/128th of its normal frequency. Therefore, it takes a corresponding length of time to assert PROCRDY. In addition, in order to avoid glitching PROCRDY, it is necessary to assert CPURESET# for a long enough time that the AMD Athlon processor can synchronize CPURESET# into the processor clock domain.

Table 1 shows minimum CPURESET# duration to ensure the proper PROCRDY pin behavior as a function of the low power ratio.

Table 1. CPURESET# Minimum Duration

AMD Athlon™ Processor Module Version	Low Power Divisor (recommended)	CPURESET# Min assertion time
AMD Athlon Processor Module Model 1	8	0.5µs @100Mhz SYSCLK
AMD Athlon Processor Module Model 2	128	2.5µs @100MHz SYSCLK
AMD Athlon Processor Module Model 4	128	2.5µs @100MHz SYSCLK

Assertion of CPURESET# to Deassertion of NBRESET#

When the system controller comes out of reset, the processor must have PROCRDY asserted in response to the CPURESET# assertion or else the system controller may start sending the SIP stream (because some system controllers sample only for a low PROCRDY level). This scenario implies a dependency from CPURESET#=0 to NBRESET#=1:

Sample Current Motherboard Implementation Solution

This section describes the currently implemented motherboard solution, assuming the use of a AMD-756™ peripheral bus controller (Southbridge), and describes how the solution meets the requirements described in "Power-Up Requirements" on page 2 and "Processor Warm Reset Requirements" on page 5.

The motherboard has the following two voltage regulators:

- The AMD Athlon processor core voltage regulator (VCC_CORE)

  This regulator uses 5V and provides a processor core voltage determined by the voltage ID (VID). A typical core voltage is 1.6V. The 5V is provided by the silver box power supply.

  Current motherboards use 5V to power the VID resistor network.

- SRAM core voltage regulator (VCC_SRAM)

  This regulator either passes 3.3V from the power supply or 2.5V. The voltage is determined by VCC2SEL, which identifies if the SRAM requires a core voltage of 2.5V or 3.3V.

Although the system clock generator is powered from the 3.3V supply, the outputs are open drain and pulled up to the AMD Athlon processor core voltage. Therefore, the system clock does not really toggle until the processor core voltage has ramped.

A resistor network on the processor module provides VCCA from VCC_SRAM. VCCA nominally should be 2.5V and therefore, the network may divide down from 3.3V.

Description of Power-Up Sequence

The power-up sequence is as follows:

1. The power supply ramps and the startup VID value becomes stable.
2. At this time, the processor core regulator begins ramping VCC_CORE. In addition, the SRAM regulator begins ramping VCC_SRAM based on the value of VCC2SEL and the system clock generator begins to power up.
3. A resistor network powered by VCC_SRAM begins to provide VCCA.
4. The power supply asserts PWROK as much as 500ms after the power supply begins to provide stable 5V and 3.3V. (This is not the same signal as the PowerGood signal to the Southbridge input).
5. PWROK is provided to the processor once the processor core voltage regulator produces a stable voltage based on VID and 5V from the power supply. In addition, pullup resistors on the open-drain system clocks from the clock generator become stable and SYSCLK/SYSCLK# begins transitioning.
6. PowerGood is provided to the Southbridge once 5V is valid from the power supply and VCC_CORE is valid. (PowerGood to the Southbridge is based on processor VCC_CORE, not PWROK). Before PowerGood is asserted, the Southbridge drives CPURESET# and NBRESET# asserted.
7. When the Southbridge sees the assertion of PowerGood, it waits 1.8ms and then deasserts NBRESET#. It then waits 1.5µs before deasserting CPURESET#.

Satisfaction of Requirements

The satisfaction requirements are as follows:

- CPURESET# must be asserted before PWROK asserts.

  This requirement is satisfied because the Southbridge asserts CPURESET# before PowerGood is asserted to the Southbridge. The Southbridge gets its power from the supply and begins driving CPURESET# Low as many as 500ms before the supply asserts PowerGood. PWROK asserts once the AMD Athlon processor core regulator powered by the supply becomes stable.

- All supplies should be ramped before PWROK asserts.

  PWROK asserts only when the processor VCC_CORE is stable. The requirement is for approximately 10µs to pass from the time processor VCC_CORE is of high enough voltage to reset some flops until PWROK asserts, which is accomplished by an RC network powered by VCC_CORE driving PWROK.

  VCCA asserts once VCC_SRAM is stable, which can be an issue because PWROK is a function of only the processor core regulator providing a stable voltage when it should be a function of the SRAM core regulator as well. The RC time constant of the circuit that drives PWROK must be large enough to ensure that VCC_SRAM and VCCA are stable when PWROK asserts.

- The system clock should be running before PWROK asserts.

  The system clock itself only runs when AMD Athlon processor VCC_CORE is ramped. PWROK asserts only when processor VCC_CORE is stable. Therefore, in theory, this requirement is not strictly satisfied. However, it is presumed that the regulator has ramped VCC sufficiently High (that is, ~1.2V) for a substantial length of time prior to the assertion of PWROK. This requirement should provide enough swing on the system clock that it is running well enough in advance of the assertion of PWROK. It is recommended that 6ms has elapsed prior to the assertion of PWROK.

- PWROK assertion to deassertion of CPURESET#

  The system implementation only ensures the time from the Southbridge PowerGood to the deassertion of CPURESET#. It is known that the Southbridge PowerGood is generated after processor core VCC but not precisely after PWROK. This requirement is satisfied if:

  ```
  (AMD Athlon processor VCC_CORE Valid -> Southbridge
  PowerGood -> CPURESET# deassertion time) >
  (AMD Athlon processor Core Vcc Valid -> PWROK + PLL lock
  time)
  ```

  The motherboard design is such that the delta time to Southbridge PowerGood and PWROK from processor core VCC is not large and PLL lock time is much smaller than the 1.8ms reset duration, which satisfies this requirement.

- PWROK should be monotonic

  Because PWROK asserts when processor VCC_CORE is stable, it should not be deasserted and reasserted.

- NBRESET# should be asserted prior to the deassertion of CPURESET#.

  The Southbridge asserts both CPURESET# and NBRESET# when Southbridge PowerGood is not asserted, therefore, this requirement is satisfied.

Satisfaction of Requirements Specific to Warm Resets:

The satisfaction requirements specific to warm boots are as follows:

- Duration of CPURESET#

  All AMD-756 peripheral bus controllers from Rev B on implement 1.8ms warm resets, which is long enough for the AMD Athlon processor.

- Assertion of CPURESET# to deassertion of NBRESET#

  This requirement is currently satisfied by the implementation, because CPURESET# and NBRESET# are asserted simultaneously. In addition, NBRESET# is always asserted for at least 1.8ms. The AMD-756 peripheral bus controller must be programmed such that port 92 and KBC resets are directed to the INIT# pin and not to the CPURESET# pin. In addition, there are some bits in C3A50 (a AMD-756 peripheral bus controller register) that should never be set because they could force CPURESET# independent of NBRESET#.

Miscellaneous

FID Sampling

The AMD Athlon processor module Model 1 and Model 2 transparently sample the BP/FID pins from the time PWROK asserts until the deassertion of CPURESET#.

The AMD Athlon processor module Model 4 transparently samples the pads in the same manner as the Model 1 and Model 2 parts. The clock multiplier may be provided either external to the part or via resistors in the package.