Intel® Xeon® Processor E5 v4 Product Family

Thermal Mechanical Specification and Design Guide

June 2016

Document Number: 333812-002

Intel technologies' features and benefits depend on system configuration and may require enabled hardware, software or service activation. Learn more at Intel.com, or from the OEM or retailer.

No computer system can be absolutely secure. Intel does not assume any liability for lost or stolen data or systems or any damages resulting from such losses.

You may not use or facilitate the use of this document in connection with any infringement or other legal analysis concerning Intel products described herein. You agree to grant Intel a non-exclusive, royalty-free license to any patent claim thereafter drafted which includes subject matter disclosed herein.

No license (express or implied, by estoppal or otherwise) to any intellectual property rights is granted by this document.

The products described may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Intel disclaims all express and implied warranties, including without limitation, the implied warranties of merchantability, fitness for a particular purpose, and non-infringement, as well as any warranty arising from course of performance, course of dealing, or usage in trade.

Intel® Turbo Boost Technology requires a PC with a processor with Intel Turbo Boost Technology capability. Intel Turbo Boost Technology performance varies depending on hardware, software and overall system configuration. Check with your PC manufacturer on whether your system delivers Intel Turbo Boost Technology. For more information, see http://www.intel.com/technology/turboboost

Copies of documents which have an order number and are referenced in this document may be obtained by calling 1-800-548-4725 or by visiting www.intel.com/design/literature.htm.

Intel, Xeon, and the Intel logo are trademarks of Intel Corporation in the U.S. and/or other countries.

*Other names and brands may be claimed as the property of others.

Copyright © 2016, Intel Corporation. All Rights Reserved.

Contents

1 Introduction 7
- 1.1 Definition of Terms 7
- 1.2 Reference Documents 9

2 Processor Thermal Specifications and Features 11
- 2.1 Margin to Thermal Specification (M) 11
- 2.2 Embedded Server Thermal Profiles 13
  - 2.2.1 NEBS T_{CASE} Thermal Profile 13
  - 2.2.2 NEBS T_{DTS} Thermal Profile 14
- 2.3 Processor Thermal Features 15
  - 2.3.1 Absolute Processor Temperature 15
  - 2.3.2 Short Duration TCC Activation 16
  - 2.3.3 Thermal Design Guidelines 16

3 Processor Thermal Specifications 19
- 3.1 Thermal Specifications 19
- 3.2 TCASE and DTS Based Thermal Specifications 20
- 3.3 Thermal Metrology 20
- 3.4 Server Processor Thermal Profiles and Form Factors 21
- 3.5 Embedded Server Processor Thermal Profiles 25

4 Processor Mechanical Specifications 27
- 4.1 Package Size 27
- 4.2 Package Loading Specifications 28
- 4.3 Processor Mass Specification 29
- 4.4 Processor Materials 29
- 4.5 Processor Markings 29
- 4.6 Package Handling Guidelines 29

5 Quality, Reliability and Ecological Requirements 31
- 5.1 Use Conditions 31
- 5.2 Intel Reference Component Validation 32
  - 5.2.1 Board Functional Test Sequence 32
  - 5.2.2 Post-Test Pass Criteria Examples 32
  - 5.2.3 Recommended BIOS/Processor/Memory Test Procedures 33
- 5.3 Material and Recycling Requirements 33

A Mechanical Drawings 35

B Embedded Thermal Solutions 39
- B.1 Performance Targets 39
- B.2 Mechanical Drawings and Supplier Information 40

Figures

2-1 Margin to Thermal Spec (M) 12
2-2 NEBS TCASE Thermal Profile Example....14
2-3 NEBS DTS Thermal Profile Example....15
2-4 Thermal Characterization Parameters 18
3-1 Typical Thermal Profile Graph (Illustration Only) 20
3-2 TCASE Measurement Location 21
4-1 Processor Package Assembly Sketch....27
4-2 Intel® Xeon® Processor E5-2600 v4 Processor Substrate Size 28
4-3 Processor Markings 29
A-1 Package Mechanical Drawing (Sheet 1 of 2)....36
A-2 Package Mechanical Drawing (Sheet 2 of 2)....37
B-1 ATCA Heatsink Performance Curves....40
B-2 ATCA Reference Heatsink Fin and Base (Sheet 1 of 2)....41
B-3 ATCA Reference Heatsink Fin and Base (Sheet 2 of 2)....42

Tables

1-1 Terms and Descriptions 7
1-2 Reference Documents.... 9
2-1 DTS 2.0 Margin From PECI....12
2-2 DTS 2.0 Margin From Processor Register: CSR for PACKAGE_THERM_MARGIN 13
3-1 Intel Xeon Processor E5-2600 v4 Processor Family Thermal Profiles....21
3-2 Intel Xeon Processor E5-4600 v4 Product Family TCASE and DTS Thermal Profiles, and Correction Factors 24
3-3 Intel Xeon Processor E5-1600 v4 Product Family TCASE and DTS Thermal Profiles, and Correction Factors 25
3-4 Embedded Server Processor Thermal Profiles....26
4-1 Processor Loading Specifications....28
4-2 Processor Materials 29
4-3 Load Limits for Package Handling....30
A-1 List of Mechanical Drawings....35
B-1 Reference Thermal Solution Boundary Conditions....39
B-2 High Case Temperature Thermal Profile 40
B-3 Mechanical Drawings List 40

Revision History

Revision Number	Description	Date
001	• Initial Release	March 2016
002	• Added Intel Xeon processor E5-1600 v4 and E5-4600 v4 product families.	June 2016

§

1 Introduction

This document provides specifications and guidelines for the design of thermal and mechanical solutions for the Intel® Xeon® Processor E5 v4 Product Family.

The components and information described in this document include:

- Thermal profiles and other processor specifications and recommendations
- Processor Mechanical load limits

The goals of this document are:

- To assist board and system thermal mechanical designers
- To assist designers and suppliers of processor heatsinks

1.1 Definition of Terms

Table 1-1. Terms and Descriptions (Sheet 1 of 2)

Term	Description
Bypass	Bypass is the area between a passive heatsink and any object that can act to form a duct. For this example, it can be expressed as a dimension away from the outside dimension of the fins to the nearest surface.
DTS	Digital Thermal Sensor reports a relative die temperature as an offset from TCC activation temperature.
FSC	Fan Speed Control
IHS	Integrated Heat Spreader: a component of the processor package used to enhance the thermal performance of the package. Component thermal solutions interface with the processor at the IHS surface.
Square ILM	Independent Loading Mechanism that provides the force needed to seat the 2011-LGA package onto the socket contacts and has an 80 x 80mm heatsink mounting hole pattern.
Narrow ILM	Independent Loading Mechanism that provides the force needed to seat the 2011-LGA package onto the socket contacts and has a 56 × 94mm heatsink mounting hole pattern.
LGA2011-3 Socket	The processor mates with the system board through this surface mount, 2011-contact socket.
PECI	The Platform Environment Control Interface (PECI) is a one-wire interface that provides a communication channel between Intel processor and chipset components to external monitoring devices.
Ψ_{CA}	Case-to-ambient thermal characterization parameter (psi). A measure of thermal solution performance using total package power. Defined as ($T_{CASE} - T_{LA}$) / Total Package Power. Heat source should always be specified for Ψ measurements.

Table 1-1. Terms and Descriptions (Sheet 2 of 2)

Term	Description
Ψ_{CS}	Case-to-sink thermal characterization parameter. A measure of thermal interface material performance using total package power. Defined as $(T_{CASE} - T_S)$ / Total Package Power.
Ψ_{SA}	Sink-to-ambient thermal characterization parameter. A measure of heatsink thermal performance using total package power. Defined as $(T_S - T_{LA})$ / Total Package Power.
T_{CASE}	The case temperature of the processor measured at the geometric center of the topside of the IHS.
T_{CASE_MAX}	The maximum case temperature as specified in a component specification.
TCC	Thermal Control Circuit: Thermal monitor uses the TCC to reduce the die temperature by using clock modulation and/or operating frequency and input voltage adjustment when the die temperature is very near its operating limits.
$T_{CONTROL}$	$T_{CONTROL}$ is a static value below TCC activation used as a trigger point for fan speed control. When DTS > $T_{CONTROL}$, the processor must comply to the thermal profile.
TDP	Thermal Design Power: Thermal solution should be designed to dissipate this target power level. TDP is not the maximum power that the processor can dissipate.
Thermal Monitor	A power reduction feature designed to decrease temperature after the processor has reached its maximum operating temperature.
Thermal Profile	Line that defines case temperature specification of a processor at a given power level.
TIM	Thermal Interface Material: The thermally conductive compound between the heatsink and the processor case. This material fills the air gaps and voids, and enhances the transfer of the heat from the processor case to the heatsink.
T_{LA}	The measured ambient temperature locally surrounding the processor. The ambient temperature should be measured just upstream of a passive heatsink or at the fan inlet for an active heatsink.
T_{SA}	The system ambient air temperature external to a system chassis. This temperature is usually measured at the chassis air inlets.
U	A unit of measure used to define server rack spacing height. 1U is equal to 1.75 in, 2U equals 3.50 in, and so forth.

1.2 Reference Documents

Table 1-2. Reference Documents

Document Title	Document Number
Intel® Xeon® Processor E5-1600/2600/4600 v3 Product Families - Thermal Mechanical Specification and Design Guide (TMSDG)	330786
Intel® Xeon® Processor E5-2600 v4 Product Family Datasheet, Volume One: Electrical	333809
Intel® Xeon® Processor E5-2600 v4 Product Family Datasheet, Volume Two: Registers	333810
Intel® Xeon® Processor E5-2600 v4 Product Family Specification Update	333811

Note: Contact your Intel representative for availability.

§

2 Processor Thermal Specifications and Features

Thermal solutions should be sized such that the processor complies to the T_{CASE} thermal profile all the way up to Thermal Design Power (TDP), because, when all cores are active, a thermal solution sized as such will have the capacity to meet the DTS (Digital Thermal Sensor) thermal profile, by design. When all cores are not active or when Intel Turbo Boost Technology is active, attempting to comply with the DTS thermal profile may drive system fans to speeds higher than the fan speed required to comply with the T_{CASE} thermal profile at TDP.

In cases where thermal solutions are undersized, and the processor does not comply with the T_{CASE} thermal profile at TDP, compliance can occur when the processor power is kept lower than TDP, and the actual T_{CASE} is below the T_{CASE} thermal profile at that lower power.

In most situations, implementation of DTS thermal profile can reduce average fan power and improve acoustics, as compared to $T_{CONTROL}$-based fan speed control. When DTS < $T_{CONTROL}$, the processor is compliant, and T_{CASE} and DTS thermal profiles can be ignored.

2.1 Margin to Thermal Specification (M)

To simplify processor thermal specification compliance, the processor calculates and reports margin to DTS thermal profile (M) using the following method.

Processor reads firmware programmable values:

1. TCC_OFFSET: In-band: TEMPERATURE_TARGET[27:24]. BIOS must write in a value before CPL3.

Processor gathers information about itself:

1. Processor stores the intercept and slope terms (T_{LA} and Ψ_{PA}) from the DTS Thermal Profile for that particular SKU (one-time read only)
2. Processor reads its own energy consumption and calculates power, P
3. Processor reads its own temperature, DTS

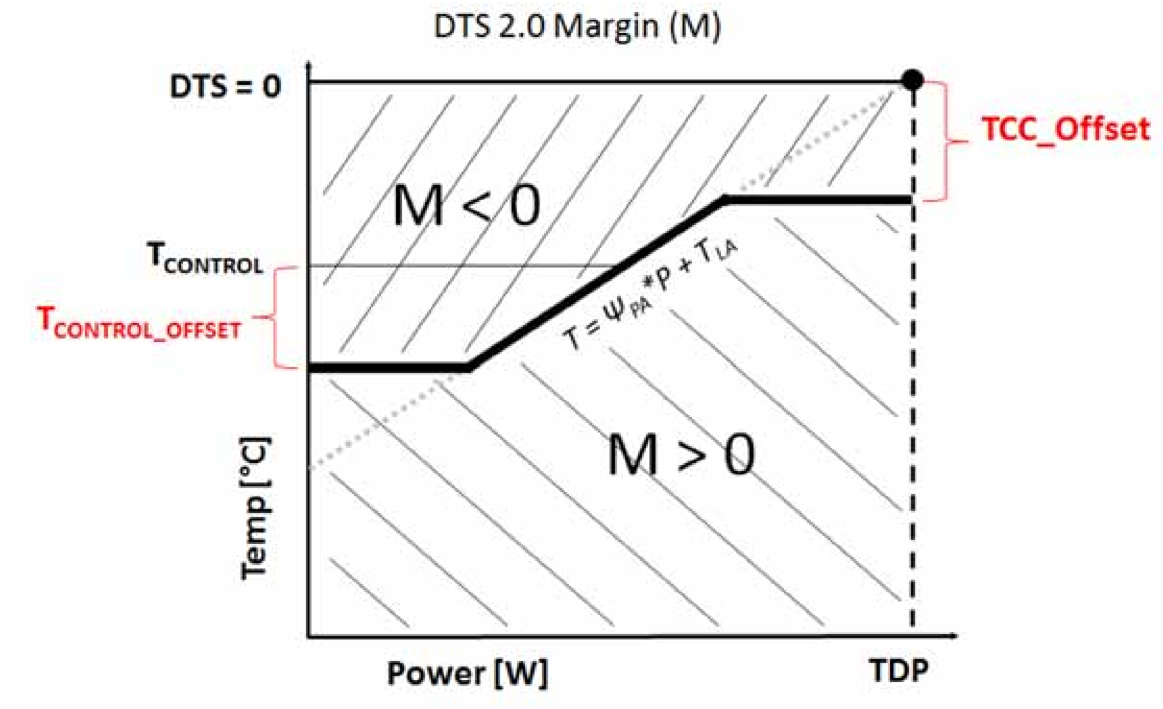
Finally, processor calculates the margin value (M) to the specification (solid black line in the graph below). The PECI command for reading margin (M) is RdPkgConfig(), Index 10.

M < 0 indicates gap to spec, processor needs more cooling (for example, increase fan speed).

M > 0 this indicates margin to spec, processor is sufficiently cooled.

Graphically, this is represented below. $T_{CONTROL\_OFFSET}$ is not writable to a register.

Figure 2-1. Margin to Thermal Spec (M)


DTS 2.0 Margin (M)
DTS = 0
TCC_Offset
M < 0
T_CONTROL
T_CONTROL_OFFSET
T = Ψ_PA * P + T_LA
M > 0
Temp [°C]
Power [W]
TDP

DTS 2.0 processor Margin values can be obtained via PECI or Processor register see documentation below as well as *Intel® Xeon® Processor E5-2600 v4 Product Family Datasheet, Volume Two: Registers*.

Table 2-1. DTS 2.0 Margin From PECI

Service	Index Value (IV) (decimal)	Parameter Value (word)	RdPkgConfig() Data (dword)	WrPkgConfi g() Data (dword)	Description
Thermal Margin	10	0x0000	15:0--Package Temperature margin in 8.8 format, 32:16--Reserved	N/A	Package temperature margin with regards to DTS Thermal Profile. Positive indicates thermal margin, and package is less than DTS thermal profile

Table 2-2. DTS 2.0 Margin From Processor Register: CSR for PACKAGE_THERM_MARGIN

Bus:1 Device:30 Function:0Offset:E0			
Bit	**Attr**	**Default**	**Description**
31:16	RSVD-P	0000h	Reserved--Protected
15:0	R0-V	0000h	THERM_MARGIN--This field provides Platform Firmware with running average of the instantaneous temperature margin above Tspec in 2's complement 8.8 format. This is the recommended field for Platform firmware to use for fan control. When this value is negative, it indicates a firmware must increase the fan speed. With a positive value, firmware may decrease the speed of the fan

Notes:
1. DTS 2.0 Thermal Margin CSR is a mirror of MSR (1A1h) PACKAGE_THERM_MARGIN
2. Refer to *Intel® Xeon® Processor E5-2600 v4 Product Family Datasheet, Volume Two: Registers* for full documentation of MSR and CSR usage and field descriptions

2.2 Embedded Server Thermal Profiles

Network Equipment Building System (NEBS) is the most common set of environmental design guidelines applied to telecommunications equipment. Embedded server SKUs target operation at higher case temperatures and/or NEBS thermal profiles for embedded communications server and storage form factors. The term “Embedded” is used to refer to those segments collectively. Thermal profiles in this section pertain only to those specific Embedded SKUs.

The Nominal Thermal Profile must be used for standard operating conditions or for products that do not require NEBS Level 3 compliance.

The Short-Term Thermal Profile may only be used for short-term excursions to higher ambient operating temperatures, not to exceed 96 hours per instance, 360 hours per year, and a maximum of 15 instances per year, as intended by NEBS Level 3.

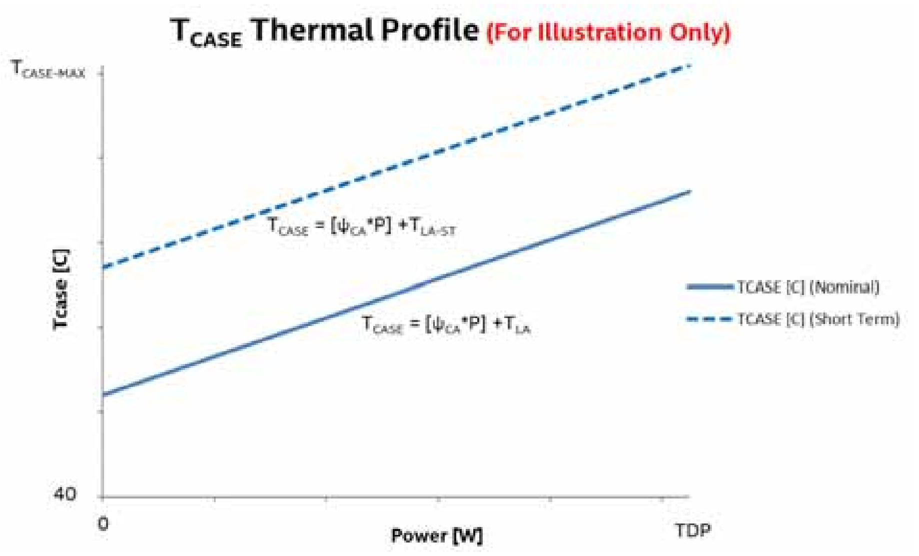
Operation at the Short-Term Thermal Profile for durations exceeding 360 hours per year violate the processor thermal specifications and may result in permanent damage to the processor.

Implementation of the defined thermal profile should result in virtually no TCC activation.

2.2.1 NEBS T_{CASE} Thermal Profile

The NEBS thermal profiles help relieve thermal constraints for short-term NEBS conditions. To help with reliability, the processors must meet the nominal thermal profile under standard operating conditions and can only rise up to the short-term specification for the NEBS excursions as explained in the following figure.

Figure 2-2. NEBS T_{CASE} Thermal Profile Example



Notes:

1. The nominal thermal profile must be used for all normal operating conditions, or for products that do not require NEBS Level 3 compliance.
2. The short-term thermal profile may only be used for short-term excursions to higher ambient operating temperatures, not to exceed 360 hours per year as compliant with NEBS Level 3.
3. Implementation of either thermal profile should result in virtually no TCC activation. Utilization of a thermal solution that exceeds the short-term thermal profile, or which operates at the short-term thermal profile for a duration longer than the limits specified in Note 2 above, do not meet the processor thermal specifications and may result in permanent damage to the processor.

2.2.2 NEBS T_{DTS} Thermal Profile

The thermal solution is expected to be developed in accordance with the T_{CASE} thermal profile. Operational compliance monitoring of thermal specifications and fan speed modulation may be done via the DTS based thermal profile.

These T_{DTS} profiles are fully defined by the simple linear equation:

- $T_{DTS} = PSI_{PA} * P + T_{LA}$

Where:

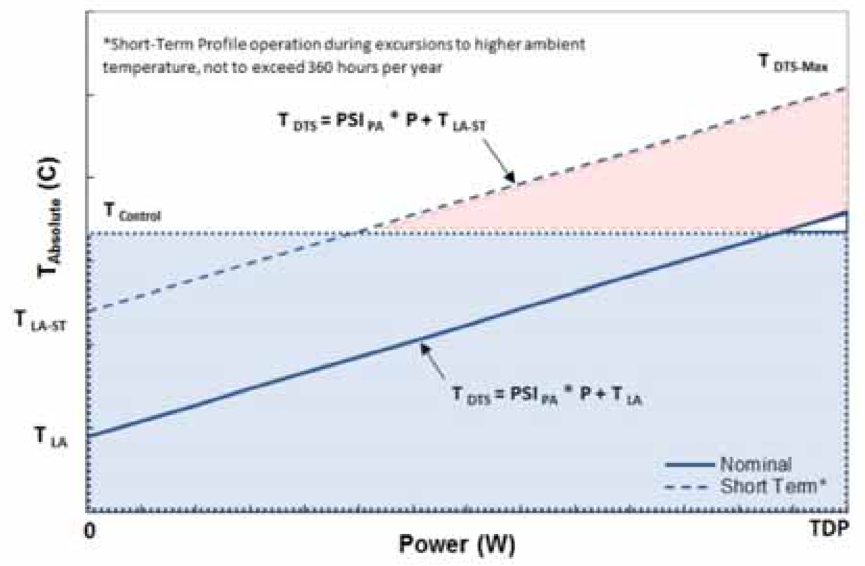
- PSI_{PA} is the Processor-to-Ambient thermal resistance of the processor thermal solution.
- T_{LA} is the Local Ambient temperature for the Nominal thermal profile.
- $T_{LA\text{-}ST}$ designates the Local Ambient temperature for Short-Term operation.
- P is the processor power dissipation.

The figure below illustrates the general form of the resulting linear graph resulting from:

- $T_{DTS} = PSI_{PA} * P + T_{LA}$.

The slope of a DTS profile assumes full fan speed which is not required over much of the power range. $T_{CONTROL}$ is the temperature above which fans must be at maximum speed to meet the thermal profile requirements. $T_{CONTROL}$ is different for each SKU and may be slightly above or below T_{DTS_MAX} of the DTS nominal thermal profile for a particular SKU. At many power levels on most embedded SKUs, temperatures of the nominal profile are less than $T_{CONTROL}$ as indicated by the blue shaded region in the DTS Figure. As a further simplification, operation at DTS temperatures up to $T_{CONTROL}$ is permitted at all power levels. Compliance to the DTS profile is required for any temperatures exceeding $T_{CONTROL}$.

Figure 2-3. NEBS DTS Thermal Profile Example



2.3 Processor Thermal Features

2.3.1 Absolute Processor Temperature

The processor has a software readable field in the TEMPERATURE_TARGET register that contains the minimum temperature at which the Thermal Control Circuit (TCC) will be activated and PROCHOT_N will be asserted.

Intel does not test any third party software that reports absolute processor temperature. As such, Intel cannot recommend the use of software that claims this capability. Since there is part-to-part variation in the TCC (thermal control circuit) activation temperature, use of software that reports absolute temperature may be misleading.

2.3.2 Short Duration TCC Activation

Systems designed to meet thermal capacity may encounter short durations of throttling, also known as TCC activation, especially when running nonsteady processor stress applications. This is acceptable and is functionally within the intended temperature control parameters of the processor. Such short duration TCC activation is not expected to provide noticeable reductions in application performance, and is typically within the normal range of processor to processor performance variation.

2.3.3 Thermal Design Guidelines

2.3.3.1 Intel® Turbo Boost Technology

Intel® Turbo Boost Technology is a feature available on certain Intel® Xeon® Processor E5-2600 v4 Product Family SKUs that opportunistically, and automatically allows the processor to run faster than the marked frequency if the part is operating below certain power and temperature limits. With Turbo Boost enabled, the instantaneous processor power can exceed TDP for short durations resulting in increased performance.

System thermal design should consider the following important parameters (set via BIOS):

- POWER_LIMIT_1 (PL1) = average processor power over a long time window (default setting is TDP)
- POWER_LIMIT_2 (PL2) = average processor power over a short time window above TDP (short excursions). Maximum allowed by the processor is 20% above TDP for all SKUs (1.2 * TDP). Note that actual power will include IMON inaccuracy.
- POWER_LIMIT_1_TIME (Tau) = time constant for the exponential weighted moving average (EWMA) which optimizes performance while reducing thermal risk. (dictates how quickly power decays from its peak)

Please note that although the processor can exceed PL1 (default TDP) for a certain amount of time, the exponential weighted moving average (EWMA) power will never exceed PL1.

A properly designed processor thermal solution is important to maximizing Turbo Boost performance. However, heatsink performance (thermal resistance, Ψ_{CA}) is only one of several factors that can impact the amount of benefit. Other factors are operating environment, workload and system design. With Turbo Mode enabled, the processor may run more consistently at higher power levels, and be more likely to operate above $T_{CONTROL}$, as compared to when Turbo Mode is disabled. This may result in higher acoustics.

2.3.3.2 Thermal Excursion Power

Under fan failure or other anomalous thermal excursions, processor temperature (either T_{CASE} or DTS) may exceed the thermal profile for a duration totaling less than 360 hours per year without affecting long term reliability (life) of the processor. For more typical thermal excursions, Thermal Monitor is expected to control the processor power level as long as conditions do not allow the processor to exceed the temperature at which Thermal Control Circuit (TCC) activation initially occurred.

Under more severe anomalous thermal excursions when the processor temperature cannot be controlled at or below thermal profile by TCC activation, then data integrity is not assured. At some higher thresholds, THERMTRIP_N will enable a shut down in an attempt to prevent permanent damage to the processor.

Thermal test vehicles (TTVs) may be used to check anomalous thermal excursion compliance by ensuring that the processor T_{CASE} value, as measured on the TTV, does not exceed T_{CASE_MAX} at the anomalous power level for the condition of interest, such as fan failure.

A designer can check anomalous power ratio of an individual part by reading register PWR_LIMIT_MISC_INFO and dividing the value of PN_POWER_OF_SKU by the SKU TDP. Please refer to *Intel® Xeon® Processor E5-2600 v4 Product Family Data Sheet, Volume Two: Registers* for details on how to read that specific register.

A designer can check anomalous power ratio of an individual part by reading register PCU_CR_PACKAGE_POWER_SKU.PKG_MIN_PWR[25:19] (MSR 0x614 [MSR_PKG_POWER_INFO]) and dividing the value of PKG_MIN_PWR by the SKU TDP (PKG_TDP bits 15:0). Refer to *Intel® Xeon® Processor E5-2600 v4 Product Family Data Sheet*, *Volume Two: Registers* for details on how to read that specific register.

2.3.3.3 Thermal Characterization Parameters

The case-to-local ambient Thermal Characterization Parameter (Ψ_{CA}) is defined by:
$\Psi_{CA} = (T_{CASE} - T_{LA}) / TDP$

Where:

T_{CASE} = Processor case temperature (°C)

T_{LA} = Local ambient temperature before the air enters the processor heatsink (°C)

TDP = TDP (W) assumes all power dissipates through the integrated heat spreader. This inexact assumption is convenient for heatsink design.

$\Psi_{CA} = \Psi_{CS} + \Psi_{SA}$

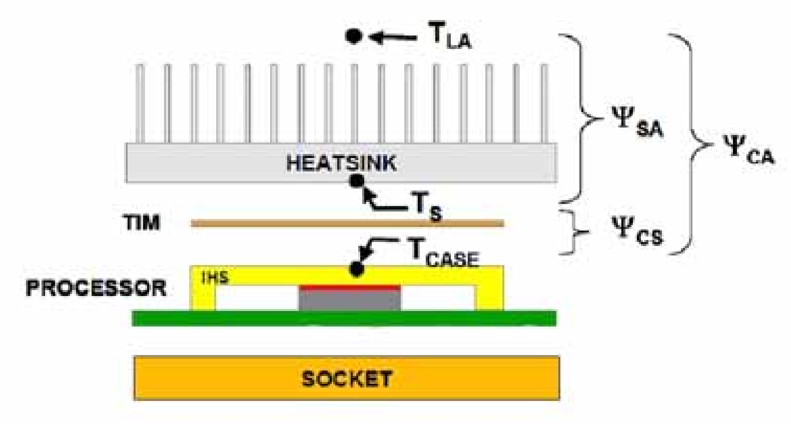
Where:

Ψ_{CS} = Thermal characterization parameter of the TIM (°C/W) is dependent on the thermal conductivity and thickness of the TIM.

Ψ_{SA} = Thermal characterization parameter from heatsink-to-local ambient (°C/W) is dependent on the thermal conductivity and geometry of the heatsink and dependent on the air velocity through the heatsink fins.

The following figure illustrates the thermal characterization parameters.

Figure 2-4. Thermal Characterization Parameters


T_{LA}
Ψ_{SA}
Ψ_{CA}
HEATSINK
T_S
TIM
Ψ_{CS}
T_{CASE}
IHS
PROCESSOR
SOCKET

§

3 Processor Thermal Specifications

The processor requires a thermal solution to maintain temperatures within operating limits. Any attempt to operate the processor outside these limits may result in permanent damage to the processor and potentially other components within the system. Maintaining the proper thermal environment is key to reliable, long-term system operation.

A complete solution includes both component and system level thermal management features. Component level thermal solutions can include active or passive heatsinks attached to the processor integrated heat spreader (IHS). Typical system level thermal solutions may consist of system fans combined with ducting and venting. Details on reference heatsinks developed for the 1S, 2S, and 4S segments of this platform may be found in the *Intel® Xeon® Processor E5-1600 / 2600 / 4600 v3 Product Families - Thermal/Mechanical Specification and Design Guide (TMSDG).*

3.1 Thermal Specifications

To allow optimal operation and long-term reliability of Intel processor-based systems, the processor must remain between the minimum and maximum case temperature (T_{CASE}) specifications as defined in the tables in the following sub-sections. Thermal solutions that do not provide sufficient thermal cooling may affect the long-term reliability of the processor and system.

Thermal profiles ensure adherence to Intel reliability requirements.

Intel assumes specific system boundary conditions (system ambient, airflow, heatsink performance / pressure drop, preheat, etc.) for each processor SKU to develop T_{CASE} and DTS thermal specifications. For servers each processor will be aligned to either 1U or 2U system boundary conditions. Customers can use other boundary conditions (for example a better thermal solution with higher ambient) providing they are compliant to those specifications. Furthermore, implementing a thermal solution that violates the thermal profile for extended periods of time may result in permanent damage to the processor or reduced life. The upper point of the thermal profile consists of the TDP and the corresponding T_{CASE_MAX} value (x = TDP and y = T_{CASE_MAX}) represents a thermal solution design point.

For embedded servers, communications and storage markets, Intel has SKUs that support thermal profiles with nominal and short-term conditions designed to meet NEBS level 3 compliance. For these SKUs, operation at either the nominal or short-term thermal profiles should result in virtually no TCC activation. Thermal profiles for these SKUs are found in this chapter as well.

Intel recommends that thermal solution designs target the Thermal Design Power (TDP). The Adaptive Thermal Monitor feature is intended to help protect the processor in the event that an application exceeds the TDP recommendation for a sustained time period. The Adaptive Thermal Monitor feature must be enabled for the processor to remain within its specifications.

3.2 T_{CASE} and DTS Based Thermal Specifications

To simplify compliance to thermal specifications at processor run time, the processor has a DTS based thermal specification. Digital Thermal Sensor outputs a relative die temperature from TCC activation temperature. T_{CASE}-based specifications are used for heatsink sizing while DTS-based specs are used for acoustic and fan speed optimizations while the server is operating. Some SKUs may share the same T_{CASE} thermal profiles but have distinct DTS thermal profiles.

All thermal profiles, whether based on T_{CASE} or DTS, follow the straight-line equation format namely, $y = mx + b$. Where,

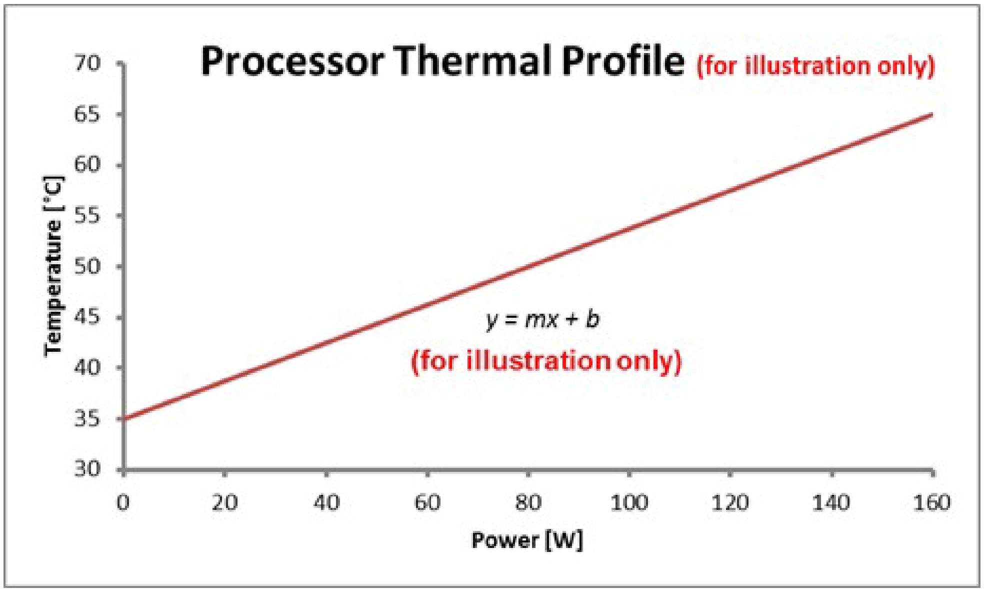
y = temperature (T) in °C

m = slope (Ψ)

x = power (P) in Watts

b = y-intercept (T_{LA}) (LA = local ambient)

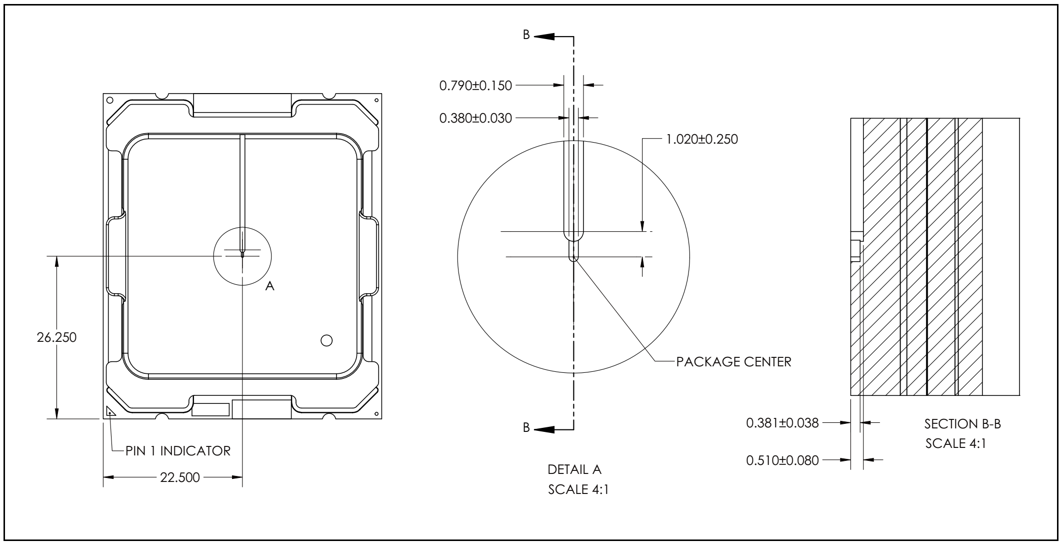
Figure 3-1. Typical Thermal Profile Graph (Illustration Only)



3.3 Thermal Metrology

The minimum and maximum case temperatures (T_{CASE}) specified are measured at the geometric top center of the processor IHS. The following figure illustrates the location where T_{CASE} temperature measurements should be made. The figure also includes geometry guidance for modifying the IHS to accept a thermocouple probe.

Figure 3-2. T_{CASE} Measurement Location


B
0.790±0.150
0.380±0.030
1.020±0.250
A
26.250
PACKAGE CENTER
B
PIN 1 INDICATOR
22.500
DETAIL A
SCALE 4:1
0.381±0.038
0.510±0.080
SECTION B-B
SCALE 4:1

Notes:

3. All values in mm.

3.4 Server Processor Thermal Profiles and Form Factors

Table 3-1. Intel Xeon Processor E5-2600 v4 Processor Family Thermal Profiles (Sheet 1 of 3)

Category	Processor Number	TDP (W)	Core Count	Assumed Heatsink Form Factor	C1E Disable Offset (°C)	$T_{CONTROL}$	Thermal Profiles		DTS max at TDP (°C)
							T_{CASE} (°C)	DTS (°C)	
Advanced	E5-2690 v4	135	14	1U Square	0	10	[0.254*P]+57	[0.365*P]+57	103
	E5-2680 v4	120	14	1U Square	0	10	[0.250*P]+56	[0.367*P]+56	100
	E5-2660 v4	105	14	1U Square	0	10	[0.248*P]+54	[0.362*P]+54	92
	E5-2650 v4	105	12	1U Square	0	10	[0.248*P]+54	[0.390*P]+54	95
Standard	E5-2640 v4	90	10	1U Square	0	10	[0.267*P]+52	[0.444*P]+52	92
	E5-2630 v4	85	10	1U Square	0	10	[0.271*P]+51	[0.459*P]+51	90
	E5-2620 v4	85	8	1U Square	0	10	[0.271*P]+51	[0.459*P]+51	90

Table 3-1. Intel Xeon Processor E5-2600 v4 Processor Family Thermal Profiles (Sheet 2 of 3)

Category	Processor Number	TDP (W)	Core Count	Assumed Heatsink Form Factor	C1E Disable Offset (°C)	$T_{CONTROL}$	Thermal Profiles		DTS max at TDP (°C)
							T_{CASE} (°C)	DTS (°C)	
Basic	E5-2609 v4	85	8	1U Square	0	10	[0.271*P]+51	[0.435*P]+51	88
	E5-2603 v4	85	6	1U Square	0	10	[0.259*P]+51	[0.459*P]+51	90
Segment Optimized	E5-2699 v4	145	22	2U Square	0	10	[0.193*P]+51	[0.290*P]+51	93
	E5-2698 v4	135	20	1U Square	0	10	[0.239*P]+58	[0.351*P]+58	105
	E5-2697A v4	145	16	2U Square	0	10	[0.186*P]+51	[0.290*P]+51	93
	E5-2697 v4	145	18	2U Square	0	10	[0.193*P]+51	[0.324*P]+51	98
	E5-2695 v4	120	18	1U Square	0	10	[0.233*P]+56	[0.350*P]+56	98
	E5-2683 v4	120	16	1U Square	0	10	[0.233*P]+56	[0.383*P]+56	102
Frequency Optimized	E5-2667 v4	135	8	2U Square	0	10	[0.222*P]+50	[0.413*P]+50	102
	E5-2643 v4	135	6	2U Square	0	10	[0.222*P]+49	[0.444*P]+49	101
	E5-2637 v4	135	4	2U Square	0	10	[0.218*P]+49	[0.403*P]+49	97
	E5-2623 v4	85	4	1U Square	0	10	[0.259*P]+51	[0.459*P]+51	90

Table 3-1. Intel Xeon Processor E5-2600 v4 Processor Family Thermal Profiles (Sheet 3 of 3)

Category	Processor Number	TDP (W)	Core Count	Assumed Heatsink Form Factor	C1E Disable Offset (°C)	$T_{CONTROL}$	Thermal Profiles		DTS max at TDP (°C)
							T_{CASE} (°C)	DTS (°C)	
Low Power	E5-2650L v4	65	14	1U Square	0	10	[0.246*P]+48	[0.385*P]+48	73
	E5-2630L v4	55	10	1U Square	0	10	[0.273*P]+47	[0.436*P]+47	71
2S Workstation Only	E5-2687W v4	160	12	WS Passive Tower	0	10	[0.200*P]+44	[0.331*P]+44	97
Off Roadmap	E5-2689 v4	165	10	Unique	0	10	[0.139*P]+29	[0.321*P]+29	82

Notes:

1. These values are specified at VccIN_MAX for all processor frequencies. Systems must be designed to ensure the processor is not subjected to any static Vcc and Icc combination wherein VccIN exceeds VccIN_MAX at a specified Icc. Please refer to the electrical loadline specifications.
2. Thermal Design Power (TDP) should be used as a target for processor thermal solution design. Processor power may exceed TDP for short durations. Please see Section 2.3.3.1, "Intel® Turbo Boost Technology" on page 16.
3. Disabling C1E will result in an automatic reduction of DTSmax so that reliability is still protected. DTSmax will be reduced by the value shown 'C1E Disable Offset'. If thermal design has not been optimized to the reduced DTSmax value, throttling may result. $T_{CONTROL}$ is already an offset to DTSmax, therefore the absolute temp at which the $T_{CONTROL}$ threshold is reached will shift by the same amount.
4. T_{CASE} Minimum is 0°C.
5. "2S Workstation Only" SKU is intended for dual processor workstations only and uses workstation specific use conditions for reliability assumptions.

Table 3-2. Intel Xeon Processor E5-4600 v4 Product Family T_{CASE} and DTS Thermal Profiles, and Correction Factors

Category	Processor Number	TDP (W)	Core Count	C1E Disable Offset (°C)	$T_{CONTROL}$	Thermal Profiles		DTS max at TDP[3] (°C)
						T_{CASE} (°C)	DTS (°C)	
High Performance Dense 4S Glueless	E5-4669 v4	135	22	0	10	[0.239*P]+58	[0.336*P]+58	103
	E5-4667 v4	135	18	0	10	[0.233*P]+57	[0.357*P]+57	103
Frequency Optimized 4S Glueless	E5-4655 v4	135	8	0	10	[0.241*P]+55	[0.420*P]+55	102
	E5-4627 v4	135	10	0	10	[0.237*P]+55	[0.404*P]+55	101
Advanced	E5-4660 v4	120	16	0	10	[0.225*P]+56	[0.358*P]+56	99
	E5-4650 v4	105	14	0	10	[0.248*P]+54	[0.371*P]+54	93
Standard	E5-4640 v4	105	12	0	10	[0.248*P]+54	[0.381*P]+54	94
	E5-4620 v4	105	10	0	10	[0.238*P]+54	[0.390*P]+54	95
Basic	E5-4610 v4	105	10	0	10	[0.238*P]+54	[0.390*P]+54	95

Notes:

1. These values are specified at VccIN_MAX for all processor frequencies. Systems must be designed to ensure the processor is not subjected to any static Vcc and Icc combination wherein VccIN exceeds VccIN_MAX at a specified Icc. Please refer to the electrical loadline specifications.
2. Thermal Design Power (TDP) should be used as a target for processor thermal solution design. Processor power may exceed TDP for short durations.
3. Disabling C1E will result in an automatic reduction of DTSmax so that reliability is still protected. DTSmax will be reduced by the value shown 'C1E Disable Offset'. If thermal design has not been optimized to the reduced DTSmax value, throttling may result. $T_{CONTROL}$ is already an offset to DTSmax, therefore the absolute temp at which the $T_{CONTROL}$ threshold is reached will shift by the same amount.
4. T_{CASE} Minimum is 0°C.
5. All SKUs assume the 1U square heatsink form factor.

Table 3-3. Intel Xeon Processor E5-1600 v4 Product Family T_{CASE} and DTS Thermal Profiles, and Correction Factors

Category	Processor Number	TDP (W)	Core Count	C1E Disable Offset (°C)	$T_{CONTROL}$	Thermal Profiles		DTS max at TDP (°C)
						T_{CASE} (°C)	DTS (°C)	
1S Workstation	E5-1680 v4	140	8	0	10	[0.200*P]+42	[0.421*P]+42	101
	E5-1660 v4	140	8	0	10	[0.200*P]+42	[0.379*P]+42	95
	E5-1650 v4	140	6	0	10	[0.193*P]+42	[0.421*P]+42	101
	E5-1630 v4	140	4	0	10	[0.193*P]+42	[0.379*P]+42	95
	E5-1620 v4	140	4	0	10	[0.193*P]+42	[0.379*P]+42	95
Off Roadmap	E5-1607 v4	140	4	0	10	[0.193*P]+42	[0.371*P]+42	94
	E5-1603 v4	140	4	0	10	[0.193*P]+42	[0.364*P]+42	93

Notes:

1. These values are specified at VccIN_MAX for all processor frequencies. Systems must be designed to ensure the processor is not subjected to any static Vcc and Icc combination wherein VccIN exceeds VccIN_MAX at a specified Icc. Please refer to the electrical loadline specifications.
2. Thermal Design Power (TDP) should be used as a target for processor thermal solution design. Processor power may exceed TDP for short durations.
3. Disabling C1E will result in an automatic reduction of DTSmax so that reliability is still protected. DTSmax will be reduced by the value shown 'C1E Disable Offset'. If thermal design has not been optimized to the reduced DTSmax value, throttling may result. $T_{CONTROL}$ is already an offset to DTSmax, therefore the absolute temp at which the $T_{CONTROL}$ threshold is reached will shift by the same amount.
4. T_{CASE} Minimum is 0°C.
5. All SKUs assume the WS Active Tower heatsink form factor.

3.5 Embedded Server Processor Thermal Profiles

Embedded Server processor SKUs target higher case temperatures and/or Network Equipment Building System (NEBS) thermal profiles for embedded communications server and storage form factors. The following thermal profiles pertain only to those specific SKUs. Network Equipment Building System is the most common set of environmental design guidelines applied to telecommunications equipment in the United States.

Table 3-4. Embedded Server Processor Thermal Profiles

Category	Processor Number	TDP (W)	Core Count	C1E Disable Offset (°C)	$T_{CONTROL}$	Maximum T_{CASE} (ºC)	T_{CASE} Thermal Profile		DTS Thermal Profile	
							T_{CASE} (°C) (Nominal)	T_{CASE} (°C) (Short Term)	T_{DTS} (°C) (Nominal)	T_{DTS} (°C) (Short Term)
4S	E5-4628L v4	75	14	0	20	87	[0.267*P]+52	[0.267*P]+67	[0.387*P]+ 52	[0.387*P]+67
Advanced	E5-2658 v4	105	14	0	20	91	[0.229*P]+52	[0.229*P]+67	[0.333*P]+52	[0.333*P]+67
	E5-2648L v4	75	14	0	20	87	[0.267*P]+52	[0.267*P] +67	[0.387*P]+52	[0.387*P]+67
Standard	E5-2628L v4	75	12	0	20	87	[0.267*P]+52	[0.267*P]+67	[0.400*P]+52	[0.400*P]+67
	E5-2618L v4	75	10	0	20	87	[0.267*P]+52	[0.267*P]+67	[0.440*P]+52	[0.440*P]+67
Basic	E5-2608L v4	50	8	0	10	94	[0.540*P]+52	[0.540*P]+67	[0.700*P]+52	[0.700*P]+67

Notes:

1. These values are specified at VccIN_MAX for all processor frequencies. Systems must be designed to ensure the processor is not subjected to any static Vcc and Icc combination wherein VccIN exceeds VccIN_MAX at a specified Icc. Please refer to the electrical loadline specifications.
2. Thermal Design Power (TDP) should be used as a target for processor thermal solution design at maximum T_{CASE}. Processor power may exceed TDP for short durations. Please see Section 2.3.3.1, "Intel® Turbo Boost Technology" on page 16.
3. Power specifications are defined at all VIDs found in the *Intel® Xeon® Processor E5-2600 v3 Product Family External Design Specification (EDS), Volume Three: Electrical*. Processors may be delivered under multiple VIDs for each frequency.
4. The Nominal Thermal Profile must be used for all normal operating conditions or for products that do not require NEBS Level 3 compliance.
5. The Short-Term Thermal Profile may only be used for short-term excursions to higher ambient operating temperatures, not to exceed 96 hours per instance, 360 hours per year, and a maximum of 15 instances per year, as compliant with NEBS Level 3. Operation at the Short-Term Thermal Profile for durations exceeding 360 hours per year violate the processor thermal specifications and may result in permanent damage to the processor.
6. Minimum T_{CASE} Specification is 0°C.

§

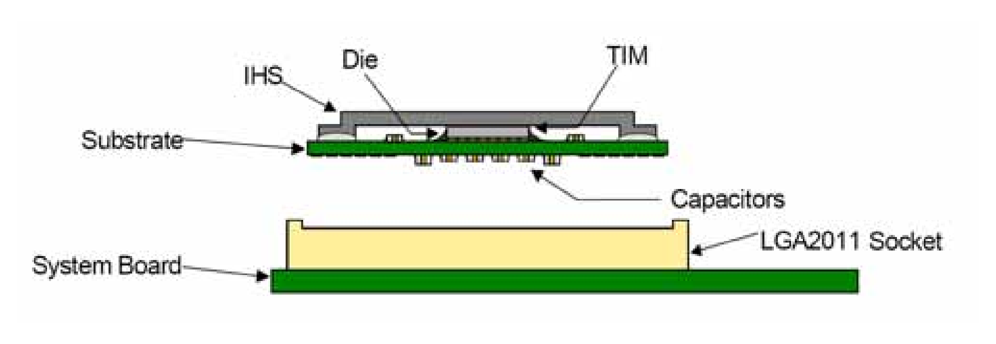
4 Processor Mechanical Specifications

The processor is packaged in a Flip-Chip Land Grid Array package that interfaces with the baseboard via an LGA2011-3 socket. The package consists of a processor mounted on a substrate land-carrier. An integrated heat spreader (IHS) is attached to the package substrate and core and serves as the mating surface for processor component thermal solutions, such as a heatsink. Diagram below shows a sketch of the processor package components and how they are assembled together.

The package components shown below include the following:

1. Integrated Heat Spreader (IHS)
2. Thermal Interface Material (TIM)
3. Processor core (die)
4. Package substrate
5. Capacitors

Figure 4-1. Processor Package Assembly Sketch



Notes:

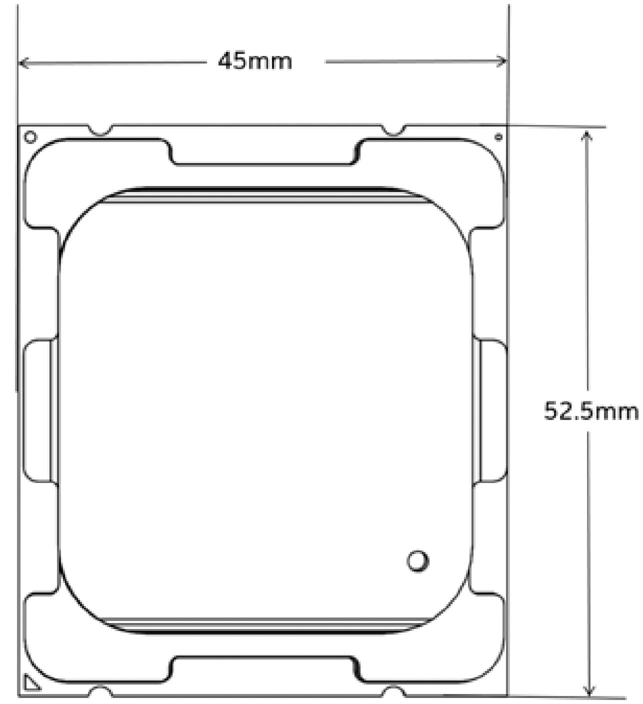
- Socket and baseboard are included for reference and are not part of processor package.
- Processor package land count may be greater than socket contact count.

4.1 Package Size

The processor has a single form factor and is compatible with socket 2011-3 (R3) and the reference ILMs. For details on the socket and ILM, see the *Intel® Xeon® Processor E5-1600/2600/4600 v3 Product Families - Thermal Mechanical Specification and Design Guide (TMSDG).*

Substrate X-Y dimensions for the package are:

Figure 4-2. Intel® Xeon® Processor E5-2600 v4 Processor Substrate Size



4.2 Package Loading Specifications

The following table provides load specifications for the processor package. These maximum limits should not be exceeded during heatsink assembly, shipping conditions, or standard use condition. Exceeding these limits during test may result in component failure. The processor substrate should not be used as a mechanical reference or load bearing surface for thermal solutions.

Table 4-1. Processor Loading Specifications

Parameter	Maximum	Notes
Static Compressive Load	1068 N (240 lbf)	This is the maximum static force that can be applied by the heatsink and Independent Loading Mechanism (ILM).
Dynamic Load	540 N (121 lbf)	Dynamic loading is defined as an 11 ms duration average load superimposed on the static load requirement. This load will be a function of the geometry and mass of the enabling components used.

Notes:
1. These specifications apply to uniform compressive loading in a direction normal to the processor IHS.
2. See the *Intel® Xeon® Processor E5-1600/2600/4600 v3 Product Families - Thermal Mechanical Specification and Design Guide (TMSDG)* for minimum socket load to engage processor within socket.

4.3 Processor Mass Specification

The typical mass of the processor is 45 grams. This mass [weight] includes all the components that are included in the package.

4.4 Processor Materials

The table below lists some of the package components and associated materials.

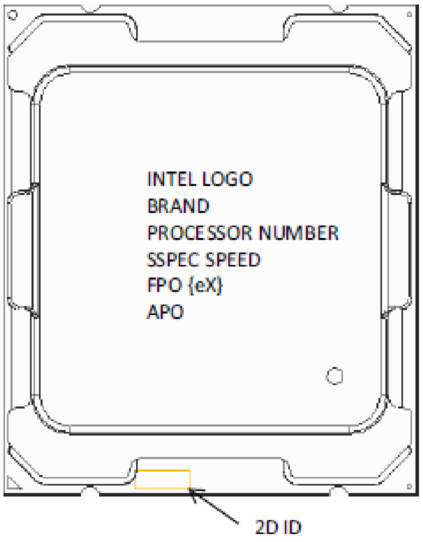
Table 4-2. Processor Materials

Component	Material
Integrated heat Spreader	Nickel Plated Copper
Substrate	Halogen Free, Fiber Reinforced Resin
Substrate lands	Gold Plated Copper

4.5 Processor Markings

The following figure identifies the processor's markings. The figure is a generic representation of text size and placement, and is not to scale.

Figure 4-3. Processor Markings



4.6 Package Handling Guidelines

The processor can be inserted into and removed from a socket 15 times. The following table includes a list of guidelines on package handling in terms of recommended maximum loading on the processor IHS relative to a fixed substrate. These package handling loads may be experienced during heatsink removal.

Table 4-3. Load Limits for Package Handling

Parameter	Maximum Recommended
Shear	356 N (80 lbf)
Tensile	156 N (35 lbf)
Torque	3.6 N-m (31.5 in-lbf)

§

5 Quality, Reliability and Ecological Requirements

5.1 Use Conditions

Intel evaluates reliability performance based on the use conditions (operating environment) of the end product by using acceleration models.

The use condition environment definitions provided in the tables below are based on speculative use condition assumptions, and are provided as examples only.

Based on the system enabling boundary condition, the solder ball temperature can vary and needs to be comprehended for reliability assessment.

Use Environment	Speculative Stress Condition	Example Use Condition	Example 7 yr. Stress Equivalent	Example 10 yr. Stress Equivalent
Slow small internal gradient changes due to external ambient (temperature cycle or externally heated) Fast, large gradient on/off to operating temp. (power cycle or internally heated including power save features)	Temperature Cycle	D T = 35 - 44°C (solder joint)	550-930 cycles Temp Cycle (-25°C to 100°C)	780-1345 cycles Temp Cycle (-25°C to 100°C)
High ambient moisture during low-power state (operating voltage)	THB/HAST	T = 25 -30°C 85%RH (ambient)	110-220 hrs at 110°C 85%RH	145-240 hrs at 110°C 85%RH
High Operating temperature and short duration high temperature exposures	Bake	T = 95 - 105°C (contact)	700 - 2500 hrs at 125°C	800 - 3300 hrs at 125°C

Use Environment	Speculative Stress Condition		Example Use Condition
Shipping and Handling	Mechanical Shock System-level Unpackaged Trapezoidal • 25 g velocity change is based on packaged weight		Total of 12 drops per system: 2 drops per axis ± direction
	Product Weight (lbs)	Non-palletized Product Velocity	
	< 20 lbs	Change (in/sec)	
	20 to > 40	250	
	40 to > 80	225	
	80 to < 100	205	
	100 to < 120	175	
	≥120	145	
		125	
	Change in velocity is based upon a 0.5 coefficient of restitution.		

Use Environment	Speculative Stress Condition		Example Use Condition
Shipping and Handling	Random Vibration System Level Unpackaged 5 Hz to 500 Hz 2.20 g RMS random • 5 Hz @ 0.001 g^2/Hz to 20 Hz @ 0.01 g^2/Hz (slope up) • 20 Hz to 500 Hz @ 0.01 g^2/Hz (flat)	Total per system: 10 minutes per axis 3 axis	

5.2 Intel Reference Component Validation

Intel tests reference components individually and as an assembly on mechanical test boards and assesses performance to the envelopes specified in previous sections by varying boundary conditions.

While component validation shows a reference design is tenable for a limited range of conditions, customers need to assess their specific boundary conditions and perform reliability testing based on their use conditions.

Intel reference components are also used in board functional tests to assess performance for specific conditions.

5.2.1 Board Functional Test Sequence

Each test sequence should start with components (baseboard, heatsink assembly, and so on) that have not previously endured any reliability testing.

Prior to the mechanical shock and vibration test, the units under test should be preconditioned for 72 hours at 45°C. The purpose is to account for load relaxation during burn-in stage.

The test sequence should always start with a visual inspection after assembly, and BIOS/processor/memory test. The stress test should be then followed by a visual inspection and then BIOS/processor/memory test.

5.2.2 Post-Test Pass Criteria Examples

The post-test pass criteria examples are:

1. No significant physical damage to the heatsink and retention hardware.
2. Heatsink remains seated and its bottom remains mated flat against the IHS surface. No visible gap between the heatsink base and processor IHS. No visible tilt of the heatsink with respect to the retention hardware.
3. No signs of physical damage on baseboard surface due to impact of heatsink.
4. No visible physical damage to the processor package.
5. Successful BIOS/Processor/memory test of post-test samples.
6. Thermal compliance testing to demonstrate that the case temperature specification can be met.

5.2.3 Recommended BIOS/Processor/Memory Test Procedures

This test is to ensure proper operation of the product before and after environmental stresses, with the thermal mechanical enabling components assembled. The test shall be conducted on a fully operational baseboard that has not been exposed to any battery of tests prior to the test being considered.

Testing setup should include the following components, properly assembled and/or connected:

- Appropriate system baseboard.
- Processor and memory.
- All enabling components, including socket and thermal solution parts.

The pass criterion is that the system under test shall successfully complete the checking of BIOS, basic processor functions and memory, without any errors. Intel PC Diags is an example of software that can be utilized for this test.

5.3 Material and Recycling Requirements

Material shall be resistant to fungal growth. Examples of non-resistant materials include cellulose materials, animal and vegetable based adhesives, grease, oils, and many hydrocarbons. Synthetic materials such as PVC formulations, certain polyurethane compositions (for example, polyester and some polyethers), plastics which contain organic fillers of laminating materials, paints, and varnishes also are susceptible to fungal growth. If materials are not fungal growth resistant, then MIL-STD-810E, Method 508.4 must be performed to determine material performance.

Cadmium shall not be used in the painting or plating of the socket. CFCs and HFCs shall not be used in manufacturing the socket.

Any plastic component exceeding 25 gm should be recyclable per the European Blue Angel recycling standards.

Supplier is responsible for complying with industry standards regarding environmental care as well as with the specific standards required per supplier's region. More specifically, supplier is responsible for compliance with the European regulations related to restrictions on the use of Lead and Bromine containing flame-retardants.

Legislation varies by geography, European Union (RoHS/WEEE), China, California, and so forth.

The following definitions apply to the use of the terms lead-free, Pb-free, and RoHS compliant.

Halogen flame retardant free (HFR-Free) PCB: Current guidance for the socket pad layout supports FR4 and HFR-Free designs.

Lead-free and Pb-free: Lead has not been intentionally added, but lead may still exist as an impurity below 1000 ppm.

RoHS compliant: Lead and other materials banned in RoHS Directive are either (1) below all applicable substance thresholds as proposed by the EU or (2) an approved/pending exemption applies.

§

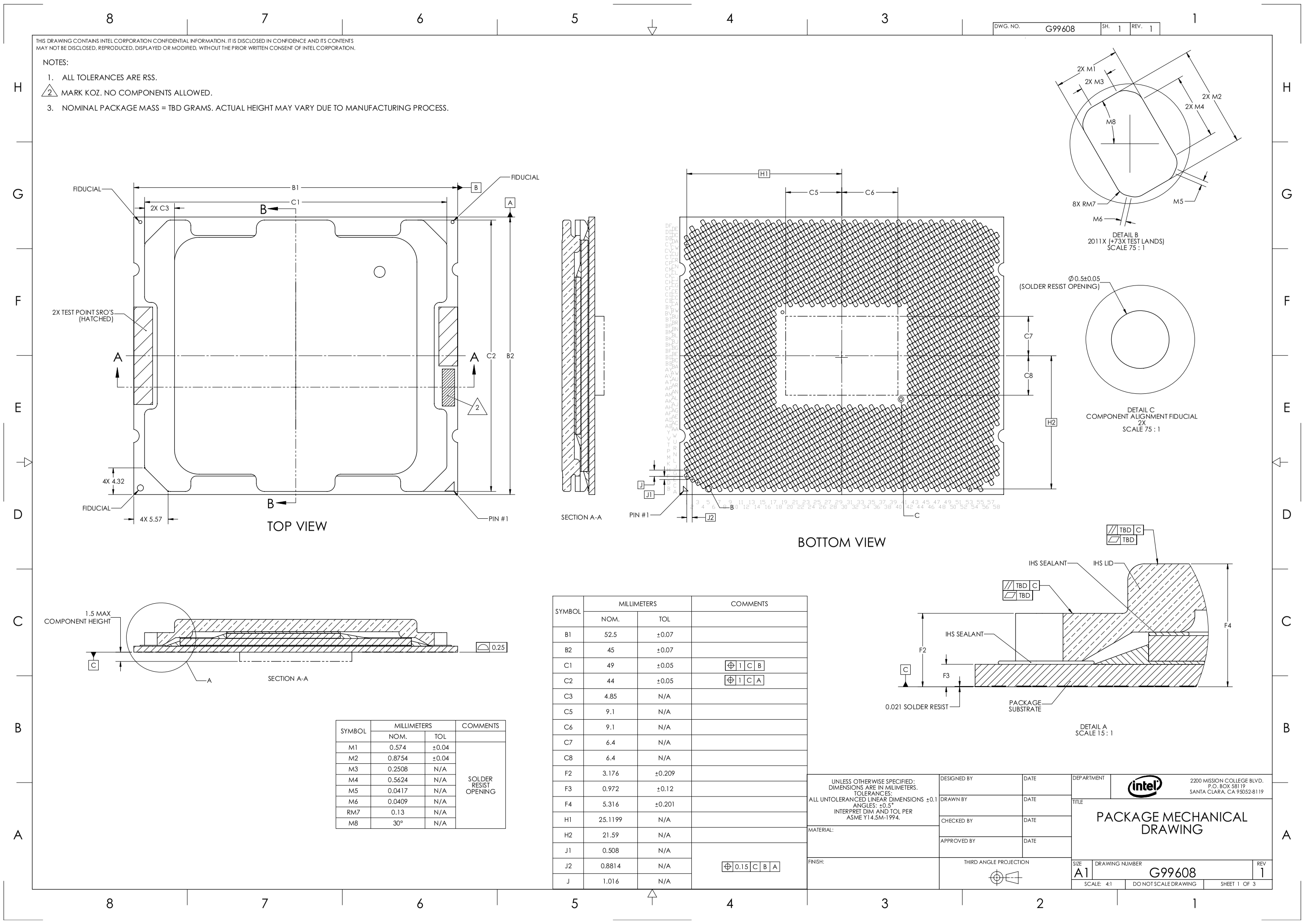
A Mechanical Drawings

The following sections contain mechanical drawings of the processor package geometry.

Table A-1. List of Mechanical Drawings

Figure number	Title
Figure A-1	“Package Mechanical Drawing (Sheet 1 of 2)”
Figure A-2	“Package Mechanical Drawing (Sheet 2 of 2)”

Figure A-1. Package Mechanical Drawing (Sheet 1 of 2)



DWG. NO. G99608 SH. 1 REV. 1
FIDUCIAL
B1
2X C3
C1
B
A
2X TEST POINT SRO'S (HATCHED)
A
A
C2
B2
2
4X 4.32
FIDUCIAL
4X 5.57
B
PIN #1
TOP VIEW
SECTION A-A
H1
C5
C6
C7
C8
H2
J
J1
J2
PIN #1
B
C
BOTTOM VIEW
2X M1
2X M3
2X M2
2X M4
M8
8X RM7
M6
M5
DETAIL B
2011X (+73X TEST LANDS)
SCALE 75 : 1
Ø0.5±0.05
(SOLDER RESIST OPENING)
DETAIL C
COMPONENT ALIGNMENT FIDUCIAL
2X
SCALE 75 : 1
1.5 MAX
COMPONENT HEIGHT
C
0.25
A
SECTION A-A
TBD C
TBD
IHS SEALANT
IHS LID
TBD C
TBD
IHS SEALANT
F2
F3
F4
C
0.021 SOLDER RESIST
PACKAGE SUBSTRATE
DETAIL A
SCALE 15 : 1

THIS DRAWING CONTAINS INTEL CORPORATION CONFIDENTIAL INFORMATION. IT IS DISCLOSED IN CONFIDENCE AND ITS CONTENTS MAY NOT BE DISCLOSED, REPRODUCED, DISPLAYED OR MODIFIED, WITHOUT THE PRIOR WRITTEN CONSENT OF INTEL CORPORATION.

NOTES:

1. ALL TOLERANCES ARE RSS.
2. MARK KOZ. NO COMPONENTS ALLOWED.
3. NOMINAL PACKAGE MASS = TBD GRAMS. ACTUAL HEIGHT MAY VARY DUE TO MANUFACTURING PROCESS.

SYMBOL	MILLIMETERS		COMMENTS
	NOM.	TOL	
M1	0.574	±0.04	SOLDER RESIST OPENING
M2	0.8754	±0.04	
M3	0.2508	N/A	
M4	0.5624	N/A	
M5	0.0417	N/A	
M6	0.0409	N/A	
RM7	0.13	N/A	
M8	30°	N/A	

SYMBOL	MILLIMETERS		COMMENTS
	NOM.	TOL	
B1	52.5	±0.07	
B2	45	±0.07	
C1	49	±0.05	⌖ 1 C B
C2	44	±0.05	⌖ 1 C A
C3	4.85	N/A	
C5	9.1	N/A	
C6	9.1	N/A	
C7	6.4	N/A	
C8	6.4	N/A	
F2	3.176	±0.209	
F3	0.972	±0.12	
F4	5.316	±0.201	
H1	25.1199	N/A	
H2	21.59	N/A	
J1	0.508	N/A	⌖ 0.15 C B A
J2	0.8814	N/A	
J	1.016	N/A	

UNLESS OTHERWISE SPECIFIED:
DIMENSIONS ARE IN MILIMETERS.
TOLERANCES:
ALL UNTOLERANCED LINEAR DIMENSIONS ±0.1
ANGLES: ±0.5°
INTERPRET DIM AND TOL PER
ASME Y14.5M-1994.

MATERIAL:

FINISH:

DESIGNED BY | DATE
DRAWN BY | DATE
CHECKED BY | DATE
APPROVED BY | DATE

THIRD ANGLE PROJECTION

DEPARTMENT

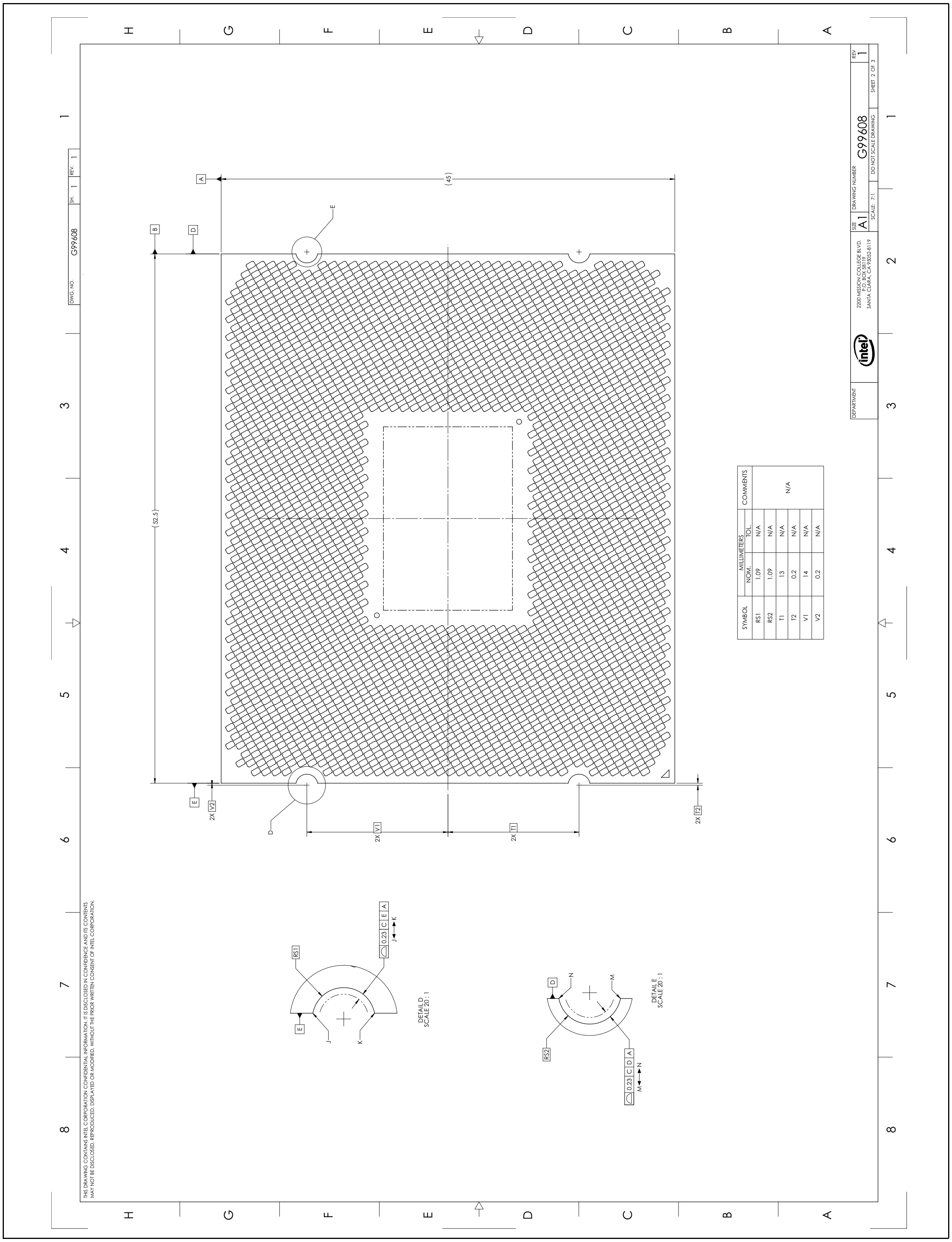
2200 MISSION COLLEGE BLVD.
P.O. BOX 58119
SANTA CLARA, CA 95052-8119

TITLE
PACKAGE MECHANICAL DRAWING

SIZE A1 DRAWING NUMBER G99608 REV 1

SCALE: 4:1 DO NOT SCALE DRAWING SHEET 1 OF 3

Figure A-2. Package Mechanical Drawing (Sheet 2 of 2)


(45)
(52.5)
A
B
D
E
2X V2
2X V1
2X T1
2X T2
DETAIL D
SCALE 20 : 1
DETAIL E
SCALE 20 : 1
RS1
RS2
0.23 C E A
0.23 C D A
J
K
M
N
DWG. NO. G99608 SH. 1 REV. 1
DEPARTMENT
2200 MISSION COLLEGE BLVD.
P.O. BOX 58119
SANTA CLARA, CA 95052-8119
SIZE A1
DRAWING NUMBER G99608
REV 1
SCALE: 7:1
DO NOT SCALE DRAWING
SHEET 2 OF 3
THIS DRAWING CONTAINS INTEL CORPORATION CONFIDENTIAL INFORMATION. IT IS DISCLOSED IN CONFIDENCE AND ITS CONTENTS MAY NOT BE DISCLOSED, REPRODUCED, DISPLAYED OR MODIFIED, WITHOUT THE PRIOR WRITTEN CONSENT OF INTEL CORPORATION.

SYMBOL	MILLIMETERS		COMMENTS
	NOM.	TOL.	
RS1	1.09	N/A	N/A
RS2	1.09	N/A	
T1	13	N/A	
T2	0.2	N/A	
V1	14	N/A	
V2	0.2	N/A	

§

B Embedded Thermal Solutions

Embedded Server SKUs target higher case temperatures and/or NEBS thermal profiles for embedded communications server and storage form factors. This section describes reference heatsinks for NEBS compliant ATCA (Advanced Telecommunications Computing Architecture) systems. These higher case temperature processors are good for any form factor that needs to meet NEBS requirements.

B.1 Performance Targets

Table B-1 provides boundary conditions and performance targets for 1U and ATCA heatsinks. These values are used to generate processor thermal specifications and to provide guidance for heatsink design.

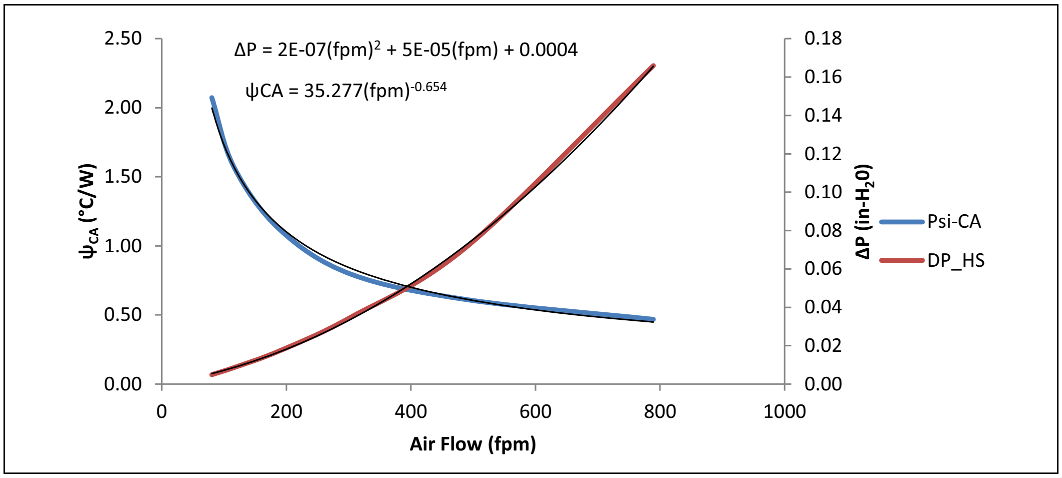
Table B-1. Reference Thermal Solution Boundary Conditions

TDP	Heatsink Form Factor[4,5]	Ψ_{CA}[2] (C/W)	T_{LA}[1] (Nominal / Short-term)	Heat sink Volumetric[3] (mm)
75W	ATCA	0.267	52/67	91.5 x 91.5 x 11.8mm
105W	1U	0.229	52/67	91.5 x 91.5 x 25.5mm

Notes:
1. Local ambient temperature of the air entering the heat sink.
2. Max target (mean + 3 sigma + offset) for thermal characterization parameter Section 2.3.3.3, “Thermal Characterization Parameters.”
3. Dimensions of heat sink do not include socket or processor.
4. All heat sinks are Non-Direct Chassis Attach (DCA)
5. See the *Intel® Xeon® Processor E5-1600/2600/4600 v3 Product Families - Thermal Mechanical Specification and Design Guide (TMSDG)* for standard 1U solutions that do not need to meet NEBS.

Detailed drawings for the ATCA reference heat sink can be found in Section B.2. Table B-1 above specifies Ψ_{CA} and pressure drop targets and Figure B-1 below shows Ψ_{CA} and pressure drop for the ATCA heatsink versus the airflow in linear feet per minute (fpm) provided. Best-fit equations are provided to prevent errors associated with reading the graph.

Figure B-1. ATCA Heatsink Performance Curves



Notes:
1. Performance shown based on a Intel Xeon processor E5 v4 compatible Thermal Test Vehicle (TTV).

B.2 Mechanical Drawings and Supplier Information

The part number below represents Intel reference designs for an ATCA reference heatsink. Customer implementation of these components may be unique and require validation by the customer. Customers can obtain these components directly from the following supplier.

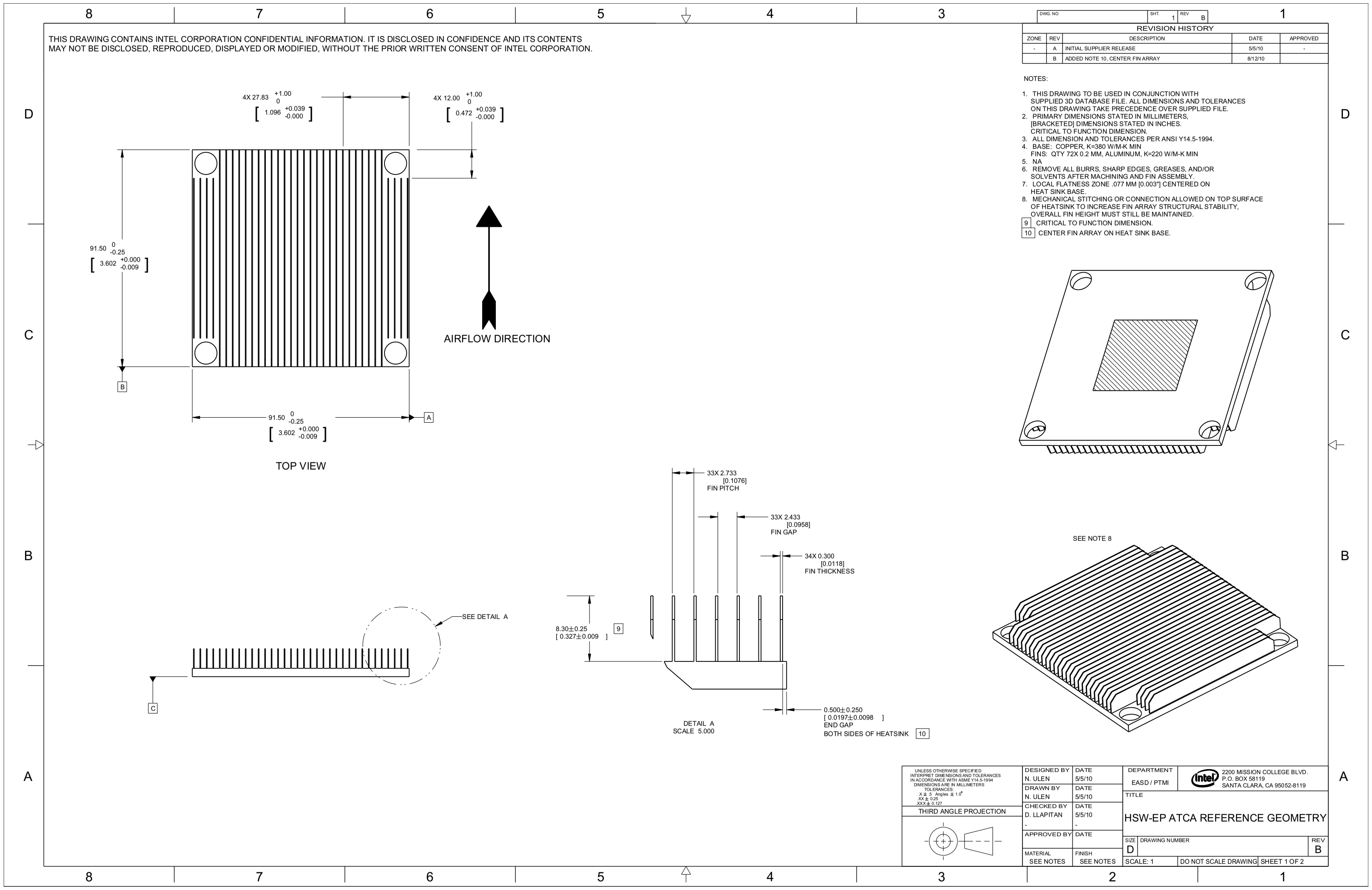
Table B-2. High Case Temperature Thermal Profile

Component	Description	Supplier PN	Supplier Contact Info
ATCA Reference Heatsink Intel P/N: J14286-001	ATCA Copper fin, Copper base, Heat Sink Assembly	1A01YY100	Foxconn/FTC Technology, Inc. www.foxconn.com

Table B-3. Mechanical Drawings List

Figure Number	Title
Figure B-2	ATCA Reference Heatsink Fin and Base (Sheet 1 of 2)
Figure B-3	ATCA Reference Heatsink Fin and Base (Sheet 2 of 2)

Figure B-2. ATCA Reference Heatsink Fin and Base (Sheet 1 of 2)


THIS DRAWING CONTAINS INTEL CORPORATION CONFIDENTIAL INFORMATION. IT IS DISCLOSED IN CONFIDENCE AND ITS CONTENTS MAY NOT BE DISCLOSED, REPRODUCED, DISPLAYED OR MODIFIED, WITHOUT THE PRIOR WRITTEN CONSENT OF INTEL CORPORATION.
4X 27.83 +1.00 0 [1.096 +0.039 -0.000]
4X 12.00 +1.00 0 [0.472 +0.039 -0.000]
91.50 0 -0.25 [3.602 +0.000 -0.009]
91.50 0 -0.25 [3.602 +0.000 -0.009]
AIRFLOW DIRECTION
TOP VIEW
A
B
C
SEE DETAIL A
33X 2.733 [0.1076] FIN PITCH
33X 2.433 [0.0958] FIN GAP
34X 0.300 [0.0118] FIN THICKNESS
8.30±0.25 [0.327±0.009] 9
0.500±0.250 [0.0197±0.0098] END GAP BOTH SIDES OF HEATSINK 10
DETAIL A SCALE 5.000
SEE NOTE 8
8
7
6
5
4
3
2
1
D
C
B
A
DWG. NO
SHT. 1
REV B

REVISION HISTORY

ZONE	REV	DESCRIPTION	DATE	APPROVED
-	A	INITIAL SUPPLIER RELEASE	5/5/10	-
	B	ADDED NOTE 10, CENTER FIN ARRAY	8/12/10	

NOTES:

1. THIS DRAWING TO BE USED IN CONJUNCTION WITH SUPPLIED 3D DATABASE FILE. ALL DIMENSIONS AND TOLERANCES ON THIS DRAWING TAKE PRECEDENCE OVER SUPPLIED FILE.
2. PRIMARY DIMENSIONS STATED IN MILLIMETERS, [BRACKETED] DIMENSIONS STATED IN INCHES. CRITICAL TO FUNCTION DIMENSION.
3. ALL DIMENSION AND TOLERANCES PER ANSI Y14.5-1994.
4. BASE: COPPER, K=380 W/M-K MIN
FINS: QTY 72X 0.2 MM, ALUMINUM, K=220 W/M-K MIN
5. NA
6. REMOVE ALL BURRS, SHARP EDGES, GREASES, AND/OR SOLVENTS AFTER MACHINING AND FIN ASSEMBLY.
7. LOCAL FLATNESS ZONE .077 MM [0.003"] CENTERED ON HEAT SINK BASE.
8. MECHANICAL STITCHING OR CONNECTION ALLOWED ON TOP SURFACE OF HEATSINK TO INCREASE FIN ARRAY STRUCTURAL STABILITY, OVERALL FIN HEIGHT MUST STILL BE MAINTAINED.

9 CRITICAL TO FUNCTION DIMENSION.

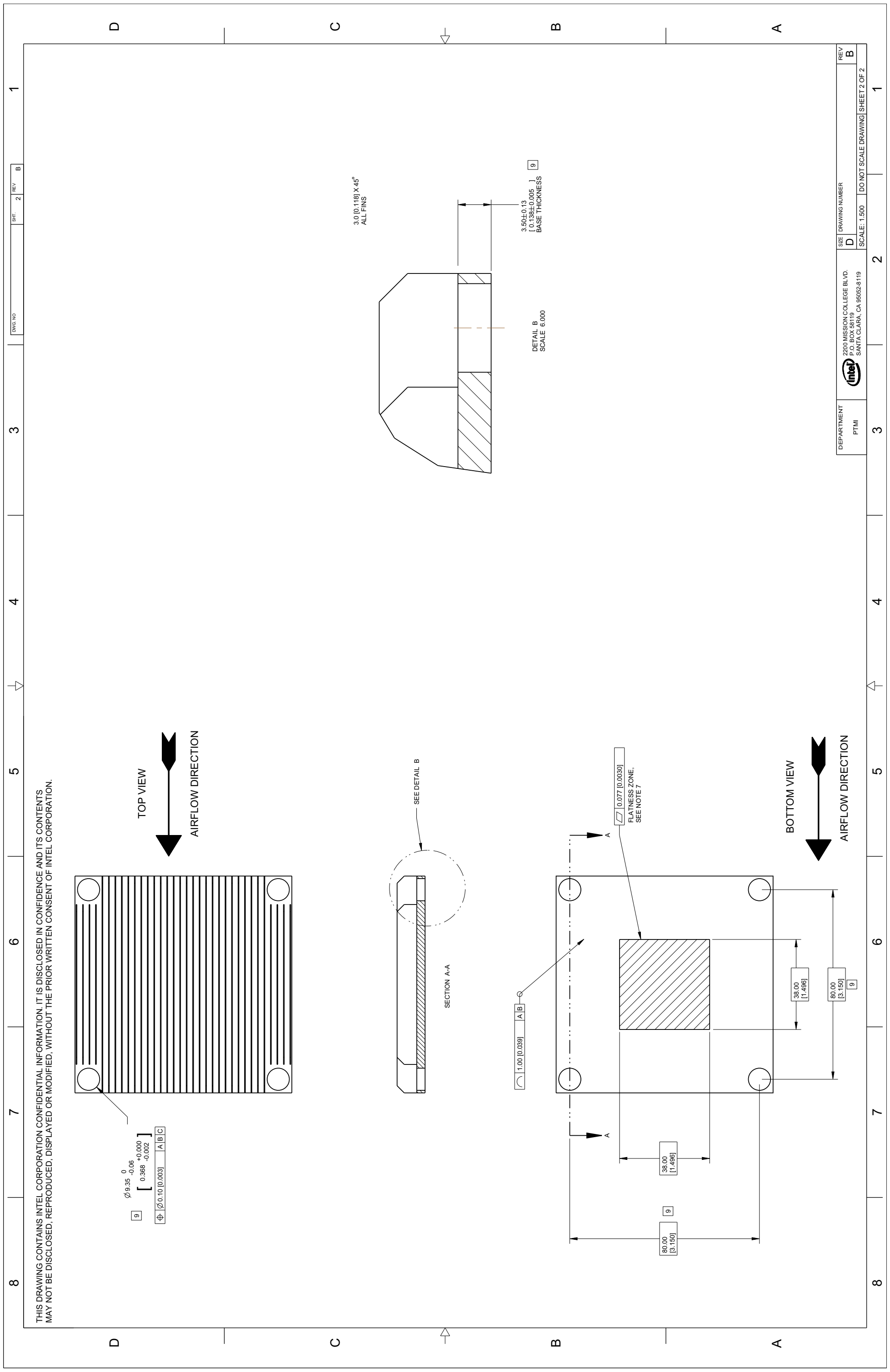
10 CENTER FIN ARRAY ON HEAT SINK BASE.

UNLESS OTHERWISE SPECIFIED
INTERPRET DIMENSIONS AND TOLERANCES
IN ACCORDANCE WITH ASME Y14.5-1994
DIMENSIONS ARE IN MILLIMETERS
TOLERANCES:
.X ± .5 Angles ± 1.0°
.XX ± 0.25
.XXX ± 0.127

THIRD ANGLE PROJECTION

DESIGNED BY N. ULEN	DATE 5/5/10	DEPARTMENT EASD / PTMI	2200 MISSION COLLEGE BLVD. P.O. BOX 58119 SANTA CLARA, CA 95052-8119
DRAWN BY N. ULEN	DATE 5/5/10	TITLE HSW-EP ATCA REFERENCE GEOMETRY	
CHECKED BY D. LLAPITAN -	DATE 5/5/10 -		
APPROVED BY	DATE	SIZE D	DRAWING NUMBER · REV B
MATERIAL SEE NOTES	FINISH SEE NOTES	SCALE: 1	DO NOT SCALE DRAWING · SHEET 1 OF 2

Figure B-3. ATCA Reference Heatsink Fin and Base (Sheet 2 of 2)


D
C
B
A
1
2
3
4
5
6
7
8
3.0 [0.118] X 45°
ALL FINS
3.50±0.13
[0.138±0.005]
BASE THICKNESS
9
DETAIL B
SCALE 6.000
DEPARTMENT
PTMI
2200 MISSION COLLEGE BLVD.
P.O. BOX 58119
SANTA CLARA, CA 95052-8119
SIZE
D
DRAWING NUMBER
REV
B
SCALE: 1.500
DO NOT SCALE DRAWING
SHEET 2 OF 2
DWG. NO
SHT
2
REV
B
TOP VIEW
AIRFLOW DIRECTION
SEE DETAIL B
SECTION A-A
0.077 [0.0030]
FLATNESS ZONE,
SEE NOTE 7
A
A
BOTTOM VIEW
AIRFLOW DIRECTION
38.00
[1.496]
80.00
[3.150]
9
1.00 [0.039] A B
38.00
[1.496]
80.00
[3.150]
9
Ø9.35 0 -0.06
[0.368 +0.000 -0.002]
9
Ø0.10 [0.003] A B C
THIS DRAWING CONTAINS INTEL CORPORATION CONFIDENTIAL INFORMATION. IT IS DISCLOSED IN CONFIDENCE AND ITS CONTENTS
MAY NOT BE DISCLOSED, REPRODUCED, DISPLAYED OR MODIFIED, WITHOUT THE PRIOR WRITTEN CONSENT OF INTEL CORPORATION.

§