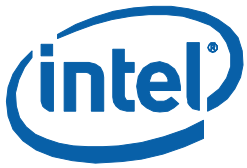

Intel® Atom™ Processor Z5xx Series

Datasheet Addendum and Specification Update Addendum

Intel® Atom™ Processor Z530P, Z520PT, Z510P, and Z510PT on 45 nm process technology

January 2011

Document Number: 321423-002

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Revision History

Revision Number	Description	Revision Date
001	• Initial release	March 2009

002	• Updated Max values in Table 3
	  • V_{CC}, V_{CCP}, V_{CCPC6} from 1.10 to 1.35
	  • Vin AGTL+ from 1.10 to 1.35
	  • Vin Asynch_CMOS from 1.10 to 1.35
		January 2011

§

1 Introduction

The Intel® Atom™ processor Z5xxPx series is built on 45-nanometer process technology — part of the first generation of low-power IA-32 architecture chips specially designed for a new class of Embedded products. It builds off the same core found in the smaller package Intel® Atom™ processor Z5xx series, but with a larger package that's easier to design with. The "P" extension to the part number denotes that the part has a larger package than its small form factor counterpart. The Intel® Atom™ processor Z5xxPx series also adds two new processors with Industrial Temperature (IT) support covering a wider range of temperature conditions. The "T" extension to the part number denotes that the part supports the Industrial Temperature range (-40° to +85°C). The Intel® Atom™ processor Z5xxPx series supports the Intel® System Controller Hub US15WPx, a single-chip System Controller Hub (SCH) component designed for low-power and ease of design. The SCH part number extensions follow the same pattern as the processor such that the "P" extension denotes larger package, and the "T" extension denotes Industrial Temperature support. Information presented in this document supplements or overrides the *Intel® Atom™ Processor Z5xx Series Datasheet* and *Specification Update* specific to the Intel® Atom™ processor Z5xxPx series.

Note: In this document, the Intel® Atom™ processor Z5xxPx series is referred to as the processor and Intel® System Controller Hub US15WPx is referred to as the SCH or chipset.

1.1 Major Features

Key features of this processor are:

- New single-core processor based on Intel® Atom™ microarchitecture
- Support for IA-32 architecture
- On die 512-kB, 8-way L2 cache
- On die, primary 32-kB instructions cache and 24-kB write-back data cache
- 100-MHz and 133-MHz Source-Synchronous front side bus (FSB)
  - 100 MHz: Intel® Atom™ processor Z510P, Z510PT
  - 133 MHz: Intel® Atom™ processor Z530P, Z520PT
- Supports new CMOS FSB signaling for reduced power
- FSB Lane Reversal for flexible routing
- Supports Hyper-Threading Technology† (HTT)
- Intel® Streaming SIMD Extensions 2 and 3 (Intel® SSE2 and Intel® SSE3) and Supplemental Streaming SIMD Extensions 3 (SSSE3) support
- Micro-FCBGA8 packaging technologies
- Thermal management support via TM1 and TM2
- Advanced power management features including Enhanced Intel SpeedStep® Technology

- Supports C0/C1(e)/C2(e)/C4(e)
- New Deep Power Down Technology (C6)
- L2 Dynamic Cache Sizing
- New Split-VTT support for lowest processor power state
- Execute Disable Bit support for enhanced security

1.2 Terminology

Term	Definition
#	A "#" symbol after a signal name refers to an active low signal, indicating a signal is in the active state when driven to a low level. For example, when RESET# is low, a reset has been requested. Conversely, when NMI is high, a non-maskable interrupt has occurred. In the case of signals where the name does not imply an active state but describes part of a binary sequence (such as address or data), the "#" symbol implies that the signal is inverted. For example, D[3:0] = "HLHL" refers to a hex 'A', and D[3:0]# = "LHLH" also refers to a hex "A" (H= High logic level, L= Low logic level).
Front Side Bus (FSB)	Refers to the interface between the processor and system core logic (also known as the SCH chipset components).
AGTL+	Advanced Gunning Transceiver Logic. Used to refer to Assisted GTL+ signaling technology on some Intel processors.
CMOS	Complementary Metal-Oxide Semiconductor.
CT	Commercial Temperature – 0 to 70°C ambient
IT	Industrial Temperature – AEC-Q100 Grade 3: -40 to 85°C ambient
Storage Conditions	Refers to a non-operational state. The processor may be installed in a platform, in a tray, or loose. Processors may be sealed in packaging or exposed to free air. Under these conditions, processor landings should not be connected to any supply voltages, have any I/Os biased, or receive any clocks. Upon exposure to "free air" (i.e., unsealed packaging or a device removed from packaging material) the processor must be handled in accordance with moisture sensitivity labeling (MSL) as indicated on the packaging material.
Enhanced Intel SpeedStep® Technology	Technology that provides power management capabilities to low power devices.
Processor Core	Processor core die with integrated L1 and L2 cache. All AC timing and signal integrity specifications are at the pads of the processor core.
Intel® 64 Technology	64-bit memory extensions to the IA-32 architecture.

Term	Definition
TDP	Thermal Design Power
V_{CC}	The processor core power supply
VR	Voltage Regulator
V_{SS}	The processor ground
V_{CC}HFM	V_{CC} at Highest Frequency Mode (HFM).
V_{CC}LFM	V_{CC} at Lowest Frequency Mode (LFM).
$V_{CC,BOOT}$	Default V_{CC} Voltage for Initial Power Up.
V_{CCP}	AGTL+ Termination Voltage.
V_{CCPC6}	AGTL+ Termination Voltage.
V_{CCA}	PLL Supply voltage.
$V_{CCDPPWDN}$	V_{CC} at Deep Power Down Technology (C6).
$V_{CCDPRSLP}$	V_{CC} at Deeper Sleep (C4).
I_{CCDES}	I_{CC} for Intel® Atom™ processor Z5xxPx series Recommended Design Target (Estimated).
I_{AH}	I_{CC} Auto-Halt
I_{SGNT}	I_{CC} Stop-Grant.
I_{DSLP}	I_{CC} Deep Sleep.
$dI_{CC/dt}$	V_{CC} Power Supply Current Slew Rate at Processor Package Pin (Estimated).
I_{CCA}	I_{CC} for V_{CCA} Supply.
P_{AH}	Auto Halt Power.
P_{SGNT}	Stop Grant Power.
P_{DPRSLP}	Deeper Sleep Power.
P_{DC6}	Intel® Deep Power Down Technology (C6).
T_J	Junction Temperature.

1.3 References - Update

Material and concepts available in the following documents may be beneficial when reading this document.

Table 1. References

Document	Document Number
Intel® Atom™ Processor Z5xx Series Datasheet	319535
Intel® Atom™ Processor, Z5xx Series Specification Update	319536
Intel® System Controller Hub (Intel® SCH) Datasheet	319537
Intel® System Controller Hub (Intel® SCH) Specification Update	319538
Intel® System Controller Hub (Intel® SCH) Datasheet Addendum for US15WP and US15WPT	321422
Intel® 64 and IA-32 Architectures Software Developer's Manuals *Volume 1: Basic Architecture* *Volume 2A: Instruction Set Reference, A-M* *Volume 2B: Instruction Set Reference, N-Z* *Volume 3A: System Programming Guide* *Volume 3B: System Programming Guide*	http://www.intel.com/products/processor/manuals/index.htm
AP-485, Intel® Processor Identification and CPUID Instruction Application Note	http://www.intel.com/Assets/PDF/appnote/241618.pdf

1.4 Component Marking Information

The Intel® Atom™ processor Z5xxPx series can be identified by the following component markings.

Figure 1. Intel® Atom™ processor Z5xxPx series Package Marking

GRP1LINE1: INTEL {M}©'07

GRP1LINE2: <S-SPEC> <FSB Speed>

GRP1LINE3: <Product Number>

GRP1LINE4: <FPO> {e1}

Table 2. Identification Table for Intel® Atom™ processor Z5xxPx series

	S-Spec	Product Stepping	TDP[2]	FSB Freq	CPU Signature	Core Speed		Qual Temp[3,4]	MM	Product Number
						HFM	LFM			
Z510PT	SLGPR[1]	C0	2.2W	400 MHz	000106C2h	1.1 GHz	600 MHz	Ind.	901877	CH80566EC005DT
Z510P	SLGPQ[1]	C0	2.2W	400 MHz	000106C2h	1.1 GHz	600 MHz	Comm.	901876	CH80566EC005DW
Z520PT	SLGPP	C0	2.2W	533 MHz	000106C2h	1.33 GHz	800 MHz	Ind.	901875	CH80566EE014DT
Z530P	SLGPN	C0	2.2W	533 MHz	000106C2h	1.6 GHz	800 MHz	Comm.	901873	CH80566EE025DW

NOTES:

1. 1.1 GHz SKUs differ from the small package Z510 in that they enable HT. Otherwise, they are functionally identical.
2. All parts have a TDP of 2.2W with Hyper-Threading Technology (HT Technology) enabled, and 2W with HT disabled.
3. Ind. = Industrial Temperature (IT). -40˚C to 85˚C ambient.
4. Comm. = Commercial Temperature (CT). 0˚C to 70˚C ambient.§

2 Electrical Specifications

This chapter contains differences and clarifications to the *Intel® Atom™ Processor Z5xx Series Datasheet* document's Electrical Specifications chapter. This chapter covers signal group descriptions, absolute maximum ratings, voltage identification, DC specifications and power sequencing.

2.1 Maximum Ratings

Table 3 specifies absolute maximum and minimum ratings. Within functional operation limits, functionality and long-term reliability can be expected.

At conditions outside functional operation condition limits, but within absolute maximum and minimum ratings, neither functionality nor long term reliability can be expected. If a device is returned to conditions within functional operation limits after having been subjected to conditions outside these limits, but within the absolute maximum and minimum ratings, the device may be functional, but with its lifetime degraded depending on exposure to conditions exceeding the functional operation condition limits.

At conditions exceeding absolute maximum and minimum ratings, neither functionality nor long term reliability can be expected. Moreover, if a device is subjected to these conditions for any length of time then, when returned to conditions within the functional operating condition limits, it will either not function or its reliability will be severely degraded.

Although the processor contains protective circuitry to resist damage from static electric discharge, precautions should always be taken to avoid high static voltages or electric fields.

Table 3. Processor Absolute Maximum Ratings[1]

Symbol	Parameter	Min	Max	Unit
$T_{STORAGE}$	Processor Storage Temperature	See *Section 4.3*		
V_{CC}, V_{CCP}, V_{CCPC6}	Any Processor Supply Voltage with Respect to V_{SS}	-0.3	1.35	V
V_{CCA}	PLL power supply	-0.3	1.575	V
Vin AGTL+	AGTL+ Buffer DC Input Voltage with Respect to V_{SS}	-0.1	1.35	V
Vin Asynch_CMOS	CMOS Buffer DC Input Voltage with Respect to V_{SS}	-0.1	1.35	V

NOTES:
1. For functional operation, all processor electrical, signal quality, mechanical and thermal specifications must be satisfied.

2.2 Processor DC Specifications

The information provided in this section supersedes the information in the Processor DC Specifications chapter in the *Intel® Atom™ Processor Z5xx Series Datasheet*, for the processor SKUs listed. Information not specifically called out for the larger package SKU may be assumed to be identical to the information for the corresponding smaller package SKU in the aforementioned datasheet.

NOTE: Unless specifically mentioned here, no significant difference in the Processor DC Specifications was measured at the higher T_J=110° C for the Z520PT and Z510PT SKUs.

Table 4. Voltage and Current Specifications for the Intel® Atom™ Processor Z520PT and Z510PT

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{CC}HFM	V_{CC} at Highest Frequency Mode (HFM)	0.90	–	1.10	V	1,2
V_{CC}LFM	V_{CC} at Lowest Frequency Mode (LFM)	0.90	–	0.90	V	1,2

NOTES:
1. Each processor is programmed with a maximum valid voltage identification value (VID), which is set at manufacturing and can not be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. Note that this differs from the VID employed by the processor during a power management event (Thermal Monitor 2, Enhanced Intel SpeedStep® Technology, or Enhanced Halt State).
2. The voltage specifications are assumed to be measured across VCC_SENSE and VSS_SENSE pins at socket with a 100-MHz bandwidth oscilloscope, 1.5-pF maximum probe capacitance, and 1-MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled in the scope probe.

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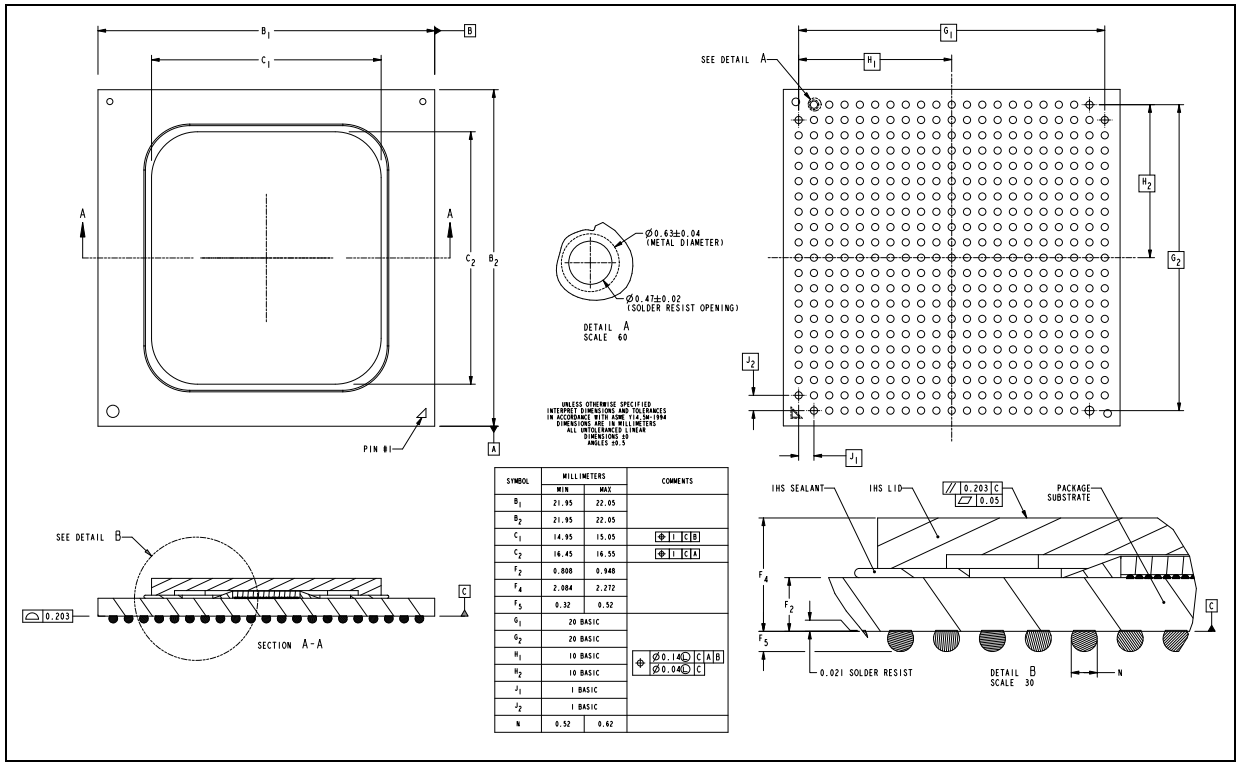
3 Package Mechanical Specifications and Pin Information

This chapter provides the package specifications, pinout assignments, and signal description. It replaces the *Package Mechanical Specifications and Pin Information* chapter of the *Intel® Atom™ Processor Z5xx Series Datasheet*.

3.1 Package Mechanical Specifications

The processor will be available in a 437 pin FCBGA8 package with an Integrated Heat Spreader (IHS).

Figure 2. Package Mechanical Drawing (IHS)



SYMBOL	MILLIMETERS MIN	MILLIMETERS MAX	COMMENTS
B_1	21.95	22.05	
B_2	21.95	22.05	
C_1	14.95	15.05	
C_2	16.45	16.55	
F_2	0.808	0.948	
F_4	2.084	2.272	
F_5	0.32	0.52	
G_1	20 BASIC		
G_2	20 BASIC		
H_1	10 BASIC		
H_2	10 BASIC		
J_1	1 BASIC		
J_2	1 BASIC		
N	0.52	0.62	

3.2 Processor Pinout Assignment

Figure 3 and *Figure 4* are graphic representations of the processor pinout assignments. *Table 5* lists the pinout by signal name.

Figure 3. Pinout Diagram (Top View, Left Side)

	AA	Y	W	V	U	T	R	P	N	M
1		VSS	VSS	VSS	D[19]#	COMP0	VSS	D[34]#	D[35]#	VSS
2	VSS	VSS	D[25]#	D[30]#	D[27]#	COMP1	D[33]#	D[37]#	D[42]#	D[36]#
3	VSS	D[24]#	D[18]#	D[26]#	VSS	D[28]#	D[32]#	VSS	D[39]#	D[44]#
4	VSS	DSTBN[1]#	D[31]#	VSS	DPWR#	VSS	RSVD	VSS	VSS	RSVD
5	D[16]#	DSTBP[1]#	VSS	TEST2	TEST1	VSS	VSS	VSS	VSS	VSS
6	D[23]#	DINV[1]#	D[21]#	VSS	VSS	RSVD	VSS	VSS	TEST4	TEST3
7	VSS	D[22]#	D[20]#	VSS	VSS	VSS	VSS	VSS	VSS	VSS
8	D[29]#	D[17]#	VSS	VSS	VCCP	VCCP	VCCP	VCCP	VCCP	VCCP
9	D[14]#	D[8]#	D[15]#	RSVD	VCCP	VSS	VSS	VSS	VSS	VSS
10	VSS	D[7]#	D[1]#	VCCPC6	VCCP	VSS	VCC	VCC	VCC	VCC
11	D[4]#	D[0]#	VSS	BCLK0	VCCP	VSS	VCC	VCC	VCC	VCC
12	VSS	D[2]#	D[5]#	BCLK1	VCCP	VSS	VCC	VCC	VCC	VCC
13	D[11]#	D[9]#	D[13]#	VSS	VCCP	VSS	VSS	VSS	VSS	VSS
14	D[3]#	DSTBN[0]#	VSS	VSS	VCCP	VCCP	VCCP	VCCP	VCCP	VCCP
15	VSS	DSTBP[0]#	D[10]#	RSVD	VSS	LINT0	LINT1	VSS	RSVD	NC_6
16	D[6]#	D[12]#	DINV[0]#	INIT#	VSS	FERR#	STPCLK#	VSS	TDI	TDO
17	HIT#	RS[1]#	VSS	PWRGOOD	SMI#	RSVD	DPSLP#	RSVD	VSS	TCK
18	VSS	DBSY#	RS[0]#	VSS	A20M#	VSS	DPRSTP#	VSS	SLP#	RSVD
19	VSS	BNR#	TRDY#	ADS#	VSS	DRDY#	REQ[4]#	VSS	A[8]#	A[10]#
20	VSS	VSS	LOCK#	HITM#	RS[2]#	BR0#	A[6]#	REQ[3]#	A[5]#	A[13]#
21		VSS	VSS	VSS	BPRI#	DEFER#	VSS	A[3]#	REQ[0]#	VSS

Figure 4. Pinout Diagram (Top View, Right Side)

L	K	J	H	G	F	E	D	C	B	A	
DINV[2]#	VSS	D[47]#	D[46]#	VSS	D[50]#	D[53]#	VSS	RSVD	VSS		1
D[43]#	DSTBN[2]#	D[45]#	D[41]#	D[49]#	D[57]#	DSTBN[3]#	D[63]#	D[48]#	VSS	VSS	2
VSS	DSTBP[2]#	D[38]#	VSS	D[40]#	DSTBP[3]#	VSS	D[51]#	D[55]#	D[60]#	RSVD	3
VSS	NC_4	IGNNE#	VSS	VSS	VSS	THRMDA	RSVD	D[61]#	D[52]#	VSS	4
VSS	NC_5	VSS	BSEL1	BSEL2	VSS	THRMDC	VSS	DINV[3]#	VSS	D[54]#	5
VSS	VSS	BSEL0	NC_3	NC_2	VSS	VSS	NC_1	D[58]#	D[59]#	D[56]#	6
VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCCA	D[62]#	CMREF	GTLREF	7
VCCP	VCCP	VCCP	VCCP	VCCP	VCCP	VSS	VSS	VSS	VSS	VSS	8
VSS	VSS	VSS	VSS	VSS	VCCP	VCCP	VCCP	VCCP	VCCP	VCCP	9
VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	10
VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	11
VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	12
VSS	VSS	VSS	VSS	VSS	VCCPC6	VCCPC6	VSS_SENSE	VCC_SENSE	VSS	NC	13
VCCP	VCCP	VCCP	VCCP	VCCP	VCCPC6	VCCPC6	VSS	A[22]#	RSVD[1]	RSVD[3]	14
VSS	VSS	BPM[3]#	BPM[2]#	VID3	VID0	VSS	RESET#	A[28]#	RSVD[2]	VSS	15
NC_7	TRST#	PREQ#	VSS	VID4	IERR#	VSS	VID1	A[31]#	A[29]#	A[20]#	16
TMS	BPM[0]#	VSS	THERMTRIP#	PROCHOT#	VSS	VID5	RSVD	VSS	A[30]#	RSVD[0]	17
VSS	PRDY#	BPM[1]#	VSS	VID6	VSS	VID2	VSS	A[23]#	A[27]#	VSS	18
VSS	A[14]#	A[7]#	VSS	REQ[2]#	A[18]#	VSS	A[21]#	A[17]#	ADSTB[1]#	VSS	19
A[12]#	ADSTB[0]#	A[15]#	A[4]#	A[9]#	COMP2	A[25]#	A[26]#	A[24]#	VSS	VSS	20
A[16]#	VSS	REQ[1]#	A[11]#	VSS	COMP3	A[19]#	VSS	RSVD	VSS		21

Table 5. Pinout Arranged By Signal Name

Signal Name	Ball #
A[3]#	P21
A[4]#	H20
A[5]#	N20
A[6]#	R20
A[7]#	J19
A[8]#	N19
A[9]#	G20
A[10]#	M19
A[11]#	H21
A[12]#	L20
A[13]#	M20
A[14]#	K19
A[15]#	J20
A[16]#	L21
A[17]#	C19
A[18]#	F19
A[19]#	E21
A[20]#	A16
A[21]#	D19
A[22]#	C14
A[23]#	C18
A[24]#	C20
A[25]#	E20
A[26]#	D20
A[27]#	B18
A[28]#	C15
A[29]#	B16
A[30]#	B17
A[31]#	C16

Signal Name	Ball #
A20M#	U18
ADS#	V19
ADSTB[0]#	K20
ADSTB[1]#	B19
BCLK[0]	V11
BCLK[1]	V12
BNR#	Y19
BPM[0]#	K17
BPM[1]#	J18
BPM[2]#	H15
BPM[3]#	J15
BPRI#	U21
BR0#	T20
RSVD	V15
BSEL[0]	J6
BSEL[1]	H5
BSEL[2]	G5
CMREF[1]	B7
COMP[0]	T1
COMP[1]	T2
COMP[2]	F20
COMP[3]	F21
D[0]#	Y11
D[1]#	W10
D[2]#	Y12
D[3]#	AA14
D[4]#	AA11
D[5]#	W12
D[6]#	AA16

Signal Name	Ball #
D[7]#	Y10
D[8]#	Y9
D[9]#	Y13
D[10]#	W15
D[11]#	AA13
D[12]#	Y16
D[13]#	W13
D[14]#	AA9
D[15]#	W9
D[16]#	AA5
D[17]#	Y8
D[18]#	W3
D[19]#	U1
D[20]#	W7
D[21]#	W6
D[22]#	Y7
D[23]#	AA6
D[24]#	Y3
D[25]#	W2
D[26]#	V3
D[27]#	U2
D[28]#	T3
D[29]#	AA8
D[30]#	V2
D[31]#	W4
D[32]#	R3
D[33]#	R2
D[34]#	P1
D[35]#	N1

Signal Name	Ball #
D[36]#	M2
D[37]#	P2
D[38]#	J3
D[39]#	N3
D[40]#	G3
D[41]#	H2
D[42]#	N2
D[43]#	L2
D[44]#	M3
D[45]#	J2
D[46]#	H1
D[47]#	J1
D[48]#	C2
D[49]#	G2
D[50]#	F1
D[51]#	D3
D[52]#	B4
D[53]#	E1
D[54]#	A5
D[55]#	C3
D[56]#	A6
D[57]#	F2
D[58]#	C6
D[59]#	B6
D[60]#	B3
D[61]#	C4
D[62]#	C7
D[63]#	D2
DBSY#	Y18
DEFER#	T21
DINV[0]#	W16

Signal Name	Ball #
DINV[1]#	Y6
DINV[2]#	L1
DINV[3]#	C5
DPRSTP#	R18
DPSLP#	R17
DPWR#	U4
DRDY#	T19
DSTBN[0]#	Y14
DSTBN[1]#	Y4
DSTBN[2]#	K2
DSTBN[3]#	E2
DSTBP[0]#	Y15
DSTBP[1]#	Y5
DSTBP[2]#	K3
DSTBP[3]#	F3
FERR#	T16
RSVD	N15
GTLREF	A7
HIT#	AA17
HITM#	V20
IERR#	F16
IGNNE#	J4
INIT#	V16
LINT0	T15
LINT1	R15
LOCK#	W20
NC	A13
NC_1	D6
NC_2	G6
NC_3	H6
NC_4	K4

Signal Name	Ball #
NC_5	K5
NC_6	M15
NC_7	L16
PRDY#	K18
PREQ#	J16
PROCHOT#	G17
PWRGOOD	V17
REQ[0]#	N21
REQ[1]#	J21
REQ[2]#	G19
REQ[3]#	P20
REQ[4]#	R19
RESET#	D15
RS[0]#	W18
RS[1]#	Y17
RS[2]#	U20
RSVD	T6
RSVD[0]	A17
RSVD[1]	B14
RSVD[2]	B15
RSVD[3]	A14
RSVD	D17
RSVD	M18
RSVD	T17
RSVD	V9
RSVD	R4
RSVD	M4
RSVD	D4
RSVD	P17
RSVD	A3
RSVD	C1

Signal Name	Ball #
RSVD	C21
SLP#	N18
SMI#	U17
STPCLK#	R16
TCK	M17
TDI	N16
TDO	M16
TEST1	U5
TEST2	V5
TEST3	M6
TEST4	N6
THERMTRIP#	H17
THRMDA	E4
THRMDC	E5
TMS	L17
TRDY#	W19
TRST#	K16
VCC	A10
VCC	A11
VCC	A12
VCC	B10
VCC	B11
VCC	B12
VCC	C10
VCC	C11
VCC	C12
VCC	D10
VCC	D11
VCC	D12
VCC	E10
VCC	E11

Signal Name	Ball #
VCC	E12
VCC	F10
VCC	F11
VCC	F12
VCC	G10
VCC	G11
VCC	G12
VCC	H10
VCC	H11
VCC	H12
VCC	J10
VCC	J11
VCC	J12
VCC	K10
VCC	K11
VCC	K12
VCC	L10
VCC	L11
VCC	L12
VCC	M10
VCC	M11
VCC	M12
VCC	N10
VCC	N11
VCC	N12
VCC	P10
VCC	P11
VCC	P12
VCC	R10
VCC	R11
VCC	R12

Signal Name	Ball #
VCCA	D7
VCCP	C9
VCCP	D9
VCCP	E9
VCCP	F8
VCCP	F9
VCCP	G8
VCCP	G14
VCCP	H8
VCCP	H14
VCCP	J8
VCCP	J14
VCCP	K8
VCCP	K14
VCCP	L8
VCCP	L14
VCCP	M8
VCCP	M14
VCCP	N8
VCCP	N14
VCCP	P8
VCCP	P14
VCCP	R8
VCCP	R14
VCCP	T8
VCCP	T14
VCCP	U8
VCCP	U9
VCCP	U10
VCCP	U11
VCCP	U12

Signal Name	Ball #
VCCP	U13
VCCP	U14
VCCP	A9
VCCP	B9
VCCPC6	V10
VCCPC6	E13
VCCPC6	E14
VCCPC6	F13
VCCPC6	F14
VCC_SENSE	C13
VID[0]	F15
VID[1]	D16
VID[2]	E18
VID[3]	G15
VID[4]	G16
VID[5]	E17
VID[6]	G18
VSS	A2
VSS	A4
VSS	A8
VSS	A15
VSS	A18
VSS	A19
VSS	A20
VSS	B1
VSS	B2
VSS	B5
VSS	B8
VSS	B13
VSS	B20
VSS	B21

Signal Name	Ball #
VSS	C8
VSS	C17
VSS	D1
VSS	D5
VSS	D8
VSS	D14
VSS	D18
VSS	D21
VSS	E3
VSS	E6
VSS	E7
VSS	E8
VSS	E15
VSS	E16
VSS	E19
VSS	F4
VSS	F5
VSS	F6
VSS	F7
VSS	F17
VSS	F18
VSS	G1
VSS	G4
VSS	G7
VSS	G9
VSS	G13
VSS	G21
VSS	H3
VSS	H4
VSS	H7
VSS	H9

Signal Name	Ball #
VSS	H13
VSS	H16
VSS	H18
VSS	H19
VSS	J5
VSS	J7
VSS	J9
VSS	J13
VSS	J17
VSS	K1
VSS	K6
VSS	K7
VSS	K9
VSS	K13
VSS	K15
VSS	K21
VSS	L3
VSS	L4
VSS	L5
VSS	L6
VSS	L7
VSS	L9
VSS	L13
VSS	L15
VSS	L18
VSS	L19
VSS	M1
VSS	M5
VSS	M7
VSS	M9
VSS	M13

Signal Name	Ball #
VSS	M21
VSS	N4
VSS	N5
VSS	N7
VSS	N9
VSS	N13
VSS	N17
VSS	P3
VSS	P4
VSS	P5
VSS	P6
VSS	P7
VSS	P9
VSS	P13
VSS	P15
VSS	P16
VSS	P18
VSS	P19
VSS	R1
VSS	R5
VSS	R7
VSS	R9
VSS	R13
VSS	R21

Signal Name	Ball #
VSS	T4
VSS	T5
VSS	T7
VSS	T9
VSS	T10
VSS	T11
VSS	T12
VSS	T13
VSS	T18
VSS	U3
VSS	U6
VSS	U7
VSS	U15
VSS	U16
VSS	U19
VSS	V1
VSS	V4
VSS	V6
VSS	V7
VSS	V8
VSS	V13
VSS	V14
VSS	V18
VSS	V21

Signal Name	Ball #
VSS	W1
VSS	W5
VSS	W8
VSS	W11
VSS	W14
VSS	W17
VSS	W21
VSS	Y1
VSS	Y2
VSS	Y20
VSS	Y21
VSS	AA2
VSS	AA3
VSS	AA4
VSS	AA7
VSS	AA10
VSS	AA12
VSS	AA15
VSS	AA18
VSS	AA19
VSS	AA20
VSS	R6
VSS_SENSE	D13

3.3 Signal Description

This list is provided as a convenient reference. No pins have changed function.

Table 6. Signal Description

Signal Name	Type	Description
A[31:3]#	I/O	A[31:3]# (Address) defines a 2^{32}-byte physical memory address space. In subphase 1 of the address phase, these pins transmit the address of a transaction. In sub-phase 2, these pins transmit transaction type information. These signals must connect the appropriate pins of both agents on the processor FSB. A[31:3]# are source synchronous signals and are latched into the receiving buffers by ADSTB[1:0]#. Address signals are used as straps which are sampled before RESET# is de-asserted.
A20M#	I	If A20M# (Address-20 Mask) is asserted, the processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-MB boundary. Assertion of A20M# is only supported in real mode. A20M# is an asynchronous signal. However, to ensure recognition of this signal following an input/output write instruction, it must be valid along with the TRDY# assertion of the corresponding input/output Write bus transaction.
ADS#	I/O	ADS# (Address Strobe) is asserted to indicate the validity of the transaction address on the A[31:3]# and REQ[4:0]# pins. All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal loop, or deferred reply ID match operations associated with the new transaction.
ADSTB[1:0]#	I/O	Address strobes are used to latch A[31:3]# and REQ[4:0]# on their rising and falling edges. Strobes are associated with signals as shown below. **Signals** — **Associated Strobe** REQ[4:0]#, A[16:3]# — ADSTB[0]# A[31:17]# — ADSTB[1]#
BCLK[1:0]	I	The differential pair BCLK (Bus Clock) determines the FSB frequency. All FSB agents must receive these signals to drive their outputs and latch their inputs. All external timing parameters are specified with respect to the rising edge of BCLK0 crossing VCROSS.
BNR#	I/O	BNR# (Block Next Request) is used to assert a bus stall by any bus agent who is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions.

Signal Name	Type	Description
BPM[0]#	O	BPM[3:0]# (Breakpoint Monitor) are breakpoint and performance monitor signals. They are outputs from the processor which indicate the status of breakpoints and programmable counters used for monitoring processor performance. BPM[3:0]# should connect the appropriate pins of all FSB agents. This includes debug or performance monitoring tools.
BPM[1]#	I/O	
BPM[2]#	O	
BPM[3]#	I/O	
BPRI#	I	BPRI# (Bus Priority Request) is used to arbitrate for ownership of the FSB. It must connect the appropriate pins of both FSB agents. Observing BPRI# active (as asserted by the priority agent) causes the other agent to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed, then releases the bus by de-asserting BPRI#.
BR0#	I/O	BR0# is used by the processor to request the bus. The arbitration is done between the processor (Symmetric Agent) and SCH (High Priority Agent).
BSEL[2:0]	O	BSEL[2:0] (Bus Select) are used to select the processor input clock frequency. The *Intel® Atom™ Processor Z5xx Series Datasheet* defines the possible combinations of the signals and the frequency associated with each combination. The required frequency is determined by the processor, chipset and clock synthesizer. All agents must operate at the same frequency. The processor operates at 400-MHz or 533-MHz system bus frequency (100-MHz or 133-MHz BCLK frequency, respectively).
CMREF	PWR	CMREF determines the signal reference level for CMOS input pins. CMREF should be set at 1/2 V_{CCP}. CMREF is used by the CMOS receivers to determine if a signal is a logical 0 or logical 1. If not using CMOS, then all CMREF and GTLREF should be provided with 2/3 V_{CCP}.
COMP[3:0]	PWR	COMP[3:0] must be terminated on the system board using precision (1% tolerance) resistors.

Signal Name	Type	Description
D[63:0]#	I/O	D[63:0]# (Data) are the data signals. These signals provide a 64-bit data path between the FSB agents, and must connect the appropriate pins on both agents. The data driver asserts DRDY# to indicate a valid data transfer. D[63:0]# are quad-pumped signals and will thus be driven four times in a common clock period. D[63:0]# are latched off the falling edge of both DSTBP[3:0]# and DSTBN[3:0]#. Each group of 16 data signals correspond to a pair of one DSTBP# and one DSTBN#. The following table shows the grouping of data signals to data strobes and DINV#. **Quad-Pumped Signal Groups** **Data Group — DSTBN#/DSTBP# — DINV#** D[15:0]# — 0 — 0 D[31:16]# — 1 — 1 D[47:32]# — 2 — 2 D[63:48]# — 3 — 3 Furthermore, the DINV# pins determine the polarity of the data signals. Each group of 16 data signals corresponds to one DINV# signal. When the DINV# signal is active, the corresponding data group is inverted and therefore sampled active high.
DBSY#	I/O	DBSY# (Data Bus Busy) is asserted by the agent responsible for driving data on the FSB to indicate that the data bus is in use. The data bus is released after DBSY# is de-asserted. This signal must connect the appropriate pins on both FSB agents.
DEFER#	I	DEFER# is asserted by an agent to indicate that a transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory or Input/Output agent. This signal must connect the appropriate pins of both FSB agents.
DINV[3:0]#	I	DINV[3:0]# (Data Bus Inversion) are source synchronous and indicate the polarity of the D[63:0]# signals. The DINV[3:0]# signals are activated when the data on the data bus is inverted. The bus agent will invert the data bus signals if more than half the bits, within the covered group, would change level in the next cycle. DINV[3:0]# assignment to data bus signals is shown below. **Bus Signal — Data Bus Signals** DINV[3]# — D[63:48]# DINV[2]# — D[47:32]# DINV[1]# — D[31:16]# DINV[0]# — D[15:0]#
DPRSTP#	I	DPRSTP# when asserted on the platform causes the processor to transition from the Deep Sleep State to the Deeper Sleep state. In order to return to the Deep Sleep State, DPRSTP# must be de-asserted. DPRSTP# is driven by the SCH.
DPSLP#	I	DPSLP# when asserted on the platform causes the processor to transition from the Sleep State to the Deep Sleep state. In order to return to the Sleep State, DPSLP# must be de-asserted. DPSLP# is driven by the SCH.

Signal Name	Type	Description
DPWR#	I	DPWR# is a control signal from the SCH used to reduce power on the processor data bus input buffers.
DRDY#	I/O	DRDY# (Data Ready) is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multi-common clock data transfer, DRDY# may be de-asserted to insert idle clocks. This signal must connect the appropriate pins of both FSB agents.
DSTBN[3:0]#	I/O	Data strobe used to latch in D[63:0]#. **Signals** **Associated Strobe** D[15:0]# DINV[0]#, DSTBN[0]# D[31:16]# DINV[1]#, DSTBN[1]# D[47:32]# DINV[2]#, DSTBN[2]# D[63:48]# DINV[3]#, DSTBN[3]#
DSTBP[3:0]#	I/O	Data strobe used to latch in D[63:0]#. **Signals** **Associated Strobe** D[15:0]# DINV[0]#, DSTBP[0]# D[31:16]# DINV[1]#, DSTBP[1]# D[47:32]# DINV[2]#, DSTBP[2]# D[63:48]# DINV[3]#, DSTBP[3]#
FERR#/PBE#	O	FERR# (Floating-point Error)/PBE# (Pending Break Event) is a multiplexed signal and its meaning is qualified with STPCLK#. When STPCLK# is not asserted, FERR#/PBE# indicates a floating point when the processor detects an unmasked floating-point error. FERR# is similar to the ERROR# signal on the Intel 387 coprocessor, and is included for compatibility with systems using MSDOS*- type floating-point error reporting. When STPCLK# is asserted, an assertion of FERR#/PBE# indicates that the processor has a pending break event waiting for service. The assertion of FERR#/PBE# indicates that the processor should be returned to the Normal state. When FERR#/PBE# is asserted, indicating a break event, it will remain asserted until STPCLK# is de-asserted. Assertion of PREQ# when STPCLK# is active will also cause an FERR# break event. For additional information on the pending break event functionality, including identification of support of the feature and enable/disable information, refer to Volume 3 of the *Intel® 64 and IA-32 Architectures Software Developer's Manuals* and the *Intel® Processor Identification and CPUID Instruction Application Note*.
GTLREF	PWR	GTLREF determines the signal reference level for AGTL+ input pins. GTLREF should be set at 2/3 V_{CCP}. GTLREF is used by the AGTL+ receivers to determine if a signal is a logical 0 or logical 1.
HIT# HITM#	I/O	HIT# (Snoop Hit) and HITM# (Hit Modified) convey transaction snoop operation results. Either FSB agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.

Signal Name	Type	Description
IERR#	O	IERR# (Internal Error) is asserted by a processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the FSB. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic. The processor will keep IERR# asserted until the assertion of RESET#, BINIT#, or INIT#.
IGNNE#	I	IGNNE# (Ignore Numeric Error) is asserted to force the processor to ignore a numeric error and continue to execute non-control floating-point instructions. If IGNNE# is de-asserted, the processor generates an exception on a non-control floating-point instruction if a previous floating-point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 (CR0) is set. IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.
INIT#	I	INIT# (Initialization), when asserted, resets integer registers inside the processor without affecting its internal caches or floating-point registers. The processor then begins execution at the power-on Reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output Write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction. INIT# must connect the appropriate pins of both FSB agents. If INIT# is sampled active on the active to inactive transition of RESET#, the processor reverses its FSB data and address signals internally to ease motherboard layout for systems where the chipset is on the other side of the motherboard. D[63:0] => D[0:63] A[31:3] => A[3:31] DINV[3:0]# is also reversed.
LINT[1:0]	I	LINT[1:0] (Local APIC Interrupt) must connect the appropriate pins of all APIC Bus agents. When the APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a non-maskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Pentium processor. Both signals are asynchronous. Both of these signals must be software configured via BIOS programming of the APIC register space to be used either as NMI/INTR or LINT[1:0]. Because the APIC is enabled by default after Reset, operation of these pins as LINT[1:0] is the default configuration.

Signal Name	Type	Description
LOCK#	I/O	LOCK# indicates to the system that a transaction must occur atomically. This signal must connect the appropriate pins/lands of all FSB agents. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction to the end of the last transaction.
PRDY#	O	Probe Ready signal used by debug tools to determine processor debug readiness.
PREQ#	I	Probe Request signal used by debug tools to request debug operation of the processor.
PROCHOT#	I/O, O (DP)	As an output, PROCHOT# (Processor Hot) will go active when the processor temperature monitoring sensor detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit (TCC) has been activated, if enabled. As an input, assertion of PROCHOT# by the system will activate the TCC, if enabled. The TCC will remain active until the system de-asserts PROCHOT#. This signal may require voltage translation on the motherboard.
PWRGOOD	I	PWRGOOD (Power Good) is a processor input. The processor requires this signal to be a clean indication that the clocks and power supplies are stable and within their specifications. 'Clean' implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGOOD. The PWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation.
REQ[4:0]#	I/O	REQ[4:0]# (Request Command) must connect the appropriate pins of both FSB agents. They are asserted by the current bus owner to define the currently active transaction type. These signals are source synchronous to ADSTB[0]#.
RESET#	I	Asserting the RESET# signal resets the processor to a known state and invalidates its internal caches without writing back any of their contents. For a power-on Reset, RESET# must stay active for at least two milliseconds after V_{CC} and BCLK have reached their proper specifications. On observing active RESET#, both FSB agents will de-assert their outputs within two clocks. All processor straps must be valid within the specified setup time before RESET# is de-asserted.
RS[2:0]#	I	RS[2:0]# (Response Status) are driven by the response agent (the agent responsible for completion of the current transaction), and must connect the appropriate pins of both FSB agents.
RSVD	Reserved	RSVD[3:0] (pins A14, B15, B14, A17) **must** be tied directly to VCCP to ensure proper operation of the processor. All other RSVD signals can be left as No Connects.

Signal Name	Type	Description
SLP#	I	SLP# (Sleep), when asserted in Stop-Grant state, causes the processor to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. Processors in this state will not recognize snoops or interrupts. The processor will recognize only assertion of the RESET# signal, de-assertion of SLP#, and removal of the BCLK input while in Sleep state. If SLP# is de-asserted, the processor exits Sleep state and returns to Stop-Grant state, restarting its internal clock signals to the bus and processor core units. If DPSLP# is asserted while in the Sleep state, the processor will exit the Sleep state and transition to the Deep Sleep state.
SMI#	I	SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, the processor saves the current state and enters System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler. If SMI# is asserted during the de-assertion of RESET# the processor will tri-state its outputs.
STPCLK#	I	STPCLK# (Stop Clock), when asserted, causes the processor to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units except the FSB and APIC units. The processor continues to snoop bus transactions and service interrupts while in Stop-Grant state. When STPCLK# is de-asserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input.
TCK	I	TCK (Test Clock) provides the clock input for the processor Test Bus (also known as the Test Access Port).
TDI	I	TDI (Test Data In) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.
TDO	O	TDO (Test Data Out) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.
TEST[1:4]		Test signals. All TEST signals can be left as No Connects.
THERMTRIP#	O	The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all execution when the junction temperature exceeds approximately 125°C. This condition is signaled to the system by the THERMTRIP# (Thermal Trip) pin.
THRMDA	PWR	Thermal Diode - Anode
THRMDC	PWR	Thermal Diode - Cathode
TMS	I	TMS (Test Mode Select) is a JTAG specification support signal used by debug tools.

Signal Name	Type	Description
TRDY#	I	TRDY# (Target Ready) is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of both FSB agents.
TRST#	I	TRST# (Test Reset) resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset.
VCCA	PWR	VCCA provides isolated power for the internal processor core PLLs.
VCC	PWR	Processor core power supply
VSS	GND	Processor core ground node.
VSS / NCTF	GND	Non Critical to Function
VID[6:0]	O	VID[6:0] (Voltage ID) pins are used to support automatic selection of power supply voltages (V_{CC}). Unlike some previous generations of processors, these are CMOS signals that are driven by the processor. The voltage supply for these pins must be valid before the VR can supply V_{CC} to the processor. Conversely, the VR output must be disabled until the voltage supply for the VID pins becomes valid. The VID pins are needed to support the processor voltage specification variations. See the *Intel® Atom™ Processor Z5xx Series Datasheet* for definitions of these pins. The VR must supply the voltage that is requested by the pins, or disable itself.
VCCP	PWR	Processor I/O Power Supply which needs to turn off in Deep Power Down Technology (C6) state if Splitt V_{TT} is incorporated.
VCCPC6	PWR	Processor I/O Power Supply which needs to remain on in Deep Power Down Technology (C6) state.
VCC_SENSE	O	VCC_SENSE is an isolated low impedance connection to processor core power (V_{CC}). It can be used to sense or measure power near the silicon with little noise.
VSS_SENSE	O	VSS_SENSE is an isolated low impedance connection to processor core V_{SS}. It can be used to sense or measure ground near the silicon with little noise.

§

4 Thermal Specifications and Design Considerations

This chapter provides clarifications to the *Thermal Specifications and Design Considerations* chapter of the *Intel® Atom™ Processor Z5xx Series Datasheet*. It should be used in conjunction with the *Intel Atom Processor Z5xxPx Thermal Design Guidelines* instead of any Intel Atom Z5xx, N2xx, or N3xx based supplemental thermal documents.

4.1 Power Specifications

Table 7 replaces all Power Specifications tables in the *Intel® Atom™ Processor Z5xx Series Datasheet*.

Table 7. Power Specifications for the Intel® Atom™ processor Z5xxPx series

Symbol	Processor Number	Core Frequency and Voltage	Thermal Design Power			Unit	Notes
TDP_{CT}	Z510P	1.1 GHz at HFM V_{CC} for Commercial Temp.	2.0 W 2.2 W with HT enabled			W	At 90°C 1, 4
	Z530P	1.6 GHz at HFM V_{CC} for Commercial Temp.					
TDP_{IT}	Z510PT	1.1 GHz at HFM V_{CC} for Industrial Temp.	2.0 W 2.2 W with HT enabled			W	At 110°C 1, 4
	Z520PT	1.33 GHz at HFM V_{CC} for Industrial Temp.					
Symbol	**Parameter**		**Min**	**Typ**	**Max**	**Unit**	**Notes**
P_{AH}, P_{SGNT}	Auto Halt, Stop Grant Power for Z530P and Z510P at HFM V_{CC} at LFM V_{CC}		—	—	 1.0 0.7	 W W	At 70°C 2
	Auto Halt, Stop Grant Power for Z520PT and Z510PT at HFM V_{CC} at LFM V_{CC}		—	—	 1.0 TBD	 W W	At 110°C 2
P_{DSLP}	Deep Sleep Power		—	—	0.5	W	At 50°C 2, 5

P_{DPRSLP}	Deeper Sleep Power	—	—	0.5	W	At 50°C 2, 5
P_{DC6}	Deep Power Down Technology (C6)	—	—	0.1	W	At 50°C 2
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Notes**
T_{J-CT}	Junction Temperature (Commercial Temp.)	0	—	90	°C	3, 4
T_{J-IT}	Junction Temperature (Industrial Temp.)	-40	—	110	°C	3, 4

NOTES:

1. The TDP specification should be used to design the processor thermal solution. The TDP is not the maximum theoretical power the processor can generate.
2. Not 100% tested. These power specifications are determined by characterization of the processor currents at higher temperatures and extrapolating the values for the temperature indicated.
3. As measured by the activation of the on-die Intel® Thermal Monitor. The Intel Thermal Monitor's automatic mode is used to indicate that the maximum TJ has been reached. Refer to the Thermal Specifications section of the *Intel® Atom™ Processor Z5xx Series Datasheet* for more details.
4. The Intel Thermal Monitor automatic mode must be enabled for the processor to operate within specifications.
5. Deep Sleep state is mapped to Deeper Sleep State.

4.2 Thermal Specifications

The thermal diode pins numbers have changed. When referencing the Thermal Diode Interface table in the *Intel® Atom™ Processor Z5xx Series Datasheet*, replace it with *Table 8* shown below.

Table 8. Thermal Diode Interface

Signal Name	Pin/Ball Number	Signal Description
THERMDA	E4	Thermal diode anode
THERMDC	E5	Thermal diode cathode

4.3 Storage Condition Specifications

Environmental storage condition limits define the temperature and relative humidity limits to which the device is exposed while being stored in a Moisture Barrier Bag. The specified storage conditions are for component level prior to board attach (see notes below guideline on post board attach limits).

Table 9 specifies absolute maximum and minimum storage temperature limits which represent the maximum or minimum device condition beyond which damage, latent or otherwise, may occur. The table also specifies sustained storage temperature, relative humidity, and time-duration limits. These limits specify the maximum or minimum

device storage conditions for a sustained period of time. At conditions outside sustained limits, but within absolute maximum and minimum ratings, quality & reliability may be affected.

Table 9. Storage Condition Ratings

Symbol	Parameter	Min	Max
$T_{abs\ storage}$	The minimum/maximum device storage temperature beyond which damage (latent or otherwise) may occur when subjected to for any length of time.	-55°C	125°C
$T_{sustained\ storage}$	The minimum/maximum device storage temperature for a sustained period of time.	-5°C	40°C
$RH_{sustained\ storage}$	The maximum device storage relative humidity for a sustained period of time.	—	60% @ 24°C
$Time_{sustained\ storage}$	A prolonged or extended period of time; typically associated with sustained storage conditions.	0 months	6 months

NOTES:

1. Storage conditions are applicable to storage environments only. In this scenario, the processor must not receive a clock, and no lands can be connected to a voltage bias. Storage within these limits will not affect the long-term reliability of the device. For functional operation, please refer to the processor case temperature specifications.
2. These ratings apply to the Intel component and do not include the tray or packaging.
3. Failure to adhere to this specification can affect the long-term reliability of the processor.
4. Non-operating storage limits post board attach: Storage condition limits for the component once attached to the application board are not specified. Intel does not conduct component level certification assessments post board attach given the multitude of attach methods, socket types and board types used by customers. Provided as general guidance only, Intel board products are specified and certified to meet the following temperature and humidity limits (Non-Operating Temperature Limit: -40C to 70C & Humidity: 50% to 90%, non condensing with a maximum wet bulb of 28C).
5. Device storage temperature qualification methods follow JESD22-A119 (low temp) and JESD22-A103 (high temp) standards.