APM883408-X2 | X-Gene® 2 Multi-Core 64-bit Processor

The AppliedMicro® APM883408-X2 X-Gene® 2 architecture encompasses a family of server class processors, including the Server on a Chip® processor, the Cloud Processor®, and the Cloud Server® processor that are optimized for next-generation data centers, cloud computing, enterprise servers, and embedded communication by offering unprecedented improvement in performance per watt per dollar against existing solutions in the market. The high level of integration with high-speed peripherals for Storage, PCI Express connectivity, and 10GE Networking, combined with server class 64-bit ARM® v8-compliant CPUs and configurable offload capability results in a solution that dramatically reduces the total cost of ownership for a data center.

Features

- Eight X-Gene 2 processor cores operating at up to 2.4 GHz
  - ARM v8-compliant 64-bit processor cores
  - Floating Point (FP) / A-SIMD (Advanced Single Instruction, Multiple Data) Unit per core
  - 32 KB L1 data cache, 32 KB L1 instruction cache per core
- Shared 256 KB L2 cache per each pair of cores
- ECC protection on caches
- Shared 8 MB L3 cache
- Hardware Cache Coherency
- ARM Generic Interrupt Controller (GICv2m)
- Four DDR3 memory controllers with ECC (72-bit)
- 512 KB On-Chip SRAM (OCM)
- High-Performance I/O Fabric (IOF)
- I/O virtualization - Supports 32 VFs for key high performance interfaces (PCIe and Ethernet) and Packet-aware DMA engine.

Offload Features

- True Random Number Generator (TRNG)
- Packet DMA Engine with RAID 5 offload

Queue Manager / Traffic Manager

- Message passing architecture
- Manages Work, Free, and Virtual Queues

High-Speed Interfaces

- Two 10-Gbps Ethernet MACs (XFI/SGMII) with in-line classification capability along with RSS and virtualization
  - SFP+ active module support
- PCI Express® Gen 3 controller with internal DMA:
  - 1x 8-lane or 2x 4-lane
- One USB 2.0 Host with integrated PHY
- Six SATA 3.0 ports

Other Interfaces

- I^2C
- UART
- GPIO
- SPI
- Embedded Local Bus (EBUS)
- SDIO 3.0

Power Management

- Multiple power planes and clock gating

The X-Gene 2 Multi-Core Processor for Performance Applications

At the heart of the APM883408-X2 are eight X-Gene 2 processor cores based on the ARM v8 architecture with full SMP support and individual Floating Point processors. The X-Gene 2 architecture offers high-end processing performance. For example the innovative Server on a Chip subsystem features the Power Management processor (PMpro) and Scalable Lightweight Intelligent Management processor (SLIMpro) to enable breakthrough flexibility in power management, resiliency, and end-to-end security for a wide range of applications from data centers, cloud computing, enterprise servers, embedded communication, and other mission-critical systems. The X-Gene 2 processors are programmable and fully compliant with an industry-standard instruction set architecture (ISA). In addition, these processors are assisted by a rich set of configurable accelerators focused on packet classification, security, packet/data manipulation, and scheduling. The X-Gene 2 architecture provides unique congestion aware management capability to optimize its available processing resources. This allows for full use control on bandwidth and services. Designed in 28nm bulk CMOS technology, the APM883408-X2 offers the best-in-class cost versus processing performance in a low-power envelope.

X-Gene 2 Processor Complex Features

The APM883408-X2 incorporates eight high performance X-Gene 2 processors. Each X-Gene 2 processor has a 32 KB data cache and a 32 KB instruction cache (which are 8-way set associative), and a FPU with SIMD execution. Each pair of X-Gene 2 cores has a shared 256 KB L2 cache with hardware cache coherency (SMP) that attaches to the high-performance coherent Central Switch (CSW). A shared 8 MB L3 cache is also attached to the CSW.

Embedded High Performance Network Controller

The Embedded high performance network controllers provide for flow, CoS, and port based classification of data with 64-byte packet line rate performance. They are programmable and can support IPv4 and IPv6, as well as proprietary protocols.

Queue Manager / Traffic Manager (QMTM)

The QMTM allows for the efficient movement of packets or data between the processors and peripherals using a message passing architecture. This is accomplished through a central communication interface that offloads software from the routing of packets and from transaction synchronization.
The Queue Manager can be used to centralize management of all transaction traffic, reduce communication overhead between software and hardware, and perform inter-processor message passing and work scheduling.

PMpro and SLIMpro – Power and System Management

The APM883408-X2 integrates two dedicated 32-bit processors, PMpro, and SLIMpro. The PMpro processor provides advanced power management capabilities such as multiple power planes and clock gating, thermal protection circuits, Advanced Configuration Power Interface (ACPI) power management states and external power throttling support. The SLIMpro processor provides system management capabilities including secure boot.

Cryptographic Acceleration

The X-Gene 2 processor core supports the ARM v8 optional cryptographic extension instructions, delivering a combination of high-performance cryptographic transform and authentication with the flexibility of software to respond to evolving security standards.

Advanced DMA

The Packet DMA can be used to perform memory-to-memory transfers, which include the SDRAM, SRAM, and PCIe memory spaces.

Specifications

Cores / Caches
- Eight X-Gene 2 processor cores Each processor contains a FPU Each with 32 KB L1 data cache, 32 KB L1 instruction cache
- Shared 256 KB L2 cache per each pair of processors
- Shared 8 MB L3 cache

X-Gene 2 Core Frequency
- Up to 2.4 GHz

Operating Junction Temperature Range
- 0 ºC to + 90 ºC

Power Supply
- CPU/SoC logic: 0.9 V
- DDR3: 1.35 V/1.5 V
- 3.3 V

Packaging
- 1624-pin Heat Spreader Flip Chip Ball Grid Array (HFCBGA)

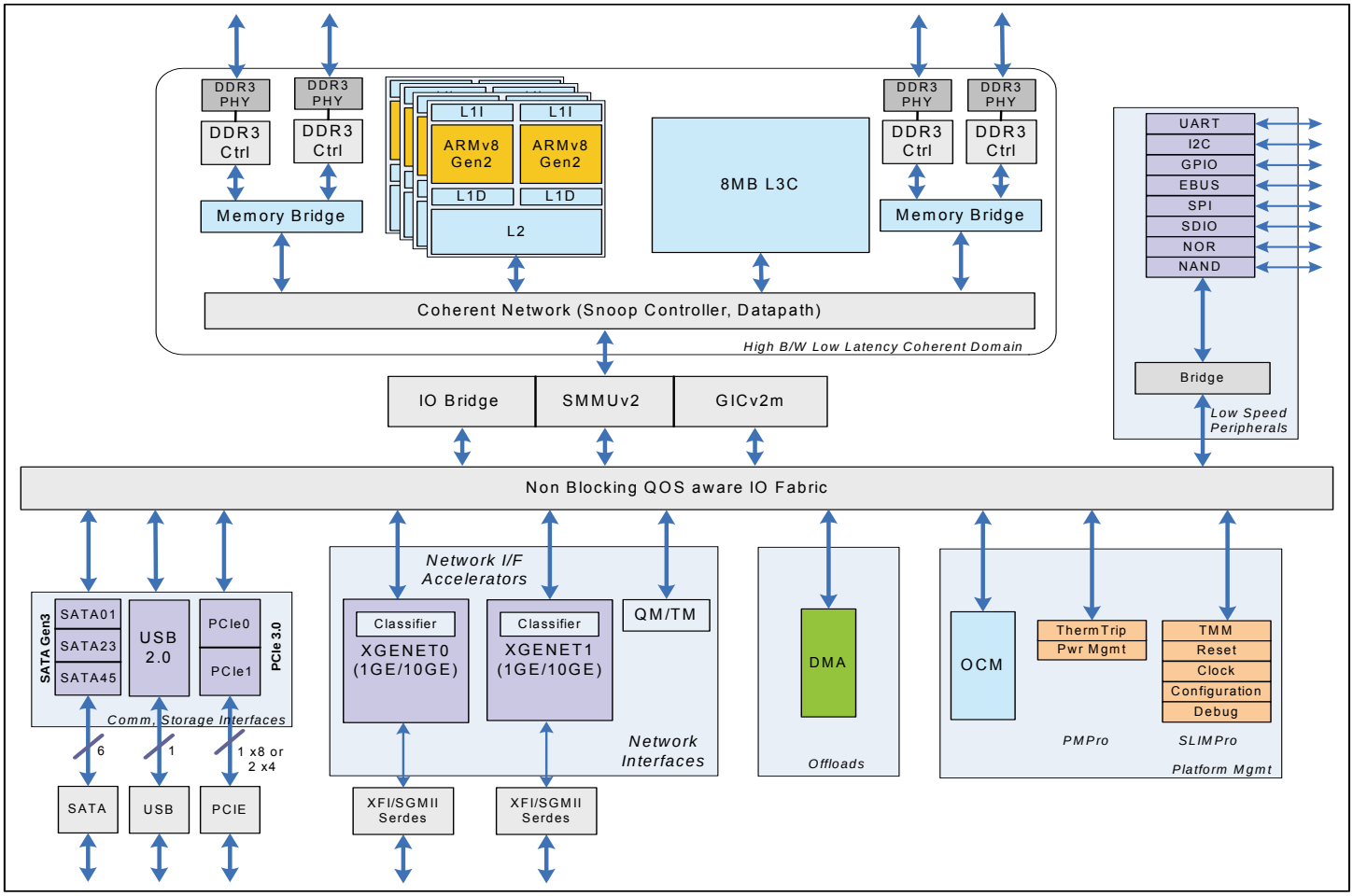
Transfers can also include certain 'on-the-fly' data manipulations such as the checksum generation or checking, CRC generation or checking, and XOR calculation for RAID-5 acceleration.
The Packet DMA comprehends data packet delineation, which enables it to perform a comprehensive list of scatter or gather operations for packet assembly and disassembly with minimal software intervention.

AppliedMicro's X-Gene 2 Partner Ecosystem

AppliedMicro's X-Gene 2 processors are supported by an extensive Partner ecosystem of products and services from a wide range of leading suppliers, including industry standard providers of:
- Server and Embedded operating systems
- Hardware and Software development tools
- Server and Embedded software products and services
- Board-level products
- System design services
- Technical training

AppliedMicro offers an evaluation kit for product evaluation and for early software development.

X-Gene 2 Block Diagram



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