μCOM-42 4-BIT SINGLE CHIP MICROCOMPUTER

DESCRIPTION

The μCOM-42 (Part No. μPD548) is a single chip microcomputer that is ideally suited for Electronic Cash Register (ECR), Point of Sale (POS) and Electronic Scale applications.

Containing a 4-bit Parallel ALU, ROM for program storage and RAM for data storage, the μCOM-42 provides an economical and simple solution to many Vending/Calculating requirements.

Because of its extensive instruction set and five input/output ports, the μCOM-42 is capable of controlling an 8 x 4 keyboard, an 8 digit display and low cost ECR-type printers.

Finally, the on-chip RAM space can be augmented by an external CMOS RAM for applications requiring low power data retention.

FEATURES

- Stand Alone 4-bit Microcomputer
- All 72 Instructions are Single Byte
- 10 μsec Instruction Cycle
- 1920 x 10-Bit Program Memory (ROM)
- 96 x 4-Bit Data Memory (RAM)
- 4-Level Stack
- 2 Interrupt Request Lines
- I/O Compatible with TTL
- 10 Discrete Output Ports (F_0-F_9)
- Two 8-Bit Output Ports (U_0-U_7, R_0-R_7)
- One 4-Bit Input Port (K_0-K_3)
- One 4-Bit Input/Output Port (S_0-S_3)
- One Single Bit Testable Input Port (K_4)
- Single Phase TTL Level Clock (200 KHz Max.)
- Single Supply, −10V PMOS Technology
- 42 Pin Plastic Dual-in-Line Package

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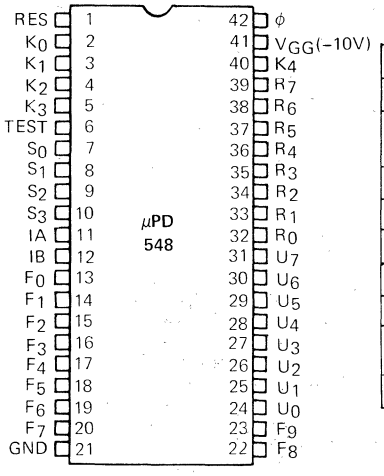
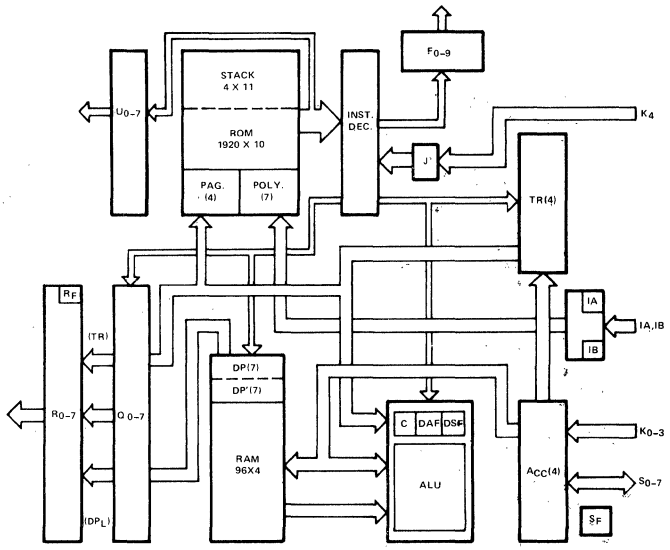
PIN CONFIGURATION



PIN NAMES

RES	Reset
K_0–K_3	Input Port K
TEST	Input for Testing (Normally V_{GG})
S_0–S_3	Input/Output Port S
IA, IB	Interrupt Input Ports
F_0–F_9	Output Port F
U_0–U_7	Output Port U
R_0–R_7	Output Port R
K_4	Input Port for Condition Test
φ	Clock Input

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Program Counter

The 11-bit program counter is composed of two sections, a 4-bit page register and a 7-bit polynomial counter. The page register selects one page out of 15, each consisting of 128 words addressed by the 7-bit polynomial counter. The contents of the page register are independent of the operation of the polynomial counter, so that it is not affected by polynomial counter overflow.

Stack Register

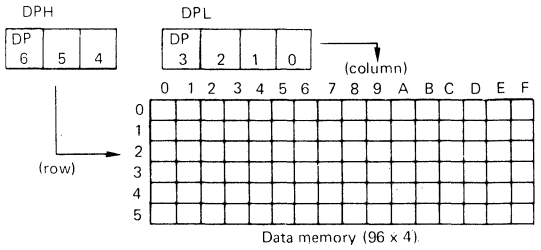
In order to store the program counter contents upon an interrupt or subroutine call, four 11-bit stack registers are provided to enable a combination of subroutine calls and interrupt nesting to four levels. The stack register is a LIFO (Last in, First-Out) type.

ROM (Read Only Memory)

The on-chip ROM consists of 1,920 words of ten bits each and is divided into 15 pages. A page is selected by the page register, the upper four bits of the program counter. Each page consists of 128 words addressed by the polynomial counter, the lower seven bits of the program counter.

RAM (Data Memory)

The data memory is a 96 x 4-bit RAM addressed by a 7-bit data pointer (DP). The RAM is divided into six rows of 16 4-bit columns each. The 7-bit data pointer consists of an upper 3-bit register (DPH) which selects the row address and a lower 4-bit register (DPL) which selects the column address.



Data memory (96 x 4)

FUNCTIONAL DESCRIPTION (CONT.)

Internal Registers

The Accumulator (ACC) is connected with the ALU and the carry flip-flop (C) and is able to perform either binary or decimal arithmetic by testing the decimal addition flip-flop (DAF) and the decimal subtraction flip-flop (DSF). Constants are loaded into the ACC as immediate data from ROM and variable data are loaded from or exchanged with RAM. The ACC is also connected with the temporary register (TR), the parallel I/O port S and the parallel input port K. The TR is an auxiliary register used for temporary storage of 4-bit data. The Q register is an 8-bit serial-in/parallel-out shift register designed for display digit strobing and generation of printer hammer triggers.

I/O Ports

The R port is an 8-bit parallel port that may be loaded from the Q register for digit strobing or loaded with the 4-bit TR and the 4-bit DPL for external RAM addressing. The U port is an 8-bit parallel port that is loaded with immediate data. It is usually used for outputting segment information for display and digit information for key scanning. The K port is a 4-bit input port that is usually used for key scan input. The K4 port is a single bit port that is testable by software. The S port is a 4-bit parallel I/O port that is typically used as the data bus to external RAM. The F port consists of ten discrete output lines that can be individually set or reset under program control.

Interrupt Ports

Two interrupt input lines, IA and IB, are available to accept an interrupt request when interrupts are enabled. IA has a higher priority level than IB. Thus when concurrent interrupts occur on both IA and IB only the IA interrupt is accepted and both are disabled. But a single IB interrupt disables only the IB interrupt and leaves IA enabled.

INSTRUCTION SET

The μCOM-42 has a powerful 72, 10-bit word, instruction set. All instructions are single words. There are a number of multi-function instructions which reduce the number of program steps. In addition, automatic data pointer modification, single word sub-routine calls and N-way branch capability all help improve operation speed and reduce ROM requirements. The μCOM-42 instruction set is summarized below.

MNEMONIC	CYCLES	DESCRIPTION	CONDITIONS FOR SKIP
CMA	1	$A_{CC} \cdot (\overline{A_{CC}})$	
CIA	1	$A_{CC} \cdot (\overline{A_{CC}}) + 1$	
INA	1/2	$A_{CC} \cdot (A_{CC}) + 1$	Carry = 1
DEA	1/2	$A_{CC} \cdot (A_{CC}) - 1$	Borrow ≠ 1
RFC	1	$C \cdot 0$	
SFC	1	$C \cdot 1$	
DSM	1	Decimal Subtract Mode	
DAM	1	Decimal Add Mode	
AD	1/2	$A_{CC} \cdot (A_{CC}) + [DP]$	Carry = 1
ADC	1	$A_{CC}, C \cdot (A_{CC}) + [DP] + (C)$	
ADI	1/2	$A_{CC} \cdot (A_{CC}) + I_3 I_2 I_1 I_0$	Carry = 1
LM	1	$A_{CC} \cdot [DP]$ $DP_H \cdot (DP_H) \vee M_2 M_1 M_0$	
XM	1	$(A_{CC}) \cdot\cdot [DP]$ $DP_H \cdot (DP_H) \vee M_2 M_1 M_0$	
XMI	1/2	$(A_{CC}) \cdot\cdot [DP]$ $DP_H \cdot (DP_H) \vee M_2 M_1 M_0$ $DP_L \cdot (DP_L) + 1$	$(DP_L) = 8$ or $(DP_L) = 0$
XMD	1/2	$(A_{CC}) \leftrightarrow [DP], DP_H \cdot (DP_H)$ $M_2M_1M_0, DP_L \cdot (DP_L) - 1$	$(DP_L) = F$ or $(DP_L) = 7$
LI	1	$A_{CC} \cdot I_3 I_2 I_1 I_0$	
LDI	1	$DP \cdot I_6 - I_0$	
IND	1/2	$DP_L \cdot (DP_L) + 1$	$(DP_L) = 8$ or $(DP_L) = 0$
DED	1/2	$DP_L \cdot (DP_L) - 1$	$(DP_L) = F$ or $(DP_L) = 7$
XDP	1	$(DP) \cdot\cdot (DP')$	
ZAG	1	$000DP_L \cdot (DP)$	

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MNEMONIC	CYCLES	DESCRIPTION	CONDITIONS FOR SKIP
XTA	1	$(A_{CC}) \leftrightarrow (TR)$	
LTI	1	$TR \leftarrow I_3\ I_2\ I_1\ I_0$	
QS1	1	$Q_{n+1} \leftarrow Q_n,\ Q_0 \leftarrow 1$	
QS0	1	$Q_{n+1} \leftarrow Q_n,\ Q_0 \leftarrow 0$	
SB	1	$[DP, B_1, B_0] \leftarrow 1$	
RB	1	$[DP, B_1, B_0] \leftarrow 0$	
SBT	1/2	Skip if $[DP, B_1, B_0] = 1$	$B_1\ B_0 = 1$
SC	1/2	Skip if (C) = 1	(C) = 1
SEM	1/2	Skip if $(A_{CC}) = [DP]$	$(A_{CC}) = [DP]$
SEI	1/2	Skip if $(A_{CC}) = I_3\ I_2\ I_1\ I_0$	$(A_{CC}) = I_3\ I_2\ I_1\ I_0$
SK4	1/2	Skip if $K_4 = 1$	$K_4 = 1$
JPT	1	$PC \leftarrow (TR), P_{6-0}$	
JPA	1	$PC_{6-4} \leftarrow P_{6-4}$ $PC_{3-0} \leftarrow P_{3-0} \vee (A_{CC})$	
JCP	1	$PC_{6-0} \leftarrow P_{6-0}$	
CAL	1	[STACK] ← (PC) $PC \leftarrow 1000\ P_6\ P_5\ P_4\ P_3\ P_2\ P_1\ P_0$	
RT	1	PC ← [STACK]	
RTS	2	PC ← [STACK] PC ← (PC) + 1	
EIA	1	Enable IA port	
DIA	1	Disable IA port	
EIB	1	Enable IB port	
DIB	1	Disable IB port	
OIU	1	$U_{7-0} \leftarrow I_{7-0}$ $R_{7-0} \leftarrow (Q_{7-0})$	
ERO	1	Enable R port	
DRO	1	Disable R port	
OGR	1	R ← (Q)	
OTR	1	$R_{7-4} \leftarrow (TR), R_{3-0} \leftarrow (DP_L)$	
SFS	1	$S \leftarrow (A_{CC})$	
RFS	1	S port Input Mode	
IS	1	$A_{CC} \leftarrow S$	
IK	1	$A_{CC} \leftarrow K$	
RF1	1	$F_1 \leftarrow 0$	
SF1	1	$F_1 \leftarrow 1$	
RF2	1	$F_2 \leftarrow 0$	
SF2	1	$F_2 \leftarrow 1$	
RF3	1	$F_3 \leftarrow 0$	
SF3	1	$F_3 \leftarrow 1$	
RF4	1	$F_4 \leftarrow 0$	
SF4	1	$F_4 \leftarrow 1$	
RF5	1	$F_5 \leftarrow 0$	
SF5	1	$F_5 \leftarrow 1$	
RF6	1	$F_6 \leftarrow 0$	
SF6	1	$F_6 \leftarrow 1$	
RF7	1	$F_7 \leftarrow 0$	
SF7	1	$F_7 \leftarrow 1$	
RF8	1	$F_8 \leftarrow 0$	
SF8	1	$F_8 \leftarrow 1$	
RF9	1	$F_9 \leftarrow 0$	
SF9	1	$F_9 \leftarrow 1$	
RF0	1	$F_0 \leftarrow 0$	
SF0	1	$F_0 \leftarrow 1$	
NOP	1	No Operation	

μCOM-42 SINGLE CHIP MICROCOMPUTER

DESCRIPTION

The μPD548 is the only version of the μCOM-42. This PMOS, −10 volt part is designed to have TTL-level compatible inputs and was specifically designed for external RAM expansion. As a μCOM-42, it includes 1920 x 10 ROM, 96 x 4 RAM and 35 I/O lines in a 42 pin plastic dual-in-line package.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +70°C
Storage Temperature	−40°C to +125°C
Supply Voltage V_{GG}	−15 to +0.3 Volts
Input Voltages	−40 to +0.3 Volts
Output Voltages	−40 to +0.3 Volts

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = −10°C to +70°C; V_{GG} = −10V ± 10%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input High Voltage	V_{IH}	0		− 2.0	V	
Input Low Voltage	V_{IL}	-4.3		V_{GG}	V	
Output High Voltage	V_{OH1}			− 3.0	V	I_{OH} = −4 mA ①
Output High Voltage	V_{OH2}			− 1.0	V	I_{OH} = −1 mA (for S port outputs)
Input Leakage Current High	I_{LIH}			+10	μA	V_I = −1V
Input Leakage Current Low	I_{LIL}			-30	μA	V_I = −36V
Output Current High	I_{OH}	-1.0			mA	V_{OH} = −1V
Output Leakage Current Low	I_{LOL1}			-30	μA	V_O = −36V
Output Leakage Current Low	I_{LOL2}			-10	μA	V_O = −5V (for S port outputs)
Supply Current	I_{GG}		-30	-60	mA	

Note: ① For R port, and when only 1 bit is ON (high level)

AC CHARACTERISTICS

T_a = −10°C to +70°C; V_{GG} = −10V ± 10%, unless otherwise noted

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Frequency	fϕ	100		200	KHz	
Clock Pulse Width	tϕw	2.25			μs	
Clock Rise-Fall Time	tr, tf			0.5	μs	

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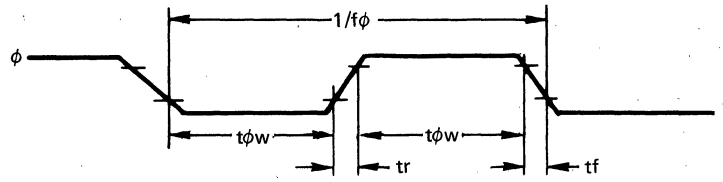
μPD548

T_a = 25°C; V_{GG} = −10V ± 10%, unless otherwise noted.

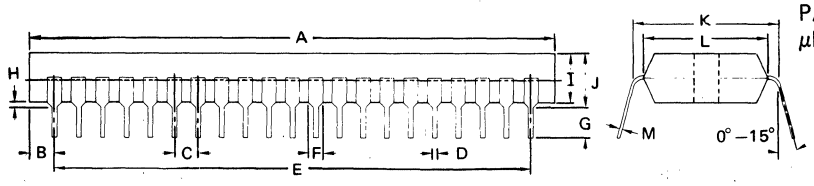
CAPACITANCE

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Capacitance, Any Input Except S	C_I			15	pF	f = 1 MHz
Capacitance, Any Output Except S	C_O			15	pF	
S Port Capacitance	C_{IO}			15	pF	

CLOCK WAVEFORM



PACKAGE OUTLINE
μPD548C



ITEM	MILLIMETERS	INCHES
A	56.0 MAX	2.2 MAX
B	2.6 MAX	0.1 MAX
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	50.8	2.0
F	1.5	0.059
G	3.2 MIN	0.126 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.20 MAX
J	5.72 MAX	0.22 MAX
K	15.24	0.6
L	13.2	0.52
M	0.3 ± 0.1	0.01 ± 0.004