

NEC Microcomputers, Inc.

NEC
 μ PD550

μ COM-45 SINGLE CHIP MICROCOMPUTER

DESCRIPTION The μ PD550 is the 640 x 8 ROM version of the μ COM-45. This PMOS, -10 volt part features both TTL-level compatible inputs as well as outputs capable of being pulled to -35 volts. This allows direct interfacing with Fluorescent Indicator Panels (FIPs). As a μ COM-45, it includes 32 x 4 RAM and 21 I/O lines in a 28 pin plastic dual-in-line package.

ABSOLUTE MAXIMUM RATINGS*					-10°C to +70°C
Operating Temperature					-10°C to +70°C
Storage Temperature					-40°C to +125°C
Supply Voltage					-15 to +0.3 Volts
Input Voltages (Port A, INT, RES, TEST)					-15 to +0.3 Volts
(All Other Inputs)					-40 to +0.3 Volts
Output Voltages					-40 to +0.3 Volts
Output Current (Ports C, D)					-4 mA
(Ports E, F, G)					-15 mA
(Total Current)					-60 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

* $T_a = 25^\circ\text{C}$.

DC/AC CHARACTERISTICS $T_a = -10^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{GG} = -10\text{V} \pm 10\%$.

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	Typ	MAX		
Input High Voltage	V_{IH}	0		-2.0	V	Ports A, C, D, INT, RES
Input Low Voltage	V_{IL1}	-4.3		V_{GG}	V	Ports A, INT, RES
	V_{IL2}	-4.3		-35	V	Port C and D
Input Leakage Current High	I_{LIH}			+10	μA	Ports A, INT, RES, TEST $V_I = 1\text{V}$
Input Leakage Current Low	I_{LIL1}			-10	μA	Ports A, INT, RES, TEST $V_I = -11\text{V}$
	I_{LIL2}			-30	μA	Port A $V_I = -35\text{V}$
I/O Leakage Current High	I_{IOH}			+10	μA	Ports C and D $V_I = -1\text{V}$
I/O Leakage Current Low	I_{IOL1}			-10	μA	Ports C and D $V_I = -11\text{V}$
	I_{IOL2}			-30	μA	Ports C and D $V_I = -35\text{V}$
Output Voltage	V_{OH1}			-1.0	V	Ports C and D $I_O = -2\text{ mA}$
	V_{OH2}			-2.5	V	Ports E, F, G $I_O = -10\text{ mA}$
Output Leakage Current	I_{OL1}			-10	μA	Ports C, D, E, F, G $V_O = -11\text{V}$
	I_{OL2}			-30	μA	Ports C, D, E, F, G $V_O = -35\text{V}$
Supply Current	I_{GG}		-20	-40	mA	
Oscillator Frequency	F	150		440	KHz	

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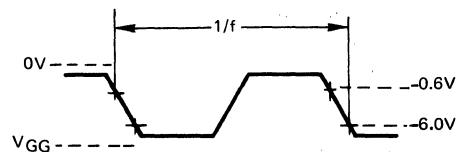
μ PD550

$T_a = 25^\circ\text{C}$, $f = 1 \text{ MHz}$

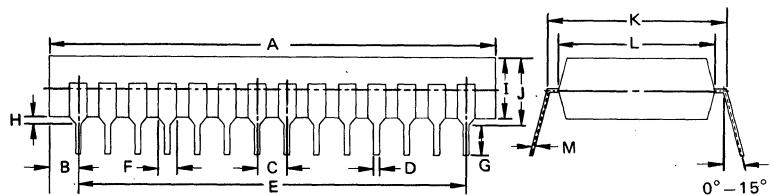
CAPACITANCE

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance	C_I			15	pf	
Output Capacitance	C_O			15	pf	$f = 1 \text{ MHz}$
Input/Output Capacitance	C_{IO}			15	pf	

CLOCK WAVEFORM



PACKAGE OUTLINE μ PD550C



ITEM	MILLIMETERS	INCHES
A	38.0 MAX.	1.496 MAX.
B	2.49	0.098
C	2.54	0.10
D	0.5 ± 0.1	0.02 ± 0.004
E	33.02	1.3
F	1.5	0.059
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	5.22 MAX.	0.205 MAX.
J	5.72 MAX.	0.225 MAX.
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$