MATHSTAR™

August 2006

Arrix™ Family Product Brief

1 GHz Field Programmable Object Array™

FPOA™ Overview

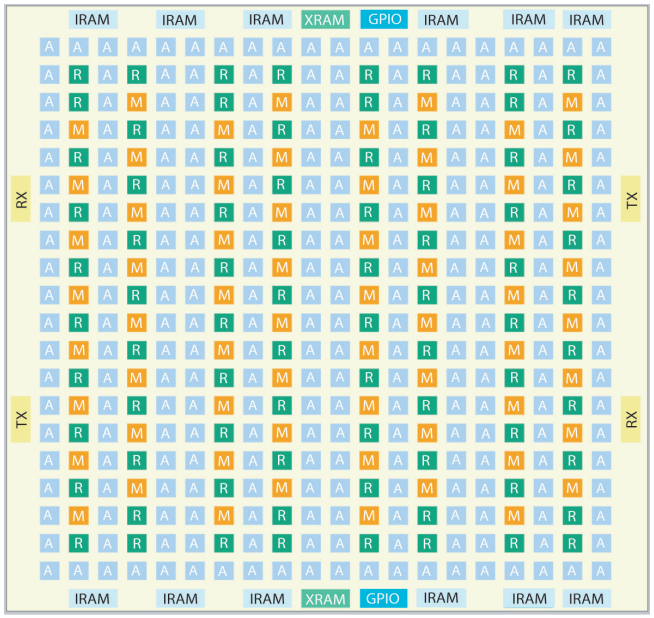
The Arrix family of 1 GHz Field Programmable Object Arrays is the second generation of FPOA products from MathStar. The Arrix family of FPOAs delivers up to four times the performance of today's top FPGAs. The FPOA combines high-performance and re-programmability to meet a wide variety of application needs. FPOAs operate deterministically at 1 GHz and therefore do not suffer from timing closure delays.

The Arrix family of FPOAs provides 256 Arithmetic Logic Unit (ALU), 80 Register File (RF), and 64 Multiply Accumulator (MAC) objects. The 1 GHz interconnect fabric joins each object to the array through 8 nearest neighbors and 10 Party Line connections. The Arrix family object array and associated I/O are shown below:

FPOA Applications:

- Digital Signal Processing
- Machine Vision
- Professional Video
- Image Processing
- Medical Imaging
- Test and Measurement
- Military/Aerospace

Discover our application-specific libraries at **www.mathstar.com**



A	Arithmetic Logic Units
R	Register Files
M	Multiply/Accumulators
IRAM	Internal SRAM Banks
XRAM	External Memory Interfaces
GPIO	General Purpose I/O Banks
TX	High Speed Transmit Ports
RX	High Speed Receive Ports

Arrix Family Silicon Object and I/O Specifications

Resources	Number	Operating Speed	Size Each	Total Capability
ALU	256 objects	Up to 1 GHz	16 bits + control logic	One operation per clock
RF	80 objects	Up to 1 GHz	128 Byte + 80 tag bits	One operation per clock
MAC	64 objects	Up to 1 GHz	16x16 bit multiplier	One operation per clock
Internal RAM	12 banks	Up to 700 MHz	2K x 76 bits	84 GBytes/sec total
External RAM	2 interfaces	Up to 266 MHz DDR	36 bit RLDRAM II	4.8 GBytes/sec total
GPIO	2 banks	Up to 100 MHz	48 pins per bank	96 pins
High Speed I/O Transmit	2 ports	18-500 MHz DDR	16 + 1 bit LVDS	32 Gbps
High Speed I/O Receive	2 ports	250-500 MHz DDR	16 + 1 bit LVDS	32 Gbps

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Array Object - Programming Features

A Arithmetic Logic Unit (ALU)
16 bit data path
4 fully programmable control bits
8 instruction state machine per ALU
Each state programmable with over 20 instructions
(Add/Sub, shift/rotate, AND/OR/XOR, etc.)

R Register File (RF)
Configurable to 64 entries of 16 + 4 bit data or 32 entries of 32 + 8 bit data
Three operational modes
- Dual ported RAM
- Single-cycle, dual-ported FIFO
- Single-cycle Read Sequential/Write Random

M Multiply Accumulator (MAC)
16 x 16 single cycle throughput multiplier
32 bit intermediate result, signed or unsigned
40 bit accumulator, 256 MACs before overflow

IRAM Internal RAM
12 independent blocks of 19 KB each (packed)
Each block is 2K deep and 76 bits wide
Single cycle access up to 700 MHz
Two cycle access up to 1 GHz
228 KB maximum memory size (packed)

Periphery Object - Programming Features

XRAM External RAM
2 Independent RLDRAM II memory controllers
Each controller runs up to 266 MHz DDR
Each controller is 36 bits wide
144 MB maximum memory size per interface (packed)
2.394 GB/s maximum throughput per interface

TX High Speed Transmit ports
Two independent transmit interfaces
16+1 or 8+1 bit width configuration
Operation from 18 MHz to 500 MHz DDR
Operation up to 640 MHz SDR
Up to 16 Gbps data throughput per interface

RX High Speed Receive ports
Two independent receive interfaces
16+1 or 8+1 bit width configuration
Operation from 250 MHz to 500 MHz DDR
Operation up to 640 MHz SDR
Up to 16 Gbps data throughput per interface

GPIO General Purpose I/O
96 pins total - 2 banks of 48 pins each
Operation up to 100 MHz SDR
LVCMOS: 2.5 V and 3.3 V tolerant
Highly programmable clocking - internal, external or asynchronous

Packaging - Environmental Specifications

Operating Parameter	Minimum	Nominal	Maximum
Voltage	1.14 V	1.2 V	1.26 V
Junction Temperature	-40° C	85 ° C	125 ° C
Package Size	n/a	31 x 31 mm	n/a

Arrix Product Family Ordering Information

Maximum Operating Frequency	Product Code	Package
1 GHz	MOA2400D-10	HFCBGA-896
800 MHz	MOA2400D-08	HFCBGA-896
400 MHz	MOA2400D-04	HFCBGA-896

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