Am8080A/9080A

8-Bit Microprocessor

Distinctive Characteristics

- Plug-in replacements for 8080A, 8080A-1, 8080A-2
- High-speed version with 1μsec instruction cycle
- Military temperature range operation to 1.5μsec
- Ion-implanted, n-channel, silicon-gate MOS technology
- 3.2mA of output drive at 0.4V (two full TTL loads)
- 700mV of high, 400mV of low level noise immunity
- 820mW maximum power dissipation at ±5% power
- 100% reliability assurance testing to MIL-STD-883

GENERAL DESCRIPTION

The Am9080A products are complete, general-purpose, single-chip digital processors. They are fixed instruction set, parallel, 8-bit units fabricated with Advanced N-Channel Silicon Gate MOS technology. When combined with external memory and peripheral devices, powerful microcomputer systems are formed. The Am9080A may be used to perform a wide variety of operations, ranging from complex arithmetic calculations to character handling to bit control. Several versions are available offering a range of performance options.

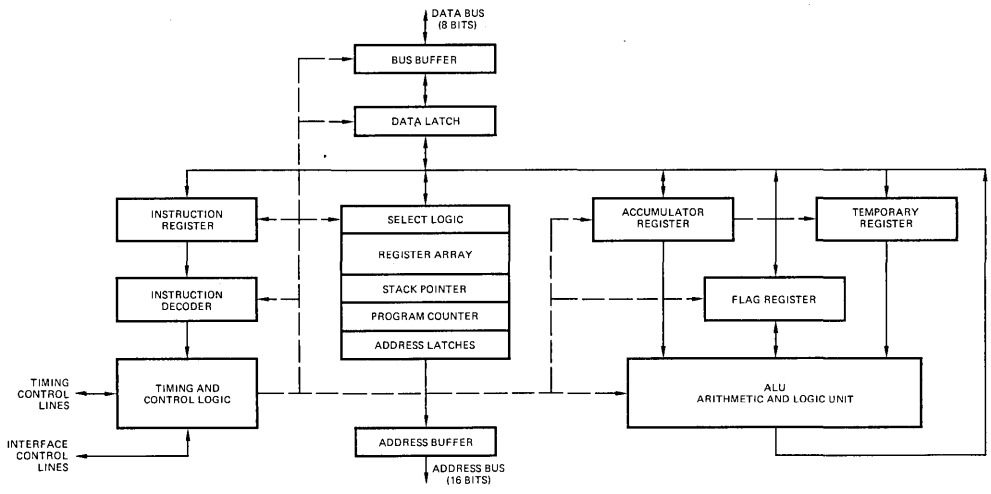
The processor has a 16-bit address bus that may be used to directly address up to 64K bytes of memory. The memory may be any combination of read/write and read-only. Data are transferred into or out of the processor on a bi-directional 8-bit data bus that is separate from the address lines. The data bus transfers instructions, data and status information between system devices. All transfers are handled using asynchronous handshaking controls so that any speed memory or I/O device is easily accommodated.

An accumulator plus six general purpose registers are available to the programmer. The six registers are each 8 bits long and may be used singly or in pairs for both 8 and 16-bit operations. The accumulator forms the primary working register and is the destination for many of the arithmetic and logic operations.

A general purpose push-down stack is an important part of the processor architecture. The contents of the stack reside in R/W memory and the control logic, including a 16-bit stack pointer, is located on the processor chip. Subroutine call and return instructions automatically use the stack to store and retrieve the contents of the program counter. Push and Pop instructions allow direct use of the stack for storing operands, passing parameters and saving the machine state.

An asynchronous vectored interrupt capability is included to allow external signals to modify the instruction stream. The interrupting device may specify an interrupt instruction to be executed and may thus vector the program to a particular service location, or perform some other direct function. Direct memory access (DMA) capability is also included.

BLOCK DIAGRAM



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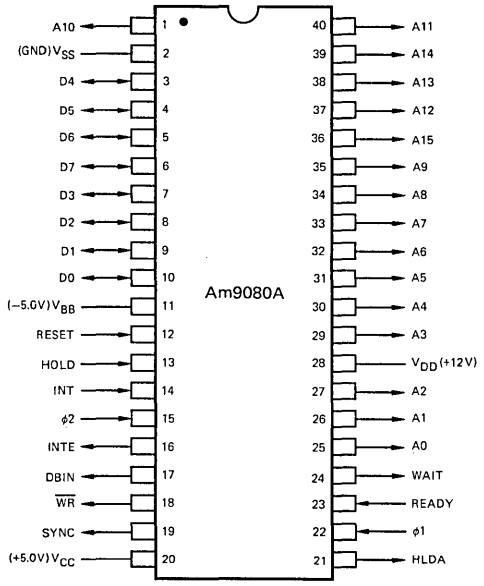
ORDERING INFORMATION

Package Type	Ambient Temperature Specification	Minimum Clock Period			
		250ns	320ns	380ns	480ns
Hermetic DIP*	0°C ≤ T_A ≤ +70°C	AM9080A-4DC AM9080A-4CC	AM9080A-1DC AM9080A-1CC D8080A-1	AM9080A-2DC AM9080A-2CC D8080A-2	AM9080ADC AM9080ACC D8080A
Molded DIP		AM9080A-4PC	AM9080A-1PC P8080A-1	AM9080A-2PC P8080A-2	AM9080APC P8080A
Hermetic DIP	−55°C ≤ T_A ≤ +125°C			AM9080A-2DM	AM9080ADM AM8080A

*Hermetic = Ceramic = DC = CC = D-40-1.

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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INTERFACE SIGNAL SUMMARY

TYPE	PINS	ABBREVIATION	SIGNAL
INPUT	1	V_{SS}	Ground
INPUT	3	V_{DD}, V_{CC}, V_{BB}	+12V, +5V, −5V Supplies
INPUT	2	$\phi 1$, $\phi 2$	Clocks
INPUT	1	RESET	Reset
INPUT	1	HOLD	Hold
INPUT	1	INT	Interrupt
INPUT	1	READY	Ready
IN/OUT	8	D_0–D_7	Data Bus
OUTPUT	16	A_0–A_{15}	Address
OUTPUT	1	INTE	Interrupt Enable
OUTPUT	1	DBIN	Data Bus In Control
OUTPUT	1	$\overline{WR}$	Write Not
OUTPUT	1	SYNC	Cycle Synchronization
OUTPUT	1	HLDA	Hold Acknowledge
OUTPUT	1	WAIT	Wait

INTERFACE SIGNAL DESCRIPTION

$\phi 1$, $\phi 2$ The Clock inputs provide basic timing generation for all internal operations. They are non-overlapping two phase, high level signals. All other inputs to the processor are TTL compatible.

RESET The Reset input initializes the processor by clearing the program counter, the instruction register, the interrupt enable flip-flop and the hold acknowledge flip-flop. The Reset signal should be active for at least three clock periods. The general registers are not cleared.

HOLD The Hold input allows an external signal to cause the processor to relinquish control over the address lines and the data bus. When Hold goes active, the processor completes its current operation, activates the Hlda output, and puts the 3-state address and data lines into their high-impedance state. The Holding device can then utilize the address and data busses without interference.

READY The Ready input synchronizes the processor with external units. When Ready is absent, indicating the external operation is not complete, the processor will enter the Wait state. It will remain in the Wait state until the clock cycle following the appearance of Ready.

INT The Interrupt input signal provides a mechanism for external devices to modify the instruction flow of the program in progress. Interrupt requests are handled efficiently with the vectored interrupt procedure and the general purpose stack. Interrupt processing is described in more detail on the next page.

D_0-D_7 The Data Bus is comprised of 8 bidirectional signal lines for transferring data, instructions and status information between the processor and all external units.

A_0-A_{15} The Address Bus is comprised of 16 output signal lines used to address memory and peripheral devices.

SYNC The Sync output indicates the start of each processor cycle and the presence of processor status information on the data bus.

DBIN The Data Bus In output signal indicates that the bidirectional data bus is in the input mode and incoming data may be gated onto the Data Bus.

WAIT The Wait output indicates that the processor has entered the Wait state and is prepared to accept a Ready from the current external operation.

$\overline{WR}$ The Write output indicates the validity of output on the data bus during a write operation.

HLDA The Hold Acknowledge output signal is a response to a Hold input. It indicates that processor activity has been suspended and the Address and Data Bus signals will enter their high impedance state.

INTE The Interrupt Enable output signal shows the status of the interrupt enable flip-flop, indicating whether or not the processor will accept interrupts.

INSTRUCTION SET INTRODUCTION

The instructions executed by the Am9080A are variable length and may be one, two or three bytes long. The length is determined by the nature of the operation being performed and the addressing mode being used.

The instruction summary shows the number of successive memory bytes occupied by each instruction, the number of clock cycles required for the execution of the instruction, the binary coding of the first byte of each instruction, the mnemonic coding used by assemblers and a brief description of each operation. Some branch-type instructions have two execution times depending on whether the conditional branch is taken or not. Some fields in the binary code are labeled with alphabetic abbreviations. That shown as **vvv** is the address pointer used in the one-byte Call instruction (RST). Those shown as **ddd** or **sss** designate destination and source register fields that may be filled as follows:

111 A register
000 B register
001 C register
010 D register
011 E register
100 H register
101 L register
110 Memory

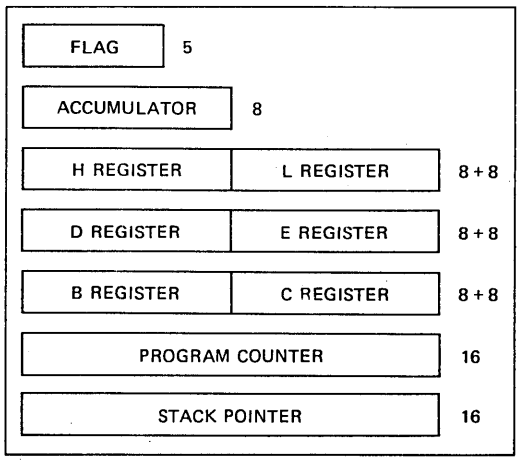
The register diagram shows the internal registers that are directly available to the programmer. The accumulator is the primary working register for the processor and is a specified or implied operand in many instructions. All I/O operations take place via the accumulator. Registers H, L, D, E, B and C may be used singly or in the indicated pairs. The H and L pair is the implied address pointer for many instructions.

The Flag register stores the program status bits used by the conditional branch instructions: carry, zero, sign and parity. The fifth flag bit is the intermediate carry bit. The flags and the accumulator can be stored on or retrieved from the stack with a single instruction. Bit positions in the flag register when pushed onto the stack (PUSH PSW) are:

7	6	5	4	3	2	1	0
S	Z	0	CY1	0	P	1	CY2

where S = sign, Z = zero, CY1 = intermediate carry, P = parity, CY2 = carry.

REGISTER DIAGRAM



During Sync time at the beginning of each instruction cycle the data bus contains operation status information that describes the machine cycle being executed. Positions for the status bits are:

7	6	5	4	3	2	1	0
MEMR	INP	M1	OUT	HLTA	STK	$\overline{WO}$	INTA

STATUS DEFINITION:

INTA Interrupt Acknowledge. Occurs in response to an Interrupt input and indicates that the processor will be ready for an interrupt instruction on the data bus when DBIN goes true.

$\overline{WO}$ Write or Output indicated when signal is low. When high, a Read or Input will occur.

STK Stack indicates that the content of the stack pointer is on the address bus.

HLTA Halt Acknowledge.

OUT Output instruction is being executed.

M1 First instruction byte is being fetched.

INP Input instruction is being executed.

MEMR Memory Read operation.

INTERRUPT PROCESSING

When the processor interrupt mechanism is enabled (INTE=1), interrupt signals from external devices will be recognized unless the processor is in the Hold State. In handling an interrupt, the processor will complete the execution of the current instruction, disable further interrupts and respond with INTA status instead of executing the next sequential instruction in the interrupted program.

The interrupting device should supply an instruction opcode to the processor during the next DBIN time after INTA status appears.

Any opcode may be used except XTHL. If the instruction supplied is a single byte instruction, it will be executed. (The usual single byte instruction utilized is RST.) If the interrupt instruction is two or three bytes long, the next one or two processor cycles, as indicated by the DBIN signal, should be used by the external device to supply the succeeding byte(s) of the interrupt instruction. Note that INTA status from the processor is not present during these operations.

If the interrupt instruction is not some form of CALL, it is executed normally by the processor except that the Program Counter is not incremented. The next instruction in the interrupted program is then fetched and executed. Notice that the interrupt mechanism must be re-enabled by the processor before another interrupt can occur.

If the interrupt instruction is some form of CALL, it is executed normally. The Program Counter is stored and control transferred to the interrupt service subroutine. This routine has responsibility for saving and restoring the machine state and for re-enabling interrupts if desired. When the interrupt service is complete, a RETURN instruction will transfer control back to the interrupted program.

INSTRUCTION SET SUMMARY

Op Code |7|6|5|4|3|2|1|0	No. of Bytes	Clock Cycles	Assembly Mnemonic	Instruction Description
DATA TRANSFER				
01dddsss	1	5	MOVr, r	Move register to register
01110sss	1	7	MOVm, r	Move register to memory
01ddd110	1	7	MOVr, m	Move memory to register
00ddd110	2	7	MVI, r	Move to register, immediate
00110110	2	10	MVI, m	Move to memory, immediate
00111010	3	13	LDA	Load Acc, direct
00001010	1	7	LDAX B	Load Acc, indirect via B & C
00011010	1	7	LDAX D	Load Acc, indirect via D & E
00101010	3	16	LHLD	Load H & L, direct
00100001	3	10	LXI H	Load H & L, immediate
00010001	3	10	LXI D	Load D & E, immediate
00000001	3	10	LXI B	Load B & C, immediate
00110001	3	10	LXI SP	Load stack pointer, immediate
00100010	3	16	SHLD	Store H & L, direct
00110010	3	13	STA	Store Acc, direct
00000010	1	7	STAX B	Store Acc, indirect via B & C
00010010	1	7	STAX D	Store Acc, indirect via D & E
11111001	1	5	SPHL	Transfer H & L to stack pointer
11101011	1	4	XCHG	Exchange D & E with H & L
11100011	1	18	XTHL	Exchange top of stack with H & L
11011011	2	10	IN	Input to Acc
11010011	2	10	OUT	Output from Acc
CONTROL				
01110110	1	7	HLT	Halt and enter wait state
00110111	1	4	STC	Set carry flag
00111111	1	4	CMC	Compliment carry flag
11111011	1	4	EI	Enable interrupts
11110011	1	4	DI	Disable interrupts
00000000	1	4	NOP	No operation
BRANCH				
11000011	3	10	JMP	Jump unconditionally
11011010	3	10	JC	Jump on carry
11010010	3	10	JNC	Jump on no carry
11001010	3	10	JZ	Jump on zero
11000010	3	10	JNZ	Jump on not zero
11110010	3	10	JP	Jump on positive
11111010	3	10	JM	Jump on minus
11101010	3	10	JPE	Jump on parity even
11100010	3	10	JPO	Jump on parity odd
11001101	3	17	CALL	Call unconditionally
11011100	3	17-11	CC	Call on carry
11010100	3	17-11	CNC	Call on no carry
11001100	3	17-11	CZ	Call on zero
11000100	3	17-11	CNZ	Call on not zero
11110100	3	17-11	CP	Call on positive
11111100	3	17-11	CM	Call on minus
11101100	3	17-11	CPE	Call on parity even
11100100	3	17-11	CPO	Call on parity odd
11001001	1	10	RET	Return unconditionally
11011000	1	11-5	RC	Return on carry
11010000	1	11-5	RNC	Return on no carry
11001000	1	11-5	RZ	Return on zero
11000000	1	11-5	RNZ	Return on not zero
11110000	1	11-5	RP	Return on positive
11111000	1	11-5	RM	Return on minus
11101000	1	11-5	RPE	Return on parity even
11100000	1	11-5	RPO	Return on parity odd
11101001	1	5	PCHL	Jump unconditionally, indirect via H & L
11VVV111	1	11	RST	Restart

Op Code |7|6|5|4|3|2|1|0	No. of Bytes	Clock Cycles	Assembly Mnemonic	Instruction Description
ARITHMETIC				
10000sss	1	4	ADDr	Add register to Acc
10001sss	1	4	ADCr	Add with carry register to Acc
10000110	1	7	ADDm	Add memory to Acc
10001110	1	7	ADCm	Add with carry memory to Acc
11000110	2	7	ADI	Add to Acc, immediate
11001110	2	7	ACI	Add with carry to Acc, immediate
00001001	1	10	DAD B	Double add B & C to H & L
00011001	1	10	DAD D	Double add D & E to H & L
00101001	1	10	DAD H	Double add H & L to H & L
00111001	1	10	DAD SP	Double add stack pointer to H & L
10010sss	1	4	SUBr	Subtract register from Acc
10011sss	1	4	SBBr	Subtract with borrow register from Acc
10010110	1	7	SUBm	Subtract memory from Acc
10011110	1	7	SBBm	Subtract with borrow memory from Acc
11010110	2	7	SUI	Subtract from Acc, immediate
11011110	2	7	SBI	Subtract with borrow from Acc, immediate
00100111	1	4	DAA	Decimal adjust Acc
STACK OPERATIONS				
11000101	1	11	PUSH B	Push registers B & C on stack
11010101	1	11	PUSH D	Push registers D & E on stack
11100101	1	11	PUSH H	Push registers H & L on stack
11110101	1	11	PUSH PSW	Push Acc and flags on stack
11000001	1	10	POP B	Pop registers B & C off stack
11010001	1	10	POP D	Pop registers D & E off stack
11100001	1	10	POP H	Pop registers H & L off stack
11110001	1	10	POP PSW	Pop Acc and flags off stack
LOGICAL				
10100sss	1	4	ANA r	And register with Acc
10100110	1	7	ANA m	And memory with Acc
11100110	2	7	ANI	And with Acc, immediate
10101sss	1	4	XRA r	Exclusive or register with Acc
10101110	1	7	XRA m	Exclusive Or memory with Acc
11101110	2	7	XRI	Exclusive Or with Acc, immediate
10110sss	1	4	ORA r	Inclusive Or register with Acc
10110110	1	7	ORA m	Inclusive Or memory with Acc
11110110	2	7	ORI	Inclusive Or with Acc, immediate
10111sss	1	4	CMP r	Compare register with Acc
10111110	1	7	CMP m	Compare memory with Acc
11111110	2	7	CPI	Compare with Acc, immediate
00101111	1	4	CMA	Compliment Acc
00000111	1	4	RLC	Rotate Acc left
00001111	1	4	RRC	Rotate Acc right
00010111	1	4	RAL	Rotate Acc left through carry
00011111	1	4	RAR	Rotate Acc right through carry
INCREMENT/DECREMENT				
00ddd100	1	5	INR r	Increment register
00110100	1	10	INR m	Increment memory
00000011	1	5	INX B	Increment extended B & C
00010011	1	5	INX D	Increment extended D & E
00100011	1	5	INX H	Increment extended H & L
00110011	1	5	INX SP	Increment stack pointer
00ddd101	1	5	DCR r	Decrement register
00110101	1	10	DCR m	Decrement memory
00001011	1	5	DCX B	Decrement extended B & C
00011011	1	5	DCX D	Decrement extended D & E
00101011	1	5	DCX H	Decrement extended H & L
00111011	1	5	DCX SP	Decrement stack pointer

MAXIMUM RATINGS (Above which useful life may be impaired)

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	−55°C to +125°C
All Signal Voltages With Respect to V_{BB}	−0.3V to +20V
All Supply Voltages With Respect to V_{BB}	−0.3V to +20V
Power Dissipation	1.5W

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGE

Part Number	T_A	V_{DD}	V_{CC}	V_{BB}	V_{SS}
Am9080A-XCC Am9080A-XPC D8080A-X P8080A-X	0°C to +70°C	+12V ±5%	+5.0V ±5%	−5.0V ±5%	0V
Am9080A-XDM M8080A	−55°C to +125°C	+12V ±10%	+5.0V ±10%	−5.0V ±10%	0V

No signal or supply voltage should ever be greater than 0.3V more negative than V_{BB}.

ELECTRICAL CHARACTERISTICS

over operating range (note 1)

Parameters	Description	Test Conditions		P8080A-X D8080A-X Min.	Typ.	Max.	Am9080A-XPC Am9080A-XCC Min.	Typ.	Max.	Am9080A-XDM M8080A Min.	Typ.	Max.	Units
V_{IL}	Input LOW Voltage			−1.0		0.8	−1.0		0.8	−1.0		0.8	Volts
V_{IH}	Input HIGH Voltage			3.3		V_{CC}+1	3.0		V_{CC}+1	3.0		V_{CC}+1	Volts
V_{ILC}	Input LOW Voltage, Clock			−1.0		0.8	−1.0		0.8	−1.0		0.8	Volts
V_{IHC}	Input HIGH Voltage, Clock	A-4					V_{DD}−2		V_{DD}+1				Volts
		A-1		9.0		V_{DD}+1	9.0		V_{DD}+1	V_{DD}−2		V_{DD}+1	
		A-2		9.0		V_{DD}+1	9.0		V_{DD}+1	V_{DD}−2		V_{DD}+1	
		A		9.0		V_{DD}+1	9.0		V_{DD}+1	V_{DD}−2		V_{DD}+1	
V_{OL}	Output LOW Voltage	I_{OL} = 3.2mA							0.40			0.40	Volts
		I_{OL} = 1.9mA				0.45							
V_{OH}	Output HIGH Voltage	I_{OH} = −200μA					3.7			3.7			Volts
		I_{OH} = −150μA		3.7									
I_{DD}(AV)	V_{DD} Supply Current, Average	Operating, Minimum Clock Period	−55°C								50	80	mA
			0°C			70		40	70		45	75	
			25°C		40			35	65		40	70	
			70°C					30	55		35	60	
			125°C								30	50	
I_{CC}(AV)	V_{CC} Supply Current, Average	Operating, Minimum Clock Period	−55°C								45	60	mA
			0°C			80		35	50		40	55	
			25°C		60			30	45		35	50	
			70°C					25	40		30	45	
			125°C								25	40	
I_{BB}(AV)	V_{BB} Supply Current, Average	Operating, Minimum Clock Period				1.0			1.0			1.0	mA
I_{IL}	Input Leakage Current	(Note 4)				±10			±10			±10	μA
I_{CL}	Clock Leakage Current	$V_{SS} \leq V_\phi \leq V_{DD}$				±10			±10			±10	μA
I_{DL}	Data Bus Current,	$V_{IN} \leq V_{SS}$ + 0.8V				−100			−100			−100	μA
	Input Mode (Note 2)	$V_{IN} \geq V_{SS}$ + 0.8V				−2.0			−2.0			−2.0	mA
I_{FL}	Address and Data Bus	$V_{A/D} = V_{CC}$				10			10			10	μA
	Leakage in OFF State	$V_{A/D} = V_{SS}$				−100			−100			−100	μA

CAPACITANCE

f = 1.0MHz, Inputs = 0V, T_A = 25°C
$V_{DD} = V_{CC} = V_{SS}$ = 0V, V_{BB} = −5.0V

Parameters	Description	Typ.	Max.	Units
C_ϕ	Clock Input Capacitance	12	25	pF
C_I	Input Capacitance	4.0	10	pF
C_O	Output Capacitance	8.0	20	pF
$C_{I/O}$	I/O Capacitance	10	20	pF

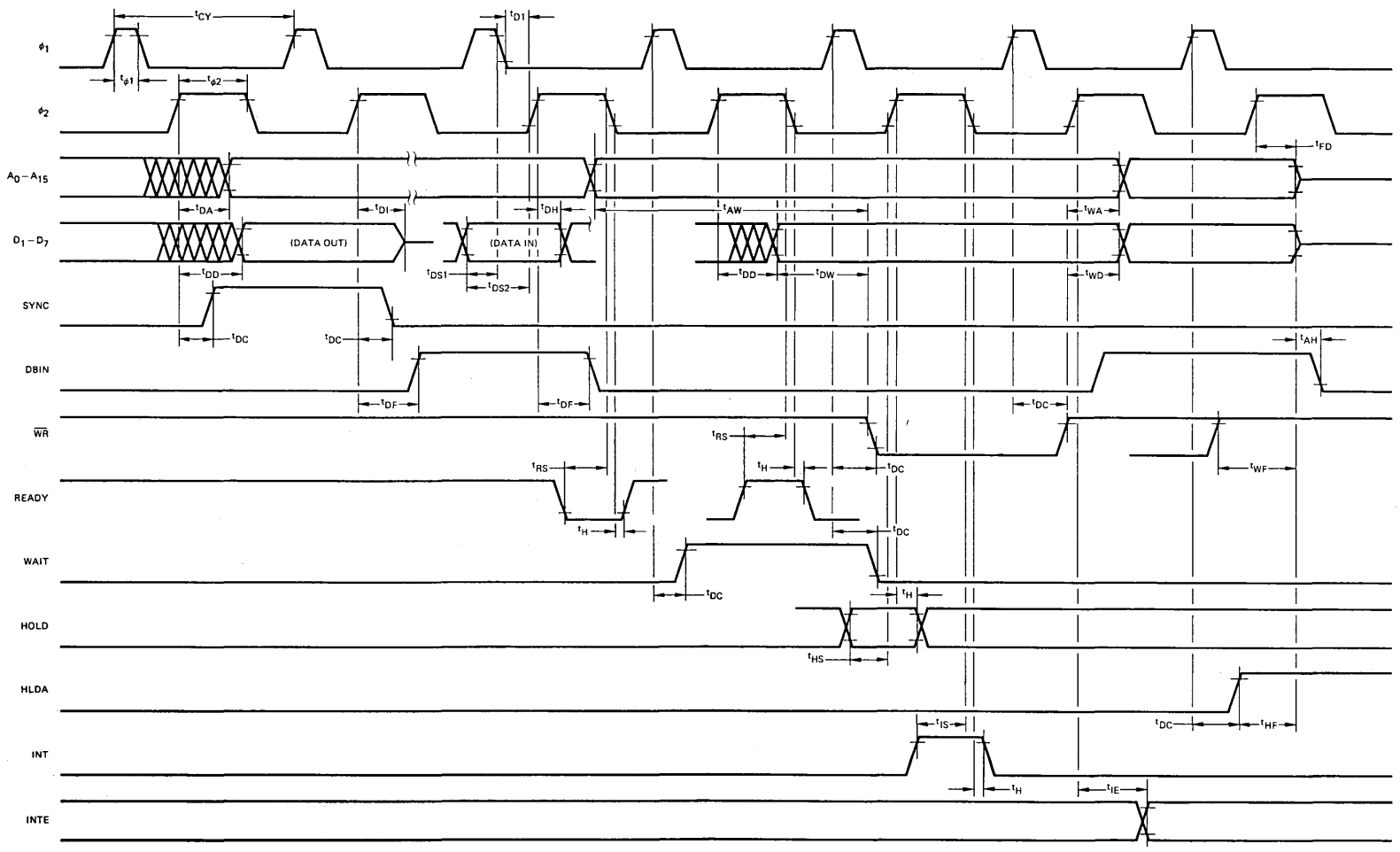
SWITCHING CHARACTERISTICS over operating range (Note 9)

			Am9080A-4		Am9080A-1		Am9080A-2		Am9080A		
Parameters	Description	Test Conditions	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t_{DA}	Clock $\phi 2$ to Address Out Delay	Load Capacitance = 100pF		125		150		175		200	ns
t_{DD}	Clock $\phi 2$ to Data Out Delay			140		180		200		220	ns
t_{DI}	Clock $\phi 2$ to Data Bus Input Mode Delay	(Note 5)		t_{DF}		t_{DF}		t_{DF}		t_{DF}	ns
t_{DS1}	Data In to Clock $\phi 1$ Set-up Time	Both t_{DS1} and t_{DS2} must be satisfied	10		10		20		30		ns
t_{DS2}	Data In to Clock $\phi 2$ Set-up Time		110		120		130		150		ns
t_{DC}	Clock to Control Output Delay	Load Capacitance = 50pF		100		110		120		120	ns
t_{RS}	Ready to Clock $\phi 2$ Set-up Time		80		90		90		120		ns
t_H	Clock $\phi 2$ to Control Signal Hold Time		0		0		0		0		ns
t_{IS}	Interrupt to Clock $\phi 2$ Set-up Time		90		100		100		120		ns
t_{HS}	Hold to Clock $\phi 2$ Set-up Time		100		120		120		140		ns
t_{IE}	Clock $\phi 2$ to INTE Delay	Load Capacitance = 50pF		100		200		200		200	ns
t_{FD}	Clock $\phi 2$ to Address/Data OFF Delay			100		120		120		120	ns
t_{DF}	Clock $\phi 2$ to DBIN Delay	Load Capacitance = 50pF	25	110	25	130	25	140	25	140	ns
t_{DH}	Clock $\phi 2$ to Data In Hold Time	(Note 5)	–	–	–	–	–	–	–	–	ns
t_{AW}	Address Valid to Write Delay	(Note 8)	–	–	–	–	–	–	–	–	ns
t_{DW}	Output Data Valid to Write Delay		–	–	–	–	–	–	–	–	ns
t_{KA}	Address Valid to Write Increment			90		110		130		140	ns
t_{KD}	Output Data Valid to Write Increment			130		150		170		170	ns
t_{WA}	Write to Address Invalid Delay		–	–	–	–	–	–	–	–	ns
t_{WD}	Write to Output Data Invalid Delay		–	–	–	–	–	–	–	–	ns
t_{HF}	HLDA to Address/Data OFF Delay		–	–	–	–	–	–	–	–	ns
t_{WF}	Write to Address/Data OFF Delay		–	–	–	–	–	–	–	–	ns
t_{KH}	HLDA to Address/Data OFF Increment			40		50		50		50	ns
t_{AH}	DBIN to Address Hold Time		0		–20		–20		–20		ns

NOTES:

1. Typical values are at $T_A = 25°C$, nominal supply voltages and nominal processing parameters.
2. Pull-up devices are connected to the Data Bus lines when the input signal is high during DBIN time. When switching the input from HIGH-to-LOW a transient current must be absorbed by the driving device until the input reaches a LOW level.
3. Timing reference levels –
   Clocks: HIGH = 8.0V, LOW = 1.0V
   Inputs: HIGH = 3.3V, LOW = 0.8V
   Outputs: HIGH = 2.0V, LOW = 0.8V
4. Control inputs impress currents on the driving signal during HIGH-to-LOW transitions. Values shown are for logic high or logic low levels. Peak current during transition is as much as 2.0mA.
5. Bus contention cannot occur and data hold times are adequate when DBIN is used to enable Data In. t_{DH} is the smaller of 50ns or t_{DF}.
6. RESET should remain active for at least three clock periods.
7. With interrupts enabled, the interrupted instruction will be one with an interrupt input stable during the indicated interval of the last clock period of the preceding instruction. Additional synchronization not necessary.
8. $t_{AW} = 2\,t_{CY} - t_{D3} - t_r - t_{KA}$
   $t_{DW} = t_{CY} - t_{D3} - t_r - t_{KD}$
   For HLDA Off: $t_{WD} = t_{WA} = t_{D3} + t_r + 10ns$
   For HLDA On: $t_{WD} = t_{WA} = t_{WF}$
   $t_{HF} = t_{D3} + t_r - t_{KH}$
   $t_{WF} = t_{D3} + t_r - 10ns$
   $t_r = \phi 2$ rise time
9. The switching specifications listed for the Am9080A, Am9080A-2, Am9080A-1 meet or exceed the corresponding specifications for the C8080A, C8080A-2, C8080A-1.

SWITCHING WAVEFORMS SUMMARY



This chart presents relative timing waveform relationships and does not show actual processor operating cycles.

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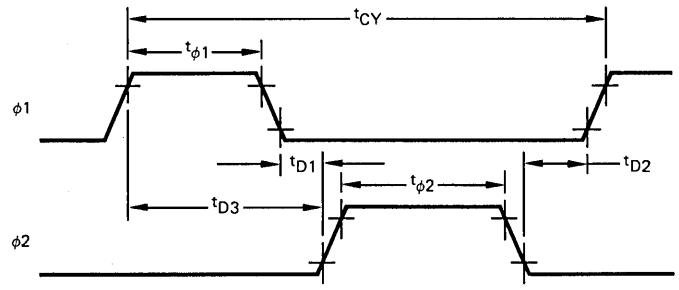
CLOCK WAVEFORM DETAIL



$$t_{CY} = t_{D3} + t_{r\phi 2} + t_{\phi 2} + t_{f\phi 2} + t_{D2} + t_{r\phi 1}$$

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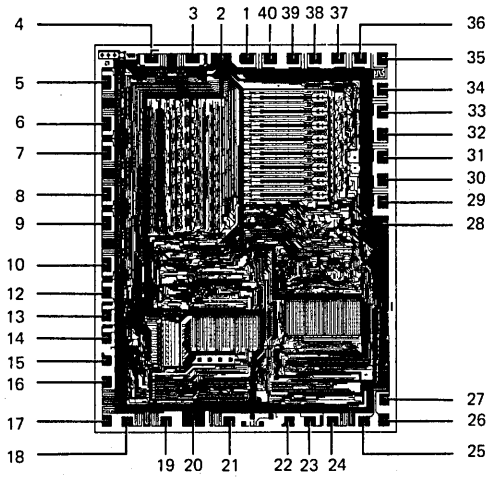
CLOCK SWITCHING CHARACTERISTICS over operating range

Parameters	Description	Am9080A-4 Min.	Am9080A-4 Max.	Am9080A-1 D8080A-1 Min.	Am9080A-1 D8080A-1 Max.	Am9080A-2 D8080A-2 Min.	Am9080A-2 D8080A-2 Max.	Am9080A D8080A Min.	Am9080A D8080A Max.	Units
t_{CY}	Clock Period	250	2000	320	2000	380	2000	480	2000	ns
t_r, t_f	Clock Transition Times	0	15	0	25	0	50	0	50	ns
$t_{\phi 1}$	Clock $\phi 1$ Pulse Width	50		50		60		60		ns
$t_{\phi 2}$	Clock $\phi 2$ Pulse Width	120		145		175		220		ns
t_{D1}	$\phi 1$ to $\phi 2$ Offset	0		0		0		0		ns
t_{D2}	$\phi 2$ to $\phi 1$ Offset	50		60		70		70		ns
t_{D3}	$\phi 1$ to $\phi 2$ Delay	50		60		70		80		ns

Metallization and Pad Layout



Pin 11 connection is substrate.

DIE SIZE 0.132" X 0.170"