AMD

AMD-K6®-III

Processor Revision Guide

Model 9

Publication # **22473** Rev: **C** Amendment/**0**
Issue Date: **July 1999**

Revision History

Date	Rev	Description
July 1999	C	Initial Release

AMD-K6®-III Processor Revision Guide - Model 9

The purpose of the *AMD-K6®-III Processor Revision Guide - Model 9* is to communicate updated product information on the AMD-K6-III processor to designers of computer systems and software developers. Model 9 of the AMD-K6 processor is manufactured in 0.25-micron process technology. This guide consists of four major sections:

- **Product Marking Identification:** This section provides product types, product revisions, OPNs (Ordering Part Numbers), and product marking information.
- **Product Errata:** This section provides a detailed description of product errata, including potential effects on system operation and suggested workarounds. An erratum is defined as a deviation from the product's specification.
- **Specification Changes/Clarifications:** This section provides changes, additions, and clarifications to product specifications.
- **Technical and Documentation Support:** This section provides a listing of available technical support resources. It also lists corrections, modifications, and clarifications to listed documents.

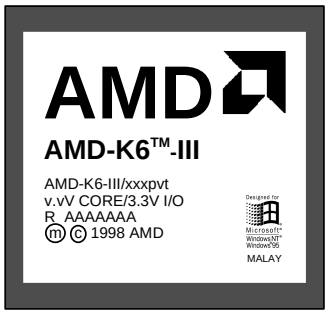
Revision Guide Policy

At times, AMD identifies deviations or changes to the specification of the AMD-K6-III processor. These are documented in the *AMD-K6®-III Processor Revision Guide* as errata or specification changes/clarifications. The descriptions are written to assist system and software designers in using the AMD-K6-III processor. In addition, any corrections to AMD's published documentation on the AMD-K6 processor are included. The errata and specification changes are the result of extensive testing and validation that is done for all AMD products. AMD works closely with system and software designers to ensure the appropriate workarounds or changes are implemented to avoid impact to PC users.

The *AMD-K6®-III Processor Revision Guide* is made publicly available to all who are interested. All issues that have been resolved and communicated to AMD's customers are included in this release.

1 Product Marking Identification

1.1 Production Marking



Ceramic Pin Grid Array (CPGA)

(Package Not Drawn to Scale)

xxxpvt = OPN, where:

- xxx = Operating Frequency
- p = Package Type
  - A = 321-pin PGA
- v = Operating Voltage
  - H = 2.3-2.5V Core/3.135-3.6V I/O
- t = Maximum Case Temperature
  - X = 65°C

v.vV = Core Voltage, where:

- 2.4V = 2.4V Component

R AAAAAAA = Revision, where:

- R = Revision
  - A = Revision A
  - B = Revision B
  - etc.
- AAAAAAA = Internally-Defined

2 Product Errata

This section documents AMD-K6-III processor product errata. The errata are divided into categories to assist referencing particular errata. A unique tracking number for each erratum has been assigned within this document for user convenience in tracking the errata within specific revision levels. Table 2-1 cross-references the revisions of the processor to each erratum. An "X" indicates that the erratum applies to the stepping. The absence of an "X" indicates that the erratum does not apply to the stepping. Shading within the table indicates an addition or modification from the previous release of this document.

Table 2-1. Cross-Reference of Product Revision to Errata

Erratum Number	Description	CPUID Stepping[1]
		1
		Revision
		B
System Bus		
2.1.1	HLDA Assertion Delayed by One Clock	X
2.1.2	Incorrect Address Driven During Writeback Cycle After Inquire Cycle	X
2.1.3	Additional Writeback Cycle After Inquire Cycle	X
Cache Operation		
2.2.1	Writing to the Page Flush/Invalidate Register (PFIR)	X
Notes:		
1.	*The CPUID stepping is returned in EAX[3:0] after executing standard function 1 of the CPUID instruction. The values shown are in hexadecimal format.*	
	Shading indicates additions or modifications from the previous release of this document	

2.1 System Bus

2.1.1 HLDA Assertion Delayed by One Clock

Products Affected. CPUID Stepping 1, revision B

Normal Specified Operation. If BOFF# and HOLD are sampled asserted on the same clock edge that negates ADS#, the processor asserts HLDA one clock edge after HOLD is sampled asserted.

Non-conformance. If BOFF# and HOLD are sampled asserted on the same clock edge that negates ADS#, the processor asserts HLDA two clock edges after HOLD is sampled asserted.

Potential Effect on System. There are three potential effects of this erratum to consider:

- If the system logic asserts BOFF# for a duration of one clock, anticipates the assertion of HLDA in clock 3 (see Figure 1)—which is the normal specified operation—and drives the address bus and EADS# for an inquire cycle in clock 3, then the processor will not sample EADS# asserted. In addition, address bus contention will occur in clock 3.
- If the system logic asserts BOFF# for a duration of two clocks, anticipates the assertion of HLDA in clock 3, and drives the address bus and EADS# for an inquire cycle in clock 3, then the processor will not sample EADS# asserted. (No address bus contention occurs in this case.)
- If the system logic asserts BOFF# for a duration of one clock, anticipates the assertion of HLDA in clock 3, and drives the address bus and EADS# for an inquire cycle in clock 4, then address bus contention may occur in clock 4. (The processor will sample EADS# asserted in this case.)

If the processor does not sample EADS# asserted during an inquire cycle, cache/memory incoherency will occur. Address bus contention can affect the reliability of the processor and the system logic.

Suggested Workaround. The system logic must sample the assertion of HLDA before asserting EADS# and driving the address bus for an inquire cycle—as shown in clock 5 of Figure 1.

Resolution Status. AMD has determined that all Socket 7 and Super7™ chipsets operate as described in the aforementioned suggested workaround. Therefore, AMD has decided to defer the resolution of this erratum until deemed necessary.

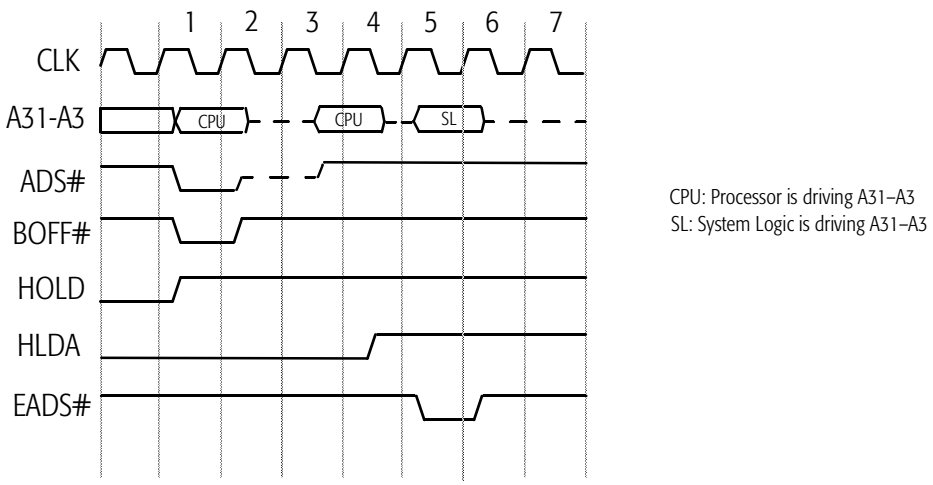


Figure 1. AMD-K6®-III Processor Assertion of HLDA Due to Simultaneous BOFF#/HOLD Assertion

2.1.2 Incorrect Address Driven During Writeback Cycle After Inquire Cycle

Products Affected. CPUID Stepping 1, revision B

Normal Specified Operation. If an inquire cycle hits a cache line in the modified state, the processor performs a writeback cycle. During the writeback cycle, the processor drives the address bus—assuming AHOLD is not sampled asserted by the system logic—with the same address that was sampled on the clock edge on which EADS# was sampled asserted during the inquire cycle. The data bus is driven with the contents of the hit cache line.

Non-conformance. If:

- The processor schedules a replacement writeback for each of the two modified cache lines in a sector, CL0 and CL1 (where CL0 and CL1 correspond to the lower-half [address bit 5 equal to 0] and upper-half [address bit 5 equal to 1] cache lines of the sector, respectively). In this case, the CL0 writeback is scheduled ahead of the CL1 writeback.
- A subsequent internal snoop cycle performed by the processor hits on CL1, in which case the CL1 writeback is scheduled ahead of the CL0 writeback.
- A subsequent inquire cycle hits on CL0.

Then: the processor erroneously drives the address bus and data bus associated with CL1 during the writeback that is performed in response to the inquire cycle that was directed at CL0.

Potential Effect on System. This erratum can lead to unpredictable system behavior. This erratum was detected by inspection and has not been observed in a system while running application or operating system software.

Suggested Workaround. None.

Resolution Status. This erratum will be corrected in a future revision of the AMD-K6-III processor.

2.1.3 Additional Writeback Cycle After Inquire Cycle

Products Affected. CPUID Stepping 1, revisions B

Normal Specified Operation. If an inquire cycle hits a cache line in the modified state, the processor performs a writeback cycle. During the writeback cycle, the processor drives the address bus—assuming AHOLD is not sampled asserted by the system logic—with the same address that was sampled on the clock edge on which EADS# was sampled asserted during the inquire cycle. The data bus is driven with the contents of the hit cache line.

Non-conformance. If:

- The processor misses the L1 data cache during a read, and hits a line in the L2 cache in the modified state (in this case the L1 data cache is supplied from the L2 cache, and the final MESI states of the line in the L1 and L2 caches are modified and exclusive, respectively).
- An inquire cycle hits this particular modified line while the line is being loaded into the L1 data cache from the L2 cache.
- A subsequent internal snoop cycle performed by the processor hits this particular modified line before the line has been completely loaded into the L1 data cache from the L2 cache.

Then: the processor correctly performs a writeback cycle in response to the inquire cycle, but erroneously follows this writeback cycle with another writeback cycle in response to the internal snoop cycle that hit the modified line. The address and data of each writeback cycle are identical, and no intervening processor cycle is executed between these two writebacks.

Potential Effect on System. If the inquire cycle is performed on behalf of an external bus master device that writes to this particular cache line in main memory after the first writeback cycle is completed, the second erroneous writeback cycle overwrites any data written by the bus master device. This erratum was detected by inspection and has not been observed in a system while running application or operating system software.

Suggested Workaround. None.

Resolution Status. This erratum will be corrected in a future revision of the AMD-K6-III processor.

2.2 Cache Operation

2.2.1 Writing to the Page Flush/Invalidate Register (PFIR)

Products Affected. CPUID Stepping 1, revision B

Normal Specified Operation. Writing to the Page Flush/Invalidate Register (PFIR) invalidates and optionally flushes a specified 4-Kbyte page from the cache.

Non-conformance. Writing to the PFIR does not invalidate any L1 instruction cache line that resides in the upper half of every sector in the specified 4-Kbyte page (the upper-half cache line corresponds to address bit 5 equal to 1). The lower-half cache line of every sector in the specified 4-Kbyte page (address bit 5 equals 0) is correctly invalidated.

The L1 data cache and the L2 cache are not affected by this erratum.

Potential Effect on System. If:

- The PFIR is used to invalidate a page, part of which resides in the L1 instruction cache
- An external bus master subsequently writes to main memory locations that correspond to this page without performing invalidating inquire cycles

Then: the processor can erroneously execute 'stale' instructions that were not invalidated by the PFIR operation (as opposed to executing those instructions written to main memory by the external bus master). However, system logic typically performs invalidating inquire cycles for external bus master writes to main memory in order to maintain cache coherency.

This erratum was detected by inspection and has not been observed in a system while running application or operating system software.

Suggested Workaround. The L1 instruction cache can be invalidated by executing the INVD or WBINVD instructions, by performing invalidating inquire cycles, or by asserting the FLUSH# signal.

Resolution Status. This erratum will be corrected in a future revision of the AMD-K6-III processor.

3 Specification Changes/Clarifications

There are no specification changes or clarifications necessary to document for the AMD-K6-III processor.

4 Technical and Documentation Support

4.1 Documentation Support

The following documents provide additional information regarding the operation of the AMD-K6 processor:

- AMD-K6®-III Processor Data Sheet (order# 21918)
- 3DNow!™ Technology Manual (order# 21928)
- AMD-K6®-2 Processor Code Optimization Application Note (order# 21924)
- AMD-K6® Processor Multimedia Technology (order# 20726)
- AMD-K6® Processor BIOS and Software Tools Developers Guide (order# 21062)
- AMD-K6® Processor BIOS Design Application Note (order# 21329)
- AMD Processor Recognition Application Note (order# 20734)
- Implementation of Write Allocate in the K86™ Processors (order# 21326)
- AMD-K6® Processor Thermal Solution Design Application Note (order# 21085)
- AMD-K6® Processor Power Supply Design Application Note (order# 21103)
- AMD-K6® Processor I/O Model Application Note (order# 21084)
- AMD-K6® Processor V_{CC2} Voltage Detection Application Note (order# 21635)
- SYSCALL and SYSRET Instruction Specification Application Note (order# 21086)
- AMD-K6® Processor x86 Code Optimization Application Note (order# 21828)
- AMD-K6® Processor 100-MHz Bus Specification (order# 21644)
- AMD-K6® Processor EMI Design Considerations (order# 22023)

For the latest updates, refer to www.amd.com/K6/k6docs and download the appropriate files.