NOVIX

Microprocessors

T-49-17-16

10 MIPs 16-BIT STACK BASED MPU NC4016

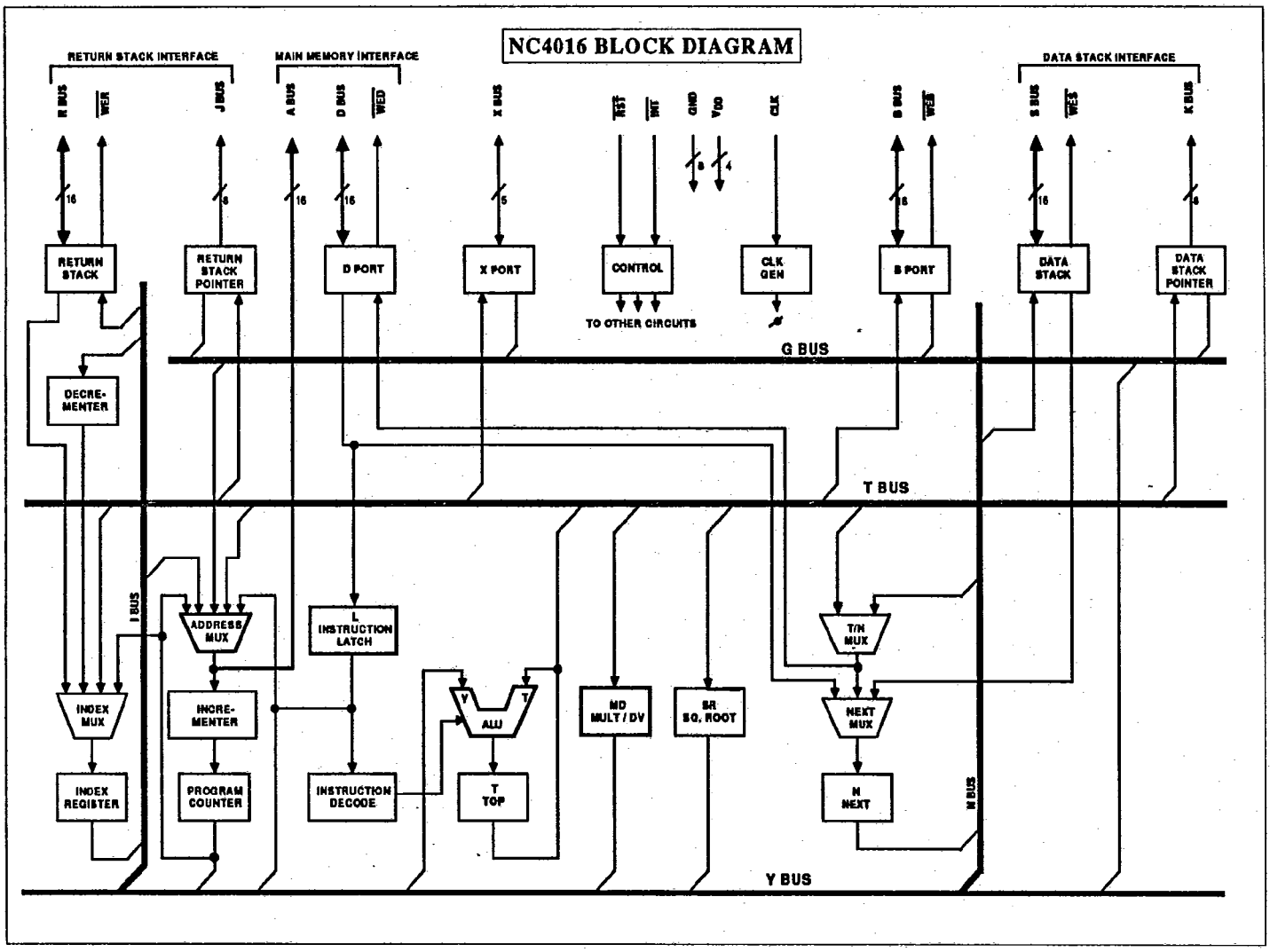
PRODUCT DESCRIPTION

The NC4016 is a stack based, internally parallel, high performance microprocessor which directly executes the primitives of the high-level FORTH language. This HCMOS MPU achieves its remarkable performance by eliminating the assembly and microcode translation that typically characterizes communication between a high-level language application and conventional MPU hardware.

Designed for simplicity and speed, the NC4016 operates simultaneously on four separate memory spaces, and can achieve 10 MIPS performance with a 7.5 MHz system clock.

The driving force of the FORTH language is the elimination of subroutine call overhead. The NC4016 represents the next logical step: a processor optimized to require one clock cycle per subroutine call. This capability makes it highly suited for real time, multi-tasking, and high speed control applications.

Third party benchmarks demonstrate that the NC4016 runs high-level FORTH code more than 20 times faster than a Motorola 68000 runs machine code. Its stack architecture also provides an ideal environment for



recursive compilers, such as the NOVIX NS4100 Small C compiler.

The HCMOS implementation of the NC4016 makes it possible to tailor the design to meet a variety of system speed and power combination requirements.

Novix offers the ND4000 Stand Alone Development System, an IBM PC-compatible software and hardware development system, and other board level products, making the NC4016 easy to work with and use.

FEATURES

- 16-bit microprocessor
- HCMOS technology for low power dissipation
- 10 MIPS performance with a 7.5 MHz system clock
- Execution of multiple FORTH words in a single-cycle, yielding over 130 available instruction combinations
- Simultaneous access of Return Stack, Data Stack, Main Memory, and I/O Bus, concurrent with operation of ALU and shifters
- One-cycle subroutine call, typically with zero-cycle return
- Supports 64K word main memory, or 2M words using extended memory addressing
- Structured IF, ELSE, and NEXT (loop operation) one-cycle instructions

	A	B	C	D	E	F	G	H	J	K	L	M	N	
13	R14	B12	R12	B10	B09	R08	B07	R07	B05	B04	R03	B01	B00	13
12	R15	B14	B13	B11	R10	B08	VDD	B06	R05	B03	B02	R01	A00	12
11	A08	WED	VSS	R13	R11	R09	VSS	R06	R04	R02	VSS	R00	A01	11
10	A11	A09	B15								WEB	A02	A04	10
9	A13	A12	A10								A03	A05	A06	9
8	RST	A15	A14				NC4016				A07	X00	X01	8
7	INT	VDD	VSS								VSS	VDD	X02	7
6	CLK	K00	K01				Top View				J00	X04	X03	6
5	K02	K03	K05				Cavity Up / Pins Down				J04	J02	J01	5
4	K04	K06	D15				INDEX				WER	J05	J03	4
3	K07	S15	VSS	S13	S11	S09	VSS	S06	S04	S02	VSS	J07	J06	3
2	WES	S14	D12	D11	S10	D08	VDD	D06	S05	D03	D01	D00	S00	2
1	D14	D13	S12	D10	D09	S08	D07	S07	D05	D04	S03	D02	S01	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	

PIN GRID ARRAY PIN-OUT DIAGRAM

- TIMES instruction allows any operation to be repeated once per cycle, including auto-increment/decrement memory access
- 258-element 16-bit hardware *data stack* with two top elements in on-chip registers
- 257-element 16-bit hardware *return stack* with one top element in on-chip register
- Two versatile I/O ports, both of which are bi-directional, maskable, auto-comparable, and programmable for either latched or tri-state output

ARCHITECTURE

Typical microprocessors decode machine instructions, subsequently invoking a sequence of internal micro-code instructions which control the MPU's actual "silicon" components. In the NC4016, bit patterns within each high level instruction directly control the processor's "silicon" components. Elimination of internal microcode contributes significantly to the speed improvement of the NC4016 over traditional microprocessors.

The NC4016's separate internal buses and stacks are uniquely configured to accommodate the efficient flow of FORTH program instructions. Parallel organization enables the execution of multiple FORTH words in a single

instruction, within a single clock cycle. It also allows simultaneous access of multiple memory spaces, and concurrent ALU activity. The distinctive architecture of the logic is based on the characteristics of the high level instructions and their execution, minimizing any obstructions to the flow of both instructions and data.

NC4016 COMPONENTS

ALU: The arithmetic/logic components perform proprietary multiplication, division and square root algorithms in hardware. The ALU operates on two 16-bit data sources. One of the sources is T, the top item of the data stack. The other source may be switched, depending on the operation, to any of the following registers:

N	Next data stack
MD	Multiply/divide
SR	Square root

The results are always in the T register. The ALU can perform +, -, OR, AND, & XOR operations in addition to swapping data elements on the stack.

Data Stack: A 16-bit data stack provides the means for passing data to and from subroutines. For speed, the top two elements of the data stack reside in on-chip registers; these two registers are T (Top) and N (Next). An additional 256 stack elements below the top two reside in off-chip memory and apart from main memory.

The MPU communicates with the off-chip data stack memory via a separate 16-bit data stack bus. The data stack pointer is an on-chip 8-bit register.

Return Stack: The return stack, integral to the FORTH architecture, holds 16-bit subroutine "return addresses".

The top element of the 257 word return stack is an on-chip register. The remaining 256 elements are located in dedicated off-chip memory.

There is no performance overhead for subroutine return stack operations, because the return stack is accessed in parallel with other I/O.

The NC4016 addresses 256 words of off-chip data stack memory

No performance overhead for subroutine return stack operations

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During a call instruction, the current address is saved on the return stack at the same time the next address is placed on the main address bus. A return operation can occur simultaneously with operations of the ALU. In most cases, no clock cycle is spent on the return operation.

Program Counter: The program counter points to the location of the next instruction to be fetched from external program memory. It is automatically altered by the jump, loop, and subroutine call instructions. The program counter is 16-bits wide and uses word-addressing, not byte-addressing.

Internal Memory: The NC4016 features 14 on-chip registers, each 16-bits wide. They are:

J/K	Data and return stack pointers
Index	I as #loop index
PC	Program counter
True	Logical true source
MD	Multiplier/divisor register
SR	Square root register
B port	I/O port B - data
Bx	I/O port B - mask
By	I/O port B - direction
Bz	I/O port B - tri-state
X port	I/O port X - data
Xx	I/O port X - mask
Xy	I/O port X - direction
Xz	I/O port X - tri-state

INSTRUCTION SET

The NC4016 instruction set includes:

- Stack Manipulation operators
- Return Stack operators
- 16-bit addition and subtraction (with or without carry)
- Multiplication
- Division
- Square Root
- Bit-wise ORs, ANDs, XORs
- Logical shifts
- Jump
- Repeat
- Data fetch and store
- Literal data fetch
- Extended-address
- Local and internal data fetch and store
- I/O functions performed by accessing internal registers

With the NC4016 instruction set and architecture, clock cycles are never wasted, even when the program counter is changed. Pipelining is unnecessary.

The CALL instruction is indicated by a zero in the instruction's high-order bit. The remaining 15 bits specify the address of the FORTH word (subroutine) to jump to. A one in the high-order bit indicates a normal machine instruction. With this technique, the NC4016 accomplishes subroutine calls in a single clock cycle, an achievement unparalleled by any known processor.

The TIMES instruction is also unique. It eliminates a repetition count prior to the execution of the instruction to be repeated without re-fetching the instruction each iteration. This feature simplifies and speeds the handling of streams of data and facilitates moving blocks of memory at full clock speed.

PRELIMINARY ELECTRICAL SPECIFICATIONS:

Supply Voltage, V_{DD}	+5.0V ± 10%
Supply Current, I_{DD}	7 Ma/MHz
Free-Air Ambient Temperature, T_A	0 to +70 °C
V_{IL} / V_{IH} Input Logic Levels	Within 30% of GND/V_{DD}
V_{OL}/V_{OH} Output Logic Levels	Within 0.1V of GND / V_{DD} at ±20 Ma
Applied Clock Frequency, F_{CLK}	0 to 10 MHz

Address Outputs Setup Delay Time
(T_A = 25 °C, V_{DD} = +5.0V)

Main Memory	75 nSec
Return Stack	95 nSec
Data Stack	100 nSec

Data Outputs Setup Delay Time
(T_A = 25 °C, V_{DD} = +5.0V)

Main Memory	95 nSec
Return Stack	45 nSec
Data Stack	75 nSec

B / X Port Outputs Setup Delay Time

B Ports	45 nSec
X Ports	45 nSec

Specifications subject to change without notice

NC4016 INSTRUCTIONS CORRESPONDING TO SINGLE FORTH WORDS

STACK MANIPULATION

COPY	Copy top of stack
DROP	Pop the top stack and discard
SWAP	Switch order of top two stack elements
OVER	Push copy of second (next) stack element onto top of stack

ARITHMETIC / LOGIC

+	Add top two stack elements as 16-bit two's complement integers
+ c	Add with carry
–	Subtract top stack element from second element, as 16-bit two's complement integers
– c	Subtract with carry
OR	Bit-by-bit logical "or" of top two stack elements
AND	Bit-by-bit logical "and" of top two stack elements
XOR	Bit-by-bit logical "xor" of top two stack elements
2/	Arithmetic shift of T right one bit
2*	Arithmetic shift of T left one bit
0<	Return "true" flag (hex FFFF) if top of stack is negative: otherwise "false" (zero)
D2/	32-bit number arithmetic-shift right
D2*	32-bit number arithmetic-shift left

RETURN STACK CONTROL

R>	Pop top of return stack onto data stack
R@	Copy top of return stack to the data stack
FOR	Copy loop limit onto return stack
>R	Pop the top of data stack to the return stack
NEXT	Decrement loop index on return stack and conditionally loop until equal to zero

STRUCTURE CONTROL

If	Jump if T is zero
Else	Unconditional Jump
Loop	Jump and decrement loop counter if it is not zero
Times	Sets repeat-instruction counter
Call	Jump to subroutine
EXIT	Return

MEMORY ACCESS

@	Fetch value at memory address pointed to by top of stack
!	Store value of the second stack element in the address pointed to by top of stack
nn	Push 5-bit literal to top of stack
nn@	Fetch value at local memory address (5-bit literal fetch)
nn!	Store value at top of stack into local memory address (5-bit literal store)
I@	Fetch value from internal register
I!	Store value into internal register

INSTRUCTIONS CORRESPONDING TO MULTIPLE FORTH WORDS

Multiple FORTH word instructions can be created for the following by combining single FORTH words:

Stack Manipulation	Local Data Fetch	Local Data Store
Shift Operations	Internal Data Fetch	Internal Data Store
ALU Operations	Data Fetch (WORD)	Data Store (WORD)
Return Stack	Short Literal Fetch	
	Full Literal Fetch	

contact NOVIX for details on these instructions

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