

Qualification of the AMD Alchemy TM Au1500 TM Processor

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Contacts

www.amd.com pcs.support@amd.com

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Revision History

| Date | Revision | Description |
|---------------|----------|--|
| May 2002 | 1 | Original document created by Sarah Bartaszewicz |
| July 2002 | 2 | Updated to reflect qualification status (Sarah Bartaszewicz) |
| December 2002 | A | Updated to reflect qualification status (Jean Paul Somers), PID assigned |
| March 2003 | В | Updated FIT information |

1. Au1500™ Product Qualification

The Au1500TM processor is a qualified product as defined by this document.

2. Levels of Qualification

A preliminary qualification level will be awarded upon completion of the Early Fail Study (EFS). EFS is completed at three lots with an equivalent Field Effective Hours of 4000.

The final qualification level is awarded upon completion of the High Temperature Operation Life (HTOL) and all other qualification stresses as outlined in this document.

3. Institutional/Agency Qualifications

EIA – Electronic Industries Association

JEDEC - Joint Electron Device Engineering Council

4. Warranty Disclaimer

Data resulting from the qualification methodology described in this document is predictive only and does not create an express or implied warranty of product performance, merchantability, or fitness for a particular purpose. Applicable warranties for AMD devices are set forth in AMD's terms and conditions of sale. AMD provides qualification data "as is" and only as predictive guidelines to assist customers with their examination of an AMD device.

5. Package Qualification

A qualified packaging technology is utilized in the Au1500TM processor as provided by Advanced Semiconductor Engineering, Inc. (ASE). The package is a 424 ball, 0.8mm ball pitch, LFBGA. The package qualification meets all SME applications for assembly and packaging processes as listed in Table 1.

Sample Test Stress/ Accept **Test Condition Qualification Point** Criteria (Package Size) Size 5 Physical 0 Fails JEDEC 95-1 as applicable Qualified by AMD Dimensions to BGAs with exemption 1st tooled substrate inspection superseded as outlined in the Package Outline Drawing Temperature 45/lot 0 Fails JEDEC 22-A104-B Qualified per ASE Report -65°C ~ 150°C, 1000 Cycles No.: RT-020717-CR02 Cycling HAST 0 Fails JEDEC 22-A118 Qualified per ASE Report 45/lot (No Bias) 130°C/85% RH. No.: RT-020717-CR02 33.5 PSIG, 100 Hours Pressure Cooker 45/lot 0 Fails JEDEC 22-A102-C Qualified per ASE Report 121°C/100% RH, No.: RT-020717-CR02 15 PSIG, 168 Hours 45/lot 0 Fails JEDEC 22-A101-B Temperature Qualified per ASE Report **Humidity Test** No.: RT-020717-CR02 85°C /85%RH, 1000 Hours (No Bias) 225 Moisture 0 Fails JEDEC J-STD-020A Qualified per ASE Report Sensitivity MSL 3, 220C & 235C No.: 580-010316-00 NA NA Laser Marking NA Marking Permanence

Table 1. Package Qualification

5A. Package Profile

Package type: LFBGA 424L

Epoxy: Ablestik/8355F

Mold Compound: Shinetsu/KMC 211AA-2

Solder Ball: 63Sn/37Pb

6. Process Qualification

A qualified process manufactured by Taiwan Semiconductor Manufacturing Company (TSMC) is utilized in the Au1500TM processor. The qualified silicon process in use is the Low Voltage version of the 0.18 μm Low Voltage logic 1.5V/3.3V 1P6M process and is documented in TSMC document number: T-018-LO-QR-002. The procedure utilized by TSMC for process qualification is outlined in the Generic Process Qualification Procedure as defined in TSMC document number: AG-3100-5020. The results of the Generic Process Qualification of the 0.18μm 1.5V/3.3V 1P6M process is documented in TSMC document number: T-018-LO-QR-001. The qualification of TSMC 0.18μm logic Low Voltage logic 1.5V/3.3V 1P6M process was achieved on passing results from the following tests:

- 1. Gate Oxide Integrity
- 2. Hot Carrier
- 3. Vt Stability (Vt Fluence)
- 4. Metal Step Coverage
- 5. Metal Integrity (Stress Migration/Voiding)
- 6. Via and Metal Line Electromigration

6A. Device Level Process Qualification

A 2M 6T SRAM test vehicle was utilized by TSMC to supplement the process qualification with a device High Temperature Operations Life test (HTOL) qualification. Passing results based on a sample size consisting of 100 units each from 3 production lots.

1. HTOL per MIL STD 883E, method 1015.8

7. Component Qualification

Component qualification awarded per the completion of requirements outlined in Table 2 with sample sizes equally divided from three process lots.

Table 2. Product Qualification at Component Level

| Test/Stress | Sample Size/Lot | Accept/ Reject | Results | Test Condition | Qualification Point |
|---|--------------------|--------------------------|---------------------|---|--|
| ESD Human Body Model | 3/stress | 0 Fails | Pass | MIL-STD-883, Method 3015 JEDEC JESD22-A114-A | Human Model stress at 500V, 1000V and 2000V |
| ESD Machine Model | 3/stress | 0 Fails | Pass | MIL-STD-883, Method 3015 JEDEC JESD22-A115-A | Machine Model stress at 100V, 200V and 400V. |
| Latch Up | 3 | 0 Fails | Accepta | JESD78 | I-Test, Over-V Test |
| High Temperature Operational Life (HTOL) | 240 | Reject if >150 FIT | Accept ^b | MIL-STD-883E, Method 1015 Tj = 125°C | 30000 Field Effective Hours (FEH) |
| Early Fail Study (EFS) | 720 | Reject if >350 FIT | Pass | MIL-STD-883E, Method 1015 Tj = 125°C | 4000 Field Effective Hours (EFS) |
| System Soft Error ^c (SSER) | NA | NA | NA | MIL-STD-10-232 | Not Required |

| table 2.1 roddet Qualification at Component Ecver | | | | | |
|---|--------------------|-------------------|---------|----------------|---------------------------|
| Test/Stress | Sample Size/Lot | Accept/ Reject | Results | Test Condition | Qualification Point |
| Accelerated Soft Error (ASER) | NA | NA | NA | MIL-STD-10-232 | Not Required |
| Power Cycling ^d | NA | 0 Fails | Pass | AMD Internal | Repeated Power Up Cycling |

Table 2. Product Qualification at Component Level

a.Latch up results are summarized in section 7B.

7A. FIT Calculations

The failure rate (FIT) calculation for three qualification lots was 85 at the Chi Square 60% Confidence Level for EFS, which corresponds to Defects per Million (DPM) of 339. Failure rate calculations performed on the four lots for HTOL resulted in a FIT rate of 18.5 at the Chi Square of 60% Confidence level, which corresponds to Mean Time to Failure (MTTF) of 54 x 10⁶.

7B. Latch Up Stress Results Summary

Results of latch up testing performed to JEDEC standard 78 as performed by a contracted external laboratory are presented in Table 3.

Table 3. Latch Up Stress Testing Results

| Type of Test | Stress Level | Test Results |
|-------------------|------------------|---|
| Over Voltage Low | 150% VDD Nominal | Pass |
| Over Voltage High | 150% VDD Nominal | Pass |
| Negative Current | -100mA Trigger | Pass |
| Positive Current | 100mA Trigger | Acceptable. Failures observed but not verified. |

Preliminary positive current testing, both input low and high, performed by the external laboratory resulted in increased currents above the acceptable level on eight input pins for all sample units tested. It should be noted that the equipment utilized by the external laboratory is unable to program the latch up test system power supplies to meet the Au1500TM processor power-up timing requirements as specified in the data sheet. AMD laboratory latch up analysis resulted in passing current levels when the correct power up timing requirements are used.

b.HTOL results are summarized in section 7A.

c.SSER, ASER: These tests are not necessary for qualification (cache limited).

d. Power Cycling: This test is not necessary for qualification, but power cycling schemes will be performed to emulate specific customer applications as needed.

References

AG-3100-5020, Taiwan Semiconductor Manufacturing Co., Generic Process Qualification Procedure

JEDEC Standard 22-A102, Highly Accelerated Moisture Resistance, Unbiased Autoclave

JEDEC Standard 22-A103, High Temperature Storage Life

JEDEC Standard 22-A110, Highly Accelerated Temperature and Humidity Stress Test (HAST)

Military Standard 883, Microcircuits

DH080600-01, Advanced Semiconductor Engineering, Inc., Reliability Test Report, Package Qualification

T-018-LO-QR-001, Taiwan Semiconductor Manufacturing Co., LTD 0.18µm Logic 1p6M 1.5V/3.3V Reliability Qualification Report

T-018-LO-QR-002, Taiwan Semiconductor Manufacturing Co., LTD 0.18µm Logic 1p6M 1.5V/3.3V Reliability Qualification Report (Low Voltage)