MPEG2 Multi-channel Decoder for FPOA

June 2006 **Preliminary Product Brief**

Features

- Decodes a combined bitstream at rate of 120 Mbps
- Maximum frequency of 800 MHz
- Complies with ISO/IEC Specification 13818-2
- Decodes four channels of MPEG2 MP@ML stream in real-time
- Configurable to decode one stream of MP@HL (High Definition) or one stream of HP@ML
- Interfaces with host through a PowerPC Local Bus

Applications

- Professional video
- Security surveillance with compressed video
- Video hardware acceleration

FPOA Background

The MathStar Field-Programmable Object Array (FPOA) architecture comprises an array of silicon objects, each performing a specific function at data rates up to 1 GHz. The architecture supports three kinds of 16-bit core objects: an Arithmetic Logic Unit (ALU), a Multiply-Accumulator (MAC) and a Register File (RF). The objects are interconnected by a two-tier interconnect structure. The interconnect structure allows for 1 GHz connectivity between Nearest Neighbor connections as well as 1 GHz connectivity between non-adjacent objects through patented Party Line interconnects. These objects are coupled with distributed internal RAM (IRAM), dedicated external memory controllers (XRAM) and a wide range of high-speed and general-purpose I/O (GPIO) to form the complete FPOA architecture. Because of its high performance, an FPOA can run many applications up to 2-4 times faster than top FPGA architectures.

General Description

The MPEG2 Multi-channel Decoder for FPOA core complies with ISO/IEC Specification 13818-2. This core is capable of decoding four channels of MPEG2 MP@ML stream in real-time. It can also be configured to decode one stream of MP@HL (High Definition) or one of HP@ML.

This decoder interfaces with a host through a PowerPC Local Bus and performs the following operations:

- It processes compressed bitstreams to re-build live video sequences
- The external host provides the bitstream with channel information embedded in the data header
- Depending on the profile and level the decoder can handle various bitstream rates and picture sizes
- The decoder uses a large external memory to store reconstructed pictures and input bitstreams
- The decoder generates video sequences in 4:2:0 color component format

Functional Overview

The functional block diagram of this decoder is depicted in Figure 1.

Host Interface (HIF) – connects FPOA via one 44-pin GPIO port with external host through a Local Bus. The raw data rate of 2.5 Gbps

VBV Buffer Controller (VBC) – manages the 8-channel VBV buffer and switches channels at the frame boundary

Variable Length Decoder (VLD) – decodes variable length code for all six VLD tables

Header Parser & Control (HPC) – main control state machine for parsing bitstreams

Motion Vector (MVR) – rebuilds the motion vector and calculates the address of reference block

Run-Length Expander (RLE) – expands the run length pair according to the scanning sequence and rebuilds the 8x8 block

IQ – performs inverse quantization

IDCT – performs inverse DCT on each 8x8 block

Motion Compensation (MCP) – rebuilds each motion compensated block

XRAM Controller – accesses external memory for reference frame, reconstructed frame and display frame. XRAM consists of 64 Mbyte DDR RLDRAM running at 266 MHz.

Video Out (VOT) – send the video data out through Host Interface

Inner Memory Loop (IML) – arbitrates concurrent accesses between Motion Compensation, Video Out, and VBV Buffer Controller.

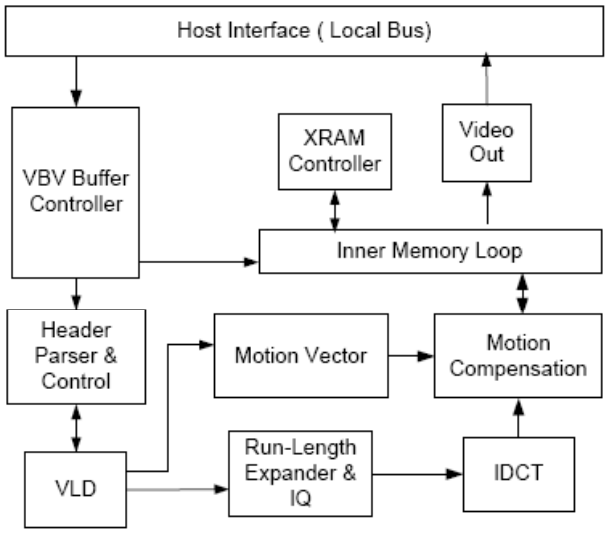

Figure 1 – MPEG2 Multi-channel Decoder block diagram

Estimated Performance

The table below summarizes the estimated performance of the MPEG2 Multi-channel Decoder. FPOA

Variable/parameter	Value
Throughput	120 Mbps
Frequency (max)	800 MHz
Target device	Consult MathStar technical documentation
Resource utilization	Approx. 80%

Note: The information provided above is preliminary and should be considered as an estimate.

Support

The MPEG2 Multi-channel Decoder for FPOA is warranted against defects for one year from purchase. Twelve months days of phone and email technical support are included. (contact MathStar, Inc. for licensing terms).

Deliverables

The MPEG2 Multi-channel Decoder for FPOA includes the following components.

- Cycle-accurate, bit-true simulation model for Visual Elite simulator
- Testbench
- OHDL files
- Mapping files for MathStar's COAST tool
- Design guide

Ordering Information

The MathStar MPEG2 Multi-channel Decoder for FPOA will be available as part number MIP-M2D02-P12. For further information, contact MathStar, Inc. at info@mathstar.com