# μCOM-43 SINGLE CHIP MICROCOMPUTER

## DESCRIPTION

The μPD650 is a CMOS version of the μCOM-43. It features a single +5 volt power supply, a 2 mA (max), 800 μA (typ) current drain and extended temperature range. As a μCOM-43, it includes 2000 x 8 ROM, 96 x 4 RAM and 35 I/O lines in a 42 pin plastic dual-in-line package.

## ABSOLUTE MAXIMUM RATINGS*

| | |
|---|---|
| Operating Temperature | −30°C to +85°C |
| Storage Temperature | −55°C to +125°C |
| Supply Voltage | −0.3 to +7.0 Volts |
| Input Voltages | −0.3 to +7.0 Volts |
| Output Voltages | −0.3 to +7.0 Volts |
| Output Current (Each Output Bit) | 2.5 mA |

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*$T_a$ = 25°C

## DC/AC CHARACTERISTICS

$T_a$ = −30°C to +85°C, $V_{CC}$ = +5V ± 10%.

| PARAMETER | SYMBOL | LIMITS MIN | LIMITS TYP | LIMITS MAX | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|
| Input High Voltage | $V_{IH}$ | $0.7V_{CC}$ | | $V_{CC}$ | V | Ports A to D, $\overline{INT}$, RES |
| Input Low Voltage | $V_{IL}$ | 0 | | $0.3V_{CC}$ | V | Ports A to D, $\overline{INT}$, RES |
| Input Leakage Current High | $I_{LIH}$ | | | +10 | μA | Ports A and B, $\overline{INT}$, RES ($V_I = V_{CC}$) |
| Input Leakage Current Low | $I_{LIL}$ | | | −10 | μA | Ports A and B, $\overline{INT}$, RES ($V_I$ = 0V) |
| I/O Leakage Current High | $I_{IOH}$ | | | +10 | μA | Ports C and D ($V_I = V_{CC}$) |
| I/O Leakage Current Low | $I_{IOL}$ | | | −10 | μA | Ports C and D ($V_O$ = 0V) |
| Output High Voltage 1 | $V_{OH1}$ | $V_{CC}$−0.5 | | | V | Ports C and D ($I_{OH}$ = −1 mA) |
| | | $V_{CC}$−0.5 | | | V | Ports E and I ($I_{OH}$ = −0.6 mA) |
| Output High Voltage 2 | $V_{OH2}$ | $V_{CC}$−2.5 | | | V | Ports C to I ($I_{OH}$ = −2 mA) |
| Output Low Voltage | $V_{OL1}$ | | | 0.6 | V | Ports E to I ($I_{OL}$ = 2 mA) |
| | $V_{OL2}$ | | | 0.4 | V | Ports E to I ($I_{OL}$ = 7.2 mA) |
| Supply Current | $I_{CC}$ | | 0.8 | 2.0 | mA | |
| Clock High Voltage | $V_{\phi H}$ | $0.7V_{CC}$ | | $V_{CC}$ | V | CLO, Ext. Clk. |
| Clock Low Voltage | $V_{\phi L}$ | 0 | | $0.3V_{CC}$ | V | CLO, Ext. Clk. |
| Clock Leakage Current High | $I_{L\phi H}$ | | | 200 | μA | CLO, Ext. Clk. ($V_{OH} = V_{CC}$) |
| Clock Leakage Current Low | $I_{L\phi L}$ | | | −200 | μA | CLO, Ext. Clk. ($V_{OL}$ = 0V) |
| Clock Frequency | f | 150 | | 440 | KHz | |
| Clock Rise and Fall Times | tr, tf | 0 | | 0.3 | μs | Ext. Clk. |
| Clock Pulse Width | $t_{\phi W}$ | 0.5 | | 5.6 | μs | Ext. Clk. |

6

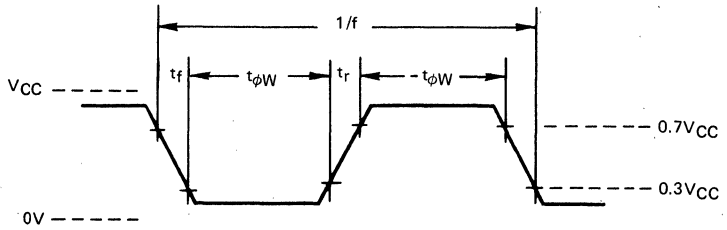
# μPD650

$T_a$ = −30°C to +85°C, $V_{CC}$ = +5V ± 10%.

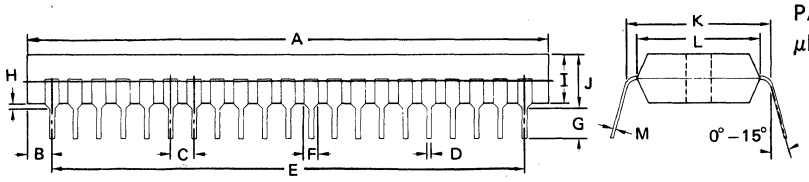
## CAPACITANCE

| PARAMETER | SYMBOL | LIMITS MIN | LIMITS TYP | LIMITS MAX | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|
| Input Capacitance | $C_I$ | | | 15 | pf | f = 1 MHz |
| Output Capacitance | $C_O$ | | | 15 | pf | |
| I/O Capacitance | $C_{IO}$ | | | 15 | pf | |

## CLOCK WAVEFORM




## PACKAGE OUTLINE μPD650C




| ITEM | MILLIMETERS | INCHES |
|---|---|---|
| A | 56.0 MAX | 2.2 MAX |
| B | 2.6 MAX | 0.1 MAX |
| C | 2.54 | 0.1 |
| D | 0.5 ± 0.1 | 0.02 ± 0.004 |
| E | 50.8 | 2.0 |
| F | 1.5 | 0.059 |
| G | 3.2 MIN | 0.126 MIN |
| H | 0.5 MIN | 0.02 MIN |
| I | 5.22 MAX | 0.20 MAX |
| J | 5.72 MAX | 0.22 MAX |
| K | 15.24 | 0.6 |
| L | 13.2 | 0.52 |
| M | 0.3 ± 0.1 | 0.01 ± 0.004 |