# 80186

High-Integration 16-Bit Microprocessor
iAPX86 Family
MILITARY INFORMATION



## DISTINCTIVE CHARACTERISTICS

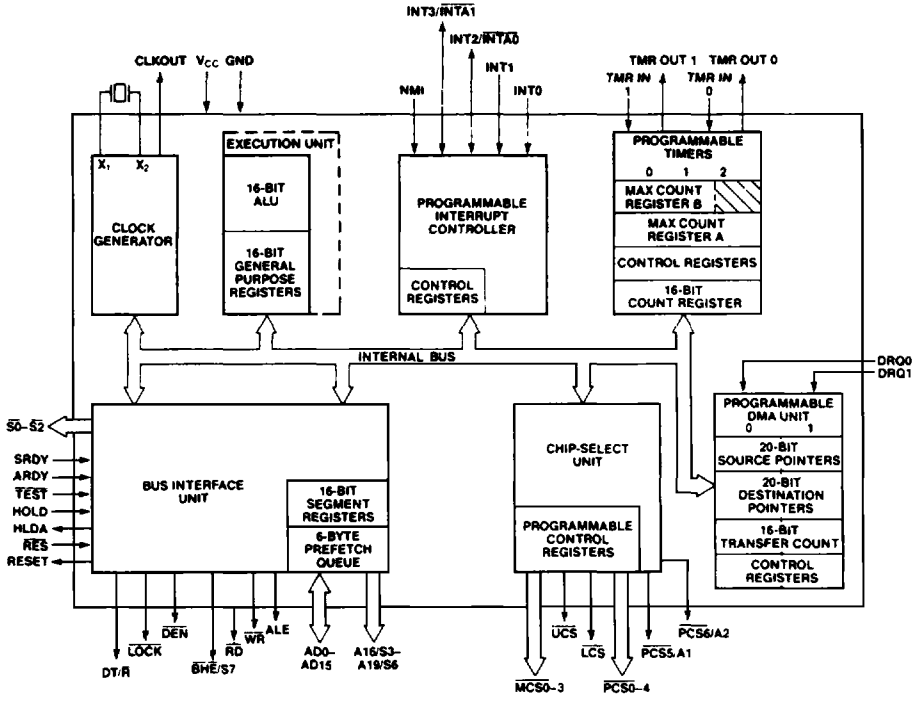
- Integrated feature set
  - Enhanced 8-MHz 8086-2 CPU
  - *Clock generator*
  - Two independent, high-speed DMA channels
  - Programmable interrupt controller
  - Three programmable 16-bit timers
  - *Programmable memory and peripheral chip-select logic*
  - Programmable wait-state generator
  - Local bus controller
- Available in 8 MHz (80186) and 6 MHz (80186-6)
- High-performance processor
  - Two times the performance of the standard 8086
  - *4 Mbyte/sec bus bandwidth interface*
- Direct addressing capability to 1 Mbyte of memory
- Completely object-code-compatible with all existing iAPX 86, 88 software
  - *Ten new instruction types*
  - Compatible with 29843/45 and 8284 bus support components
- Optional numeric processor extension
- Available in 68-pin Ceramic Leadless Chip Carrier (LCC) and Pin Grid Array (PGA) packages

## GENERAL DESCRIPTION

The 80186 is a highly integrated 16-bit microprocessor. It effectively combines 15-20 of the most common iAPX 86 system components onto one. The 80186 provides two times greater throughput than the standard 5-MHz 8086. The 80186 is upward-compatible with 8086 and 8088 software, and adds ten new instruction types to the existing set.

The 80186 comes in a 68-pin package and requires a single ±5V power supply.

## BLOCK DIAGRAM




BD003560





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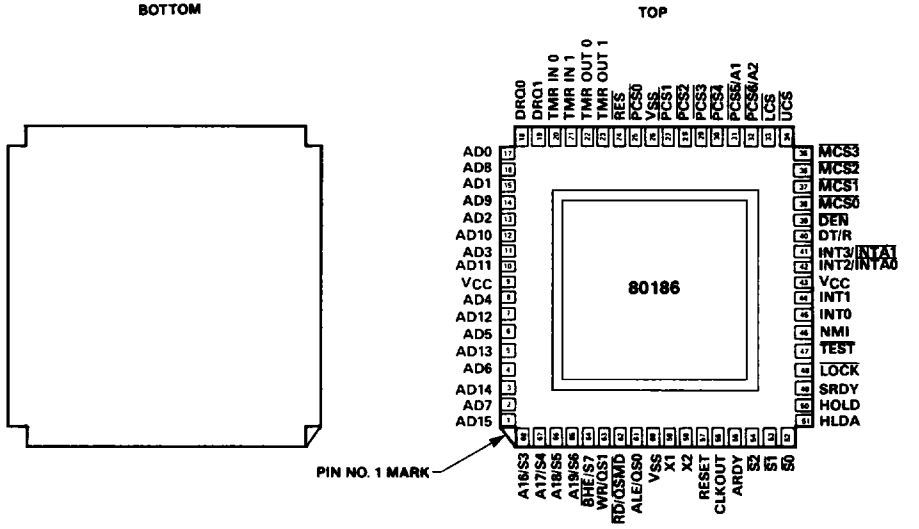
## CONNECTION DIAGRAMS

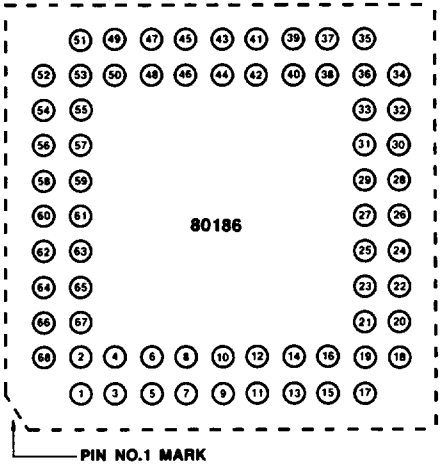
### 68-Pin Ceramic LCC Package




CD005393

### 68-Pin Grid Array
### Cavity Down Package

**Top**
**(Pins pointing away from viewer)**
**0**

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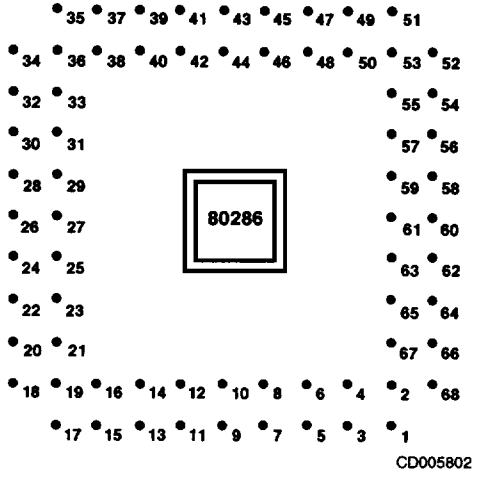
Pins are not visible from the top of this package.

**Bottom**
**(Pins pointing toward viewer)**
**3835**



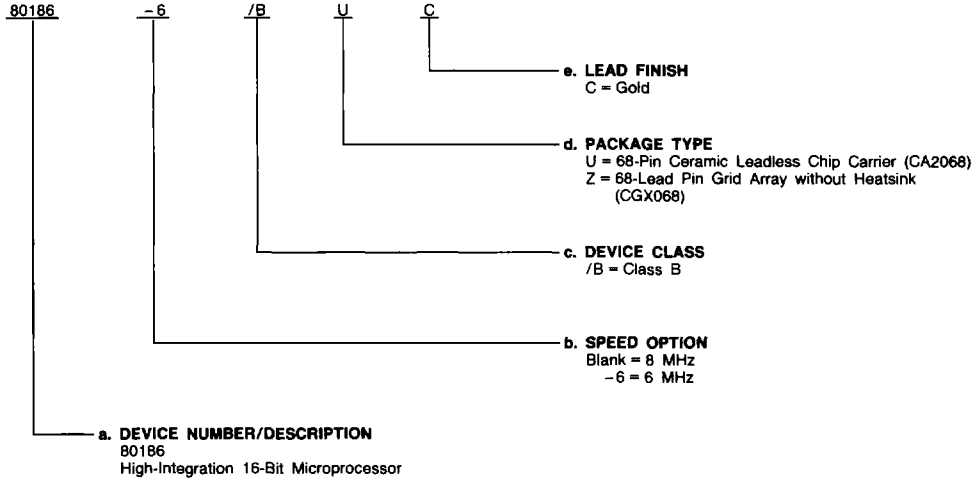

CD005802

Pins are visible from the bottom of this package.

# MILITARY ORDERING INFORMATION

## APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
**b. Speed Option** (if applicable)
**c. Device Class**
**d. Package Type**
**e. Lead Finish**




| Valid Combinations | |
|---|---|
| 80186 | /BUC, /BZC |
| 80186-6 | |

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

### Group A Tests

Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Voltage on Any Pin with
Respect to Ground ..... −1.0 V to +7 V
Power Dissipation ..... 3 W

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Military (M) Devices
Temperature ($T_C$) ..... −55 to +125°C
Supply Voltage ($V_{CC}$) ..... 5 V ±5%

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

**DC CHARACTERISTICS** over operating range (for APL products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

| Parameter Symbol | Parameter Description | Test Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{IL}$ † | Input LOW Voltage | | −0.5 | +0.8 | V |
| $V_{IH}$ † | Input HIGH Voltage (All Except $X_1$ and $\overline{RES}$) | | 2.0 | $V_{CC}$ + 0.5 | V |
| $V_{IH1}$ † | Input HIGH Voltage ($\overline{RES}$) | | 3.0 | $V_{CC}$ + 0.5 | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 2.5 mA for $\overline{S_0}$ – $\overline{S_2}$<br>$I_{OL}$ = 2.0 mA for All Other Outputs | | 0.45 | V |
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = −[illegible] | 2.4 | | V |
| $I_{CC}$ | Power Supply Current | [illegible] = $V_{CC}$ Max. | | 600 | mA |
| $I_{LI}$ | Input Leakage Current | [illegible] < $V_{CC}$ Max. | | ±10 | μA |
| $I_{LO}$ | Output Leakage Current | 0.45 V < $V_{OUT}$ < $V_{CC}$ Max. | | ±10 | μA |
| $V_{CLO}$ | Clock Output LOW | $I_{OL}$ = 4.0 mA | | 0.6 | V |
| $V_{CHO}$ | Clock Output HIGH | $I_{OH}$ = −200 μA | 4.0 | | V |
| $V_{CLI}$ † | Clock Input LOW Voltage | | −0.5 | 0.6 | V |
| $V_{CHI}$ † | Clock Input HIGH Voltage | | 3.9 | $V_{CC}$ + 1.0 | V |
| $C_{IN}$ †† | Input Capacitance | | | 10* | pF |
| $C_{IO}$ †† | I/O Capacitance | | | 20* | pF |



* Not tested; guaranteed by design.
† Group A, Subgroups 7 and 8 only are tested.
†† Not included in Group A tests.

See Section 6 of the MOS Microprocessors and Peripherals Data Book (Order #09067A) for Thermal Characteristics Information.

**SWITCHING CHARACTERISTICS** over operating range (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

**PIN TIMING**

**80186 Timing Requirements** (all timings measured at 1.5 V unless otherwise noted)

| Parameter Symbol | Parameter Description | Test Conditions | 80186 (8 MHz) & 80186-6 (6 MHz) | | Unit |
|---|---|---|---|---|---|
| | | | Min. | Max. | |
| TDVCL | Data in Setup (A/D) | | 20 | | ns |
| TCLDX | Data in Hold (A/D) | | 10 | | ns |
| TARYHCH | Asynchronous Ready (AREADY) Active Setup Time* | | 20 | | ns |
| TARYLCL | AREADY Inactive Setup Time | | 38 | | ns |
| TCHARYX | AREADY Hold Time | | 15 | | ns |
| TSRYCL | Synchronous Ready (SREADY) Transition Setup Time | | 35 | | ns |
| TCLSRY | SREADY Transition Hold Time | | 15 | | ns |
| THVCL | HOLD Setup* | | 25 | | ns |
| TINVCH | INTR, NMI, $\overline{TEST}$, TIMERIN, Setup* | | 25 | | ns |
| TINVCL | $DRQ_0$, $DRQ_1$, Setup* | | 25 | | ns |

*To guarantee recognition at next clock.

Note: Case temperatures are instant-on.

**80186 Master Interface Timing Responses**

| Parameter Symbol | Description | Test Conditions | 80186 (8 MHz) | | 80186-6 (6 MHz) | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | |
| TCLAV | Address Valid Delay | $C_L$ = 100 pF all outputs | 5 | 59 | 5 | 63 | ns |
| TCLAX | Address Hold | | 5 | | 5 | | ns |
| TCLAZ | A ddress Float Delay | | TCLAX | 35 | TCLAX | 44 | ns |
| TCHCZ | Command Lines Float Delay | | | 45 | | 56 | ns |
| TCHCV | Command Lines Valid Delay (After Float) | | | 55 | | 76 | ns |
| TLHLL | ALE Width | | TCLCL-35 | | TCLCL-35 | | ns |
| TCHLH | ALE Active Delay | | | 35 | | 44 | ns |
| TCHLL | ALE Inactive Delay | | | 35 | | 44 | ns |
| TLLAX | Address Hold to ALE Inactive | | TCHCL-25 | | TCHCL-30 | | ns |
| TCLDV | Data Valid Delay | | 5 | 44 | 5 | 55 | ns |
| TCLDOX | Data Hold Time | | 5 | | 5 | | ns |
| TWHDX | Data Hold after WR | | TCLCL-40 | | TCLCL-50 | | ns |
| TCVCTV | Control Active Delay1 | | 10 | 50 | 10 | 87 | ns |
| TCHCTV | Control Active Delay2 | | 5 | 73 | 5 | 76 | ns |
| TCVCTX | Control Inactive Delay | | 5 | 55 | 5 | 76 | ns |
| TCVDEX | $\overline{DEN}$ Inactive Delay (Non-Write Cycle) | | | 70 | | 87 | ns |
| TAZRL | Address Float to $\overline{RD}$ Active | | 0 | | 0 | | ns |
| TCLRL | $\overline{RD}$ Active Delay | | 10 | 70 | 10 | 87 | ns |
| TCLRH | $\overline{RD}$ Inactive Delay | | 10 | 55 | 10 | 76 | ns |
| TRHAV | $\overline{RD}$ Inactive to Address Active | | TCLCL-40 | | TCLCL-50 | | ns |
| TCLHAV | HLDA Valid Delay | | 5 | 67 | 5 | 67 | ns |
| TRLRH | $\overline{RD}$ Width | | 2TCLCL-50 | | 2TCLCL-50 | | ns |
| TWLWH | $\overline{WR}$ Width | | 2TCLCL-40 | | 2TCLCL-40 | | ns |
| TAVAL | Address Valid to ALE LOW | | TCLCH-25 | | TCLCH-45 | | ns |
| TCHSV | Status Active Delay | | 10 | 55 | 10 | 76 | ns |
| TCLSH | Status Inactive Delay | | 10 | 65 | 10 | 76 | ns |
| TCLTMV | Timer Output Delay | 100 pF Max. | | 60 | | 75 | ns |
| TCLRO | Reset Delay | | | 60 | | 75 | ns |
| TCHQSV | Queue Status Delay | | | 35 | | 44 | ns |
| TCHDX | Status Hold Time | | 10 | | 10 | | ns |
| TAVCH | Address Valid to Clock HIGH | | 10 | | 10 | | ns |

## SWITCHING CHARACTERISTICS (Cont'd.)

### 80186 Chip-Select Timing Responses

| Parameter Symbol | Parameter Description | Test Conditions | 80186 (8 MHz) | | 80186-6 (6 MHz) | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | |
| TCLCSV | Chip-Select Active Delay | | 5 | 66 | 5 | 80 | ns |
| TCXCSX | Chip-Select Hold from Command Inactive | | 35 | | 35 | | ns |
| TCHCSX | Chip-Select Inactive Delay | | 5 | 4 | 5 | 47 | ns |

### 80186 CLKIN Requirements

| Parameter Symbol | Parameter Description | Test Conditions | 80186 (8 MHz) | | 80186-6 (6 MHz) | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | |
| TCKIN | CLKIN Period | | 62.5 | 250 | 83.2 | 250 | ns |
| TCKHL | CLKIN Fall Time | 3.5 to 1.0 volts | | 10 | | 10 | ns |
| TCKLH | CLKIN Rise Time | 1.0 to 3.5 volts | | 10 | | 10 | ns |
| TCLCK | CLKIN Low Time | 1.5 volts | 25 | | 33 | | ns |
| TCHCK | CLKIN High Time | 1.5 volts | 25 | | 33 | | ns |

### 80186 CLKOUT Timing (200-pF load)

| Parameter Symbol | Parameter Description | Test Conditions | 80186 (8 MHz) | | 80186-6 (6 MHz) | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | |
| TCICO | CLKIN to CLKOUT Skew | | | 50 | | 62.5 | ns |
| TCLCL | CLKOUT Period | | 125 | 500 | 166 | 500 | ns |
| TCLCH | CLKOUT Low Time | 1.5 volts | ½TCLCL-7.5 | | ½TCLCL-7.5 | | ns |
| TCHCL | CLKOUT High Time | 1.5 volts | ½TCLCL-7.5 | | ½TCLCL-7.5 | | ns |
| TCH1CH2 | CLKOUT Rise Time | 1.0 to 3.5 volts | | 15 | | 15 | ns |
| TCL2CL1 | CLKOUT Fall Time | 3.5 to 1 volts | | 15 | | 15 | ns |

All timings measured at 1.5 volts unless otherwise noted.



## SWITCHING TEST INPUT/OUTPUT WAVEFORM


WF001870

AC testing inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0." The clock is driven at 4.3 V and 0.25 V. Timing measurements are made at 1.5 V for both a logic "1" and "0."