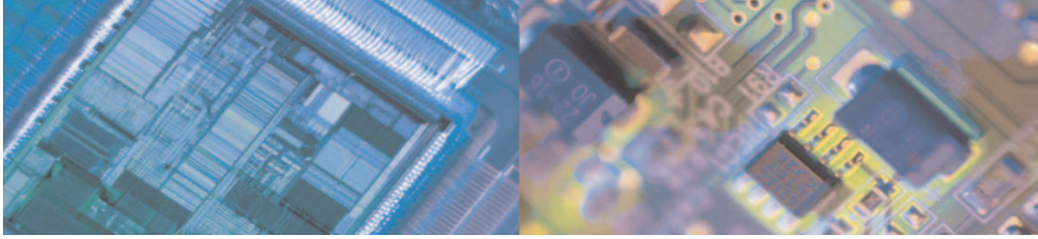
MATHSTAR™

Fast Silicon, Faster Solutions



Product Brief

The Builder Family

High performance solutions with the lowest cost of ownership

Applications

High Performance DSP

- FIR, Complex FFT
- Polyphase Filters
- Matched Filters
- Rake Receiver

High Performance Network Switch/Router

- Classification
- Policing
- Accounting

High Performance Storage

- TCP Offload Engine (TOE)
- Protocol Encapsulation/Conversion

Bridge Protocol Processing

- PCI Express - PCI Express
- Advanced switching
- Rapid I/O - HyperTransport

Features

- Ultra High Performance (1GHz max clock rates)
- I/O Bandwidth
  - 51.2Gb/s
- Memory Bandwidth
  - 36Gb/s
- High Functional Density
  - Performance Density >5x FPGA
- Libraries to Speed Design
- Rapid Time-to-Market
- No Fab Required
- Longest Time-in-Market
  - Reprogrammable Device

Overview

The Builder Series of products utilizes MathStar's revolutionary NoMASK™ technology to put the advantage of 130 nanometer and smaller processes into the engineer's hands. This revolutionary technology allows users to realize ultra high performance designs in a matter of weeks. There are no fabrication cycles, no physical timing to close and no expensive mask costs to pay. Yet, the 1GHz clock rate allows an unprecedented level of performance and ease of implementation. With MathStar's NoMASK products, 90% of the work is done. Customer solutions can be realized with a very short development that preserves your architecture and software. The reprogrammable nature of these products allows them to be upgraded in system, meaning that any product you implement can enjoy a long time in service. The revolutionary architecture of these devices is supported by a complete and familiar design interface. MathStar's simplified tool flow retains the familiar constructs of HDL design flows while eliminating the need to perform gate level synthesis and physical place and route for timing closure. The individual Builder series products comprise a core of the MathStar FPOA™ (Field Programmable Object Array) coupled with I/O blocks that are appropriate to the application and a set of library elements that enable rapid development cycles.

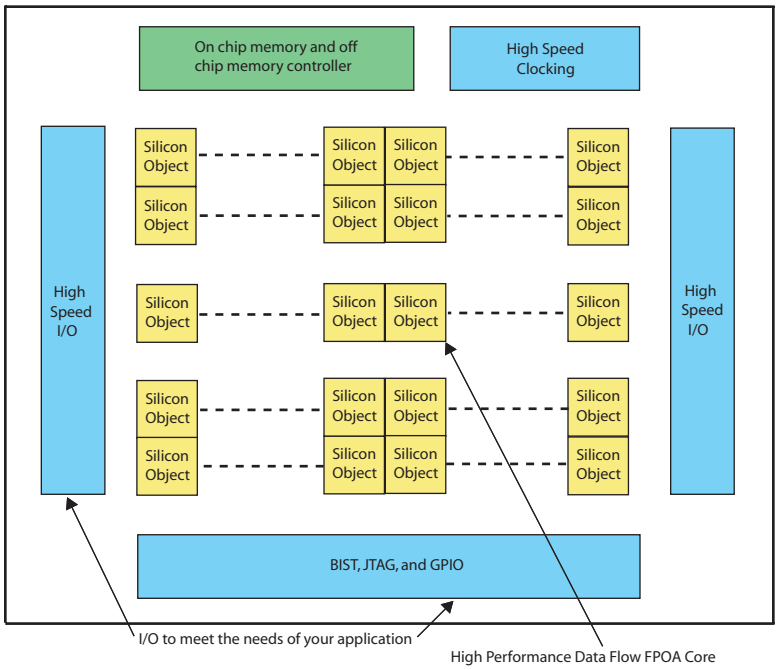


Figure 1. *Builder Series Silicon Object Architecture Diagram*

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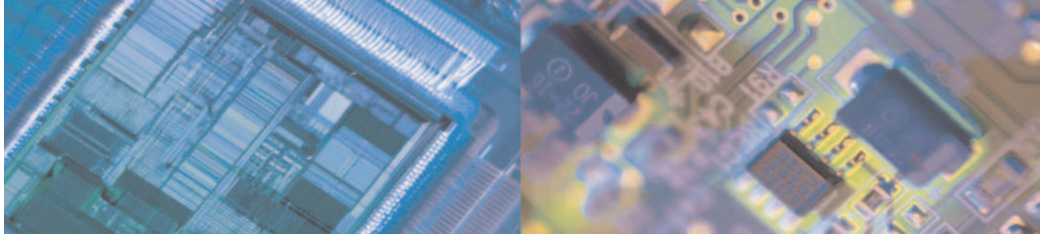

Product Lines

BridgeBuilder ™

- Custom(er) designed protocol conversions at up to 25.6Gb/s
- Line Rate Aggregation of varied protocols into one data stream
- Design upgradeable in the field as standards and needs change (IPv4 to IPv6)

FilterBuilder ™

- Ultra-high performance FFTs and FIRs
- Extreme DSP applications with over 64 single cycle 1GHz MACs

StorageBuilder ™

- Custom 1-10Gb/s TCP offload engines (TOE)
- Bridge and Aggregate serial storage protocols

SecurityBuilder ™

- Custom versions of security protocols at up to 10Gb/s
- Products that can adapt to the changing security environment

SwitchBuilder ™

- High performance switching for PCI-Express, Fibre Channel, Ethernet, Rapid I/O, and others

Design Flow

The MathStar NoGATES™ design flow means that there is no gate level synthesis and no timing closure.

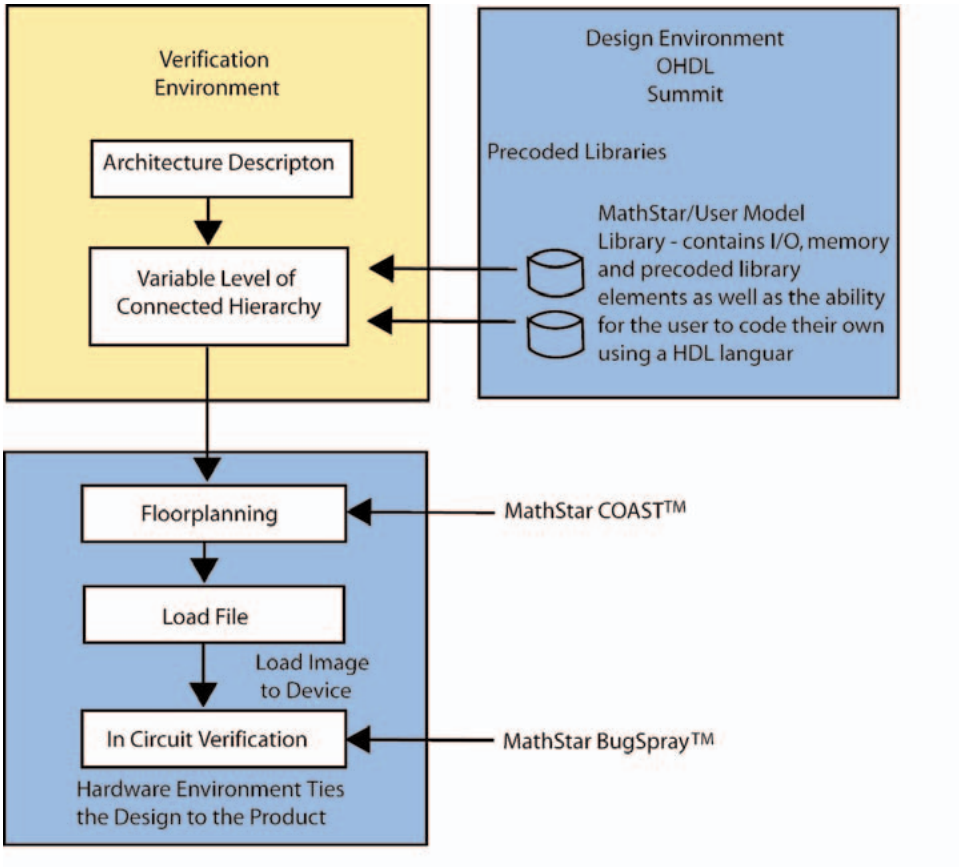

Figure 2. *Builder Series Tools Flow Diagram*

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