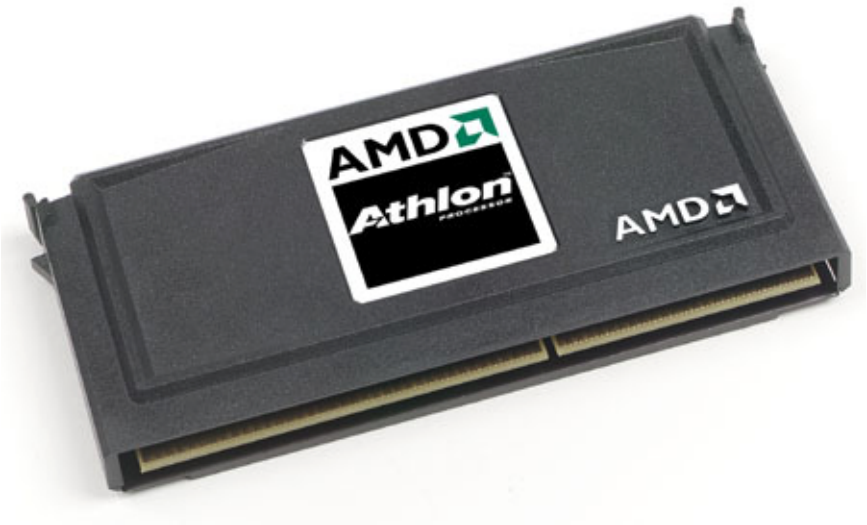
AMD

Version Created August 3, 2000

AMD Athlon™ Processor Model 1 and Model 2 Revision Guide



Publication # **22557** Rev: **D**
Issue Date: **August 2000**

AMD Athlon™ Processor Revision Guide

The purpose of the *AMD Athlon™ Processor Revision Guide* is to communicate updated product information on the AMD Athlon model 1 and model 2 processors to designers of computer systems and software developers. This guide consists of five sections:

- **Product Marking Identification:** This section, which starts on page 2, provides product types, product revisions, OPNs (Ordering Part Numbers), and product marking information.
- **Product Errata:** This section, which starts on page 4, provides a detailed description of product errata, including potential effects on system operation and suggested workarounds. An erratum is defined as a deviation from the product's specification. Product errata may cause the behavior of the AMD Athlon processor to deviate from the published specifications.
- **Product Enhancements:** This section, which starts on page 11, provides a description of product enhancements.
- **Revision Determination:** This section, which starts on page 12, shows the AMD Athlon processor identification numbers returned by the CPUID instruction for each revision of the processor.
- **Technical and Documentation Support:** This section, which starts on page 13, provides a listing of available technical support resources. It also lists corrections, modifications, and clarifications to listed documents.

Revision Guide Policy

Occasionally, AMD identifies deviations from or changes to the specification of the AMD Athlon processor. These changes are documented in the *AMD Athlon Processor Model 1 and Model 2 Revision Guide* as errata. Descriptions are written to assist system and software designers in using the AMD Athlon processor, and corrections to AMD's documentation on the AMD Athlon processor are included. This release documents currently characterized product errata.

1 Product Marking Identification

1.1 Production Marking

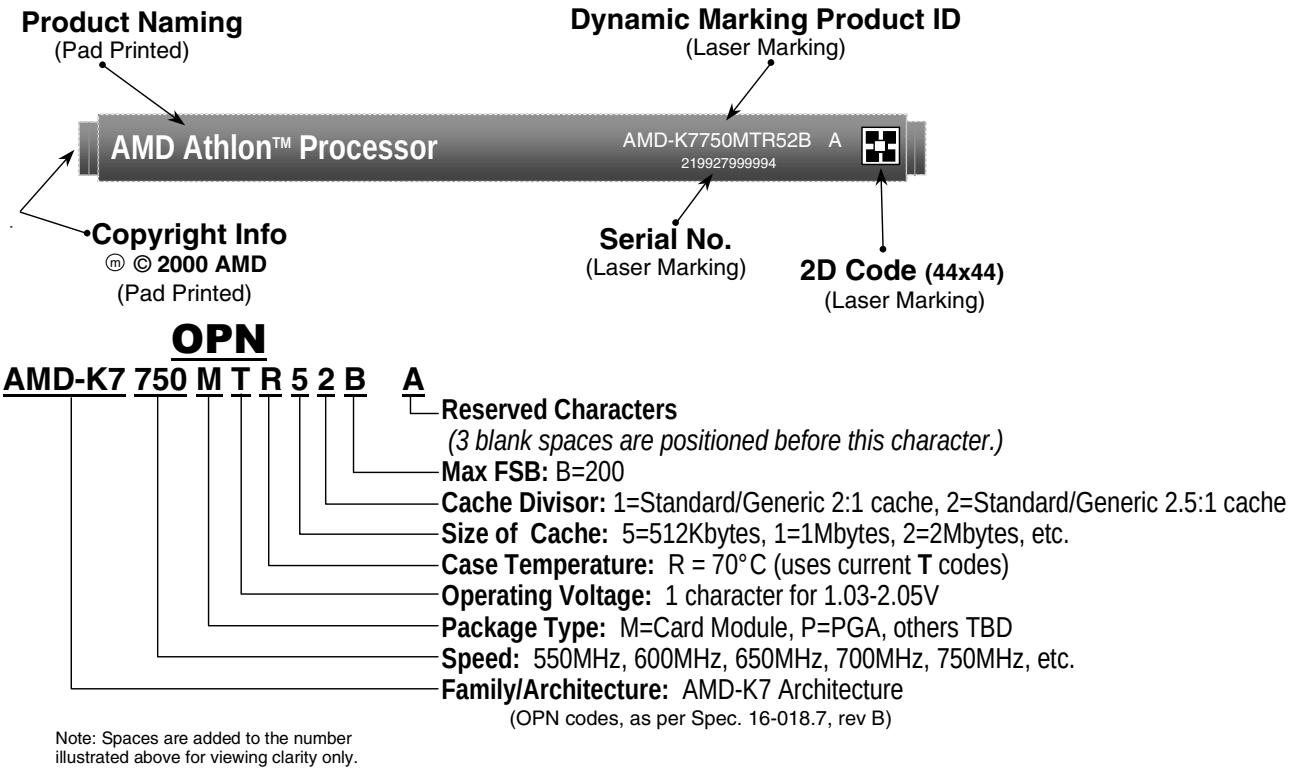


Figure 1. OPN Example for the AMD Athlon™ Processor Model 2

Table 1. Valid Ordering Part Number Combinations for Model 2

OPN	Package Type	Operating Voltage	Plate Temperature
AMD-K7550MTR51B A	Card Module	1.55V–1.65V	0°C–70°C
AMD-K7600MTR51B A	Card Module	1.55V–1.65V	0°C–70°C
AMD-K7650MTR51B A	Card Module	1.55V–1.65V	0°C–70°C
AMD-K7700MTR51B A	Card Module	1.55V–1.65V	0°C–70°C
AMD-K7750MTR52B A	Card Module	1.55V–1.65V	0°C–70°C
AMD-K7800MPR52B A	Card Module	1.65V–1.75V	0°C–70°C
AMD-K7850MPR52B A	Card Module	1.65V–1.75V	0°C–70°C

Notes:
This table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly-released combinations.

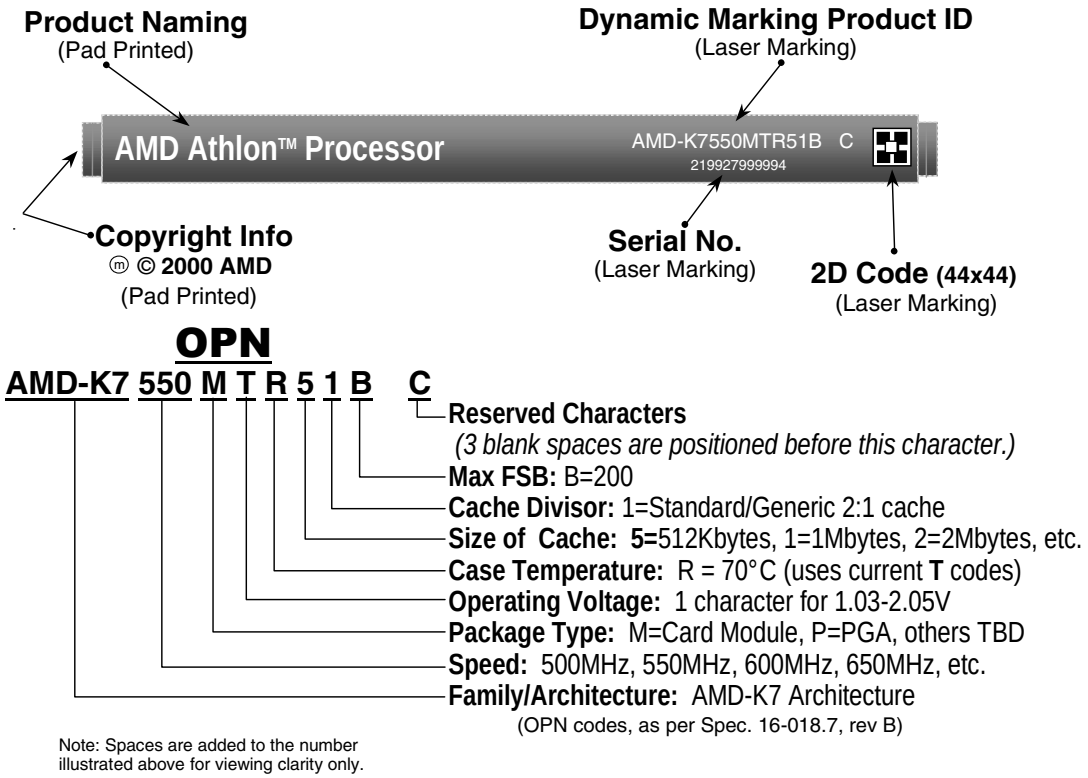


Figure 2. OPN Example for the AMD Athlon™ Processor Model 1

Table 2. Valid Ordering Part Number Combinations for Model 1

OPN	Package Type	Operating Voltage	Plate Temperature
AMD-K7500MTR51B C	Card Module	1.55V–1.65V	0°C–70°C
AMD-K7550MTR51B C	Card Module	1.55V–1.65V	0°C–70°C
AMD-K7600MTR51B C	Card Module	1.55V–1.65V	0°C–70°C
AMD-K7650MTR51B C	Card Module	1.55V–1.65V	0°C–70°C
AMD-K7700MTR51B C	Card Module	1.55V–1.65V	0°C–70°C

Notes:

This table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly-released combinations.

2 Product Errata

This section documents AMD Athlon processor model 1 and model 2 product errata. The errata are divided into categories to assist referencing particular errata. A unique tracking number for each erratum has been assigned within this document for user convenience in tracking the errata within specific revision levels. Table 3 cross-references the revisions of the processor to each erratum. An "X" indicates that the erratum applies to the stepping. The absence of an "X" indicates that the erratum does not apply to the stepping. Shading within the table indicates an addition or modification from the previous release of this document.

Note: *There can be missing errata numbers. Errata that have been resolved from early revisions of the processor have been deleted, and errata that have been reconsidered may have been deleted or renumbered.*

Table 3. Cross-Reference of Product Revision to Errata

Errata Numbers and Description	Revision Numbers			
	Model 1		Model 2	
	C1	C2	A1	A2
Processor Internals				
1 Self-Modifying Code End Case: Execution of Stale Instruction	X	X		
12 MCA Bus Unit Control Register MSR 408H Returns Incorrect Information	X	X	X	X
13 Hangs During Microsoft Windows 98 Suspend/Resume Sequence	X	X	X	X
PREFETCH				
3 Interaction of PREFETCH Followed by Stores to Writethrough, Cache-Disabled, and Write-Protected (WT/CD/WP) Memory Types	X	X		
Large Page Mappings				
5 Large Page Mappings Suppressed When SMM TSEG Range Is Enabled	X	X		
6 Large Page Mappings Not Suppressed When SMM ASEG Range Is Enabled	X	X		

Processor Internals

1 Self-Modifying Code End Case: Execution of Stale Instruction

Products Affected. C1 and C2

Normal Specified Operation. Code-modifying store flushes in-flight instructions from the pipeline.

Non-conformance. Under specific extreme conditions, an in-flight instruction can escape detection by the internal self-modifying code mechanisms, resulting in the possible execution of a stale instruction.

The following conditions are required for this erratum to occur:

- The instruction being modified is initially present in the instruction cache and data cache simultaneously.
- The code modifying store correctly determines that an instruction cache line invalidation is required.
- The stale instruction is fetched and launched in-flight just as the invalidation arrives.
- No other instructions from that cache line are in-flight anywhere in the processor.

Under these conditions, a one-time execution of the unmodified (stale) instruction may occur, even though the line is correctly invalidated from the instruction cache.

Potential Effect on System. None is expected. This non-conformance has never been detected in real system software.

Suggested Workaround. None.

Resolution Status. Fix planned for future Revision.

12 MCA Bus Unit Control Register MSR 408H Returns Incorrect Information

Products Affected. C1, C2, A1, and A2

Normal Specified Operation. System reads to MSR 408h, MCA Bus Unit Control Register, should return correct information.

Non-conformance. Reads to the Machine Check Architecture (MCA) Bus Unit Control MSR 408h return incorrect information. It returns the information stored in the upper 32 bits of the BU Status MSR 409h instead.

Potential Effect on System. If the system reads this MCA control register, the upper 32 bits, which are reported in EDX, can contain unexpected data.

Suggested Workaround. This register is only implemented as a 32-bit register. Ignore the upper 32 bits which are reported in EDX.

Resolution Status. No fix planned.

13 Hangs During Microsoft Windows 98 Suspend/Resume Sequence

Products Affected. All

Normal Specified Operation. The processor should resume properly after a wakeup event while in a system suspend mode.

Non-conformance. Some processor modules contain L2 cache SRAMs that support a low-power mode. During a suspend/resume sequence (e.g. Microsoft Windows 98 suspend), the processor directs these SRAMs to enter and exit the low-power mode. However, at elevated temperatures, a small percentage of SRAM devices do not properly exit this mode. The result is cache corruption and possible system lockup.

Potential Effect on System. Some processor modules may cause the system to hang.

Suggested Workaround. The BIOS can prevent these L2 cache SRAMs from entering a low-power state during a Microsoft Windows 98 suspend mode. Please see "AMD Athlon Processor L2 Cache Initialization Application Note" order number 23165, revision B, for a description of the recommended change.

Resolution Status. No fix planned.

PREFETCH

3 Interaction of PREFETCH Followed by Stores to Writethrough, Cache-Disabled, and Write-Protected (WT/CD/WP) Memory Types

Products Affected. C1 and C2

Normal Specified Operation. The processor maintains cache coherency.

Non-conformance. If a WP line is prefetched and subsequently stored to (within execution of a few dozen instructions and before any intervening loads), then the just-prefetched line may not be invalidated when the store is sent to the external system.

If a WT line is prefetched and subsequently stored to (within execution of a few dozen instructions and before any intervening loads), then the just-prefetched line may not be written to when the store is sent to the external system.

Other versions of the WT failure can also be encountered via several aliased, page-mapping scenarios:

- Prefetch WB line, store to via PWT mapping
- Prefetch WB line, store to via PCD mapping
- Prefetch WT line, store to via PCD mapping

Potential Effect on System. None expected because these memory types are generally not used with the PREFETCH instruction. However, if PREFETCH is used with the WT/WP memory types, the store goes to the bus, leaving the just prefetched line in the cache in an incoherent state.

Suggested Workaround. None. These memory types are generally not used with PREFETCH.

Resolution Status. Fix planned for future Revision.

Large Page Mappings

5 Large Page Mappings Suppressed When SMM TSEG Range Is Enabled

Products Affected. C1 and C2

Normal Specified Operation. When the SMM TSEG range is enabled, the AMD Athlon processor should suppress the use of any large page (2 Mbytes/4 Mbytes) mappings that overlap this range.

Non-conformance. This erratum may result in a slight performance degradation. There is no functional impact. The AMD Athlon processor suppresses the use of all large page mappings when the SMM TSEG range is enabled—whether they intersect that region or not.

Potential Effect on System. Any system that employs the SMM TSEG range does not derive a performance benefit from using large pages. All large page mappings are decomposed into 4-Kbyte fragments and cached in the normal 4-Kbyte TLBs. This behavior does not depend on whether or not the processor is in SMM at the time. Rather, it occurs whenever the SMM TSEG range is enabled for the system.

Suggested Workaround. The following workarounds are possible:

- Do nothing. This erratum is a performance issue only.
- Do not use the SMM TSEG range (use only the legacy ASEG range).
- Enable the SMM TSEG range only while the processor is in SMM (from the ASEG range).

Resolution Status. Fix planned for future Revision.

6 Large Page Mappings Not Suppressed When SMM ASEG Range Is Enabled

Products Affected. C1 and C2

Normal Specified Operation. When the SMM ASEG range is enabled, the AMD Athlon processor should suppress the use of any large page (2 Mbytes/4 Mbytes) mappings that overlap that range.

Non-conformance. When the SMM ASEG range is enabled, the AMD Athlon processor does not suppress the large page mappings that overlap that range.

Potential Effect on System. This non-conformance has not been observed in any system software. This non-conformance is of no consequence because any system that uses the SMM ASEG range (the legacy SMM range) also uses the fixed range MTRRs to map out the first Mbyte of the address space. The enabling of the fixed range MTRRs itself causes the required large page decomposition behavior in this region. The problem could only be made visible if a system (that used a large page mapping in the first 2 Mbytes/4 Mbytes) employed the SMM ASEG range but did not employ the fixed range MTRRs. No such system is known to exist.

Suggested Workaround. None

Resolution Status. Fix planned for future Revision.

3 Product Enhancements

Enhancements for Model 2, Stepping 2 and Greater

PDEs and PTEs in Cacheable DRAM

The TLB force cacheable (TLBC) bit in the hardware control register (bit 3 of the HWCR) forces TLB reload accesses to be to DRAM and to be cacheable, independent of the MTRR configuration. This bit is ignored if the L2 cache is disabled. The reset state of this bit is cleared.

When TLBC is set, the processor assumes PDEs and PTEs are in cacheable memory. This feature allows for potential performance improvements.

For detailed information regarding this enhancment, see the *AMD Athlon Processor BIOS Developers Guide*, order number 21656.

4 Revision Determination

Table 4 shows the AMD Athlon processor identification numbers returned by the CPUID instruction for each revision of the processor.

Table 4. CPUID Values for the Revisions of the AMD Athlon™ Processor

Revision	CPUID
C1	611
C2	612
A1	621
A2	622

5 Technical and Documentation Support

5.1 Documentation Support

The following documents provide additional information regarding the operation of the AMD Athlon processor:

- *AMD Athlon™ Processor Data Sheet* (order# 21016)
- *AMD-751™ System Controller Data Sheet* (order# 21910)
- *AMD-756™ Peripheral Bus Controller Data Sheet* (order# 22548)
- *AMD Athlon™ System Bus Specification* (order# 21902)
- *AMD Athlon™ Processor BIOS, Software, and Debug Tools Developers Guide* (order# 21656)

For the latest updates, refer to www.amd.com and download the appropriate files. For documents under NDA, please contact your local sales representative for updates.