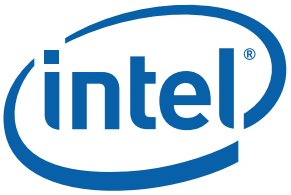

# 2nd Generation Intel® Core™ Processor Family Mobile

## Thermal Design Guide for Embedded Applications

*March 2013*

**Revision 003**

Order Number: 325676

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# Revision History

| Date | Revision | Description |
|---|---|---|
| June 2010 | 001 | Initial release of this document |
| May 2012 | 002 | Updated to include 2CF package designs |
| March 2013 | 003 | Fixed typo in Equation 4 |

# 1.0 Introduction

The power needs of electronic components has risen along with the increase in complexity of computer systems. To ensure quality, reliability, and performance goals are met over the product's life cycle, the heat generated by the device must be properly dissipated. Typical methods to improve heat dissipation include selective use of airflow ducting, and/or the use of heatsinks.

The goals of this document are to:

- Specify the thermal and mechanical specification for the device.
- Describe a reference thermal solution that meets the specifications.

A properly designed thermal solution will adequately cool the device at or below the thermal specification. This is accomplished by providing a suitable local-ambient temperature, ensuring adequate local airflow, and minimizing the die to local-ambient thermal resistance. Operation outside the functional limits can degrade system performance and may cause permanent changes in the operating characteristics of the component.

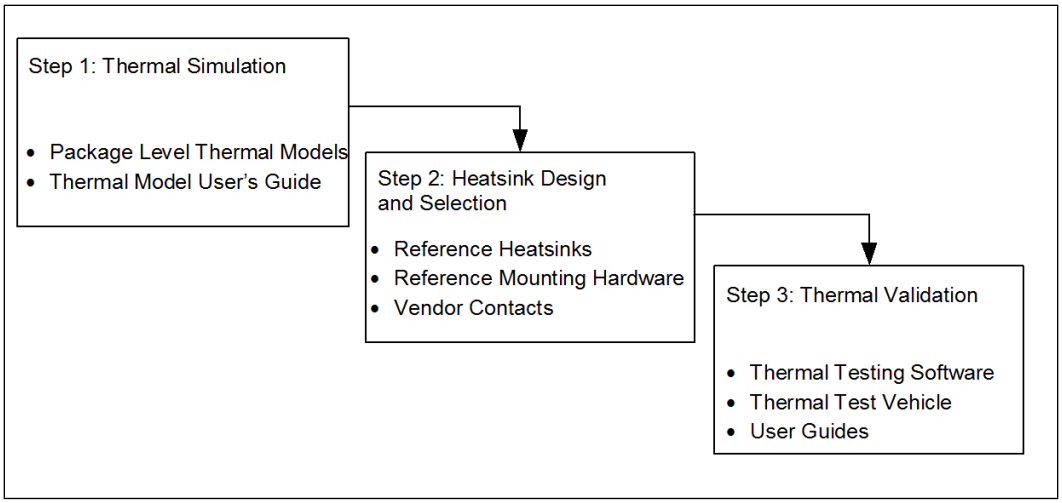
This document describes thermal design guidelines for the 2nd Generation Intel® Core™ Processor Family Mobile in the micro-Flip Chip Pin Grid Array (micro-FCPGA988) package and the micro-Flip Chip Ball Grid Array (micro-FCBGA1023) package. The information provided in this document is for reference only, and additional validation must be performed prior to implementing the designs into final production. The intent of this document is to assist each original equipment manufacturer (OEM) with the development of thermal solutions for their individual designs. The final heatsink solution, including the heatsink, attachment method, and thermal interface material (TIM) must comply with the mechanical design, environmental, and reliability requirements delineated in the processor datasheet. It is the responsibility of each OEM to validate the thermal solution design with their specific applications.

This document addresses thermal and mechanical design specifications for the 2nd Generation Intel® Core™ Processor Family Mobile only. For thermal design information on other Intel components, refer to their respective thermal mechanical design guidelines.

## 1.1 Design Flow

Intel provides several tools to assist in the development of a reliable, cost-effective thermal solution. Figure 1 illustrates a typical thermal solution design process with available tools noted. The tools are available through your local Intel field sales representative.

**Figure 1. Thermal Design Process**




## 1.2 Definition of Terms

**Table 1. Definition of Terms (Sheet 1 of 2)**

| Term | Definition |
|---|---|
| FCPGA | Flip Chip Pin Grid Array. A pin grid array packaging technology where the die is exposed on the package substrate. |
| FCBGA | Flip Chip Ball Grid Array. A ball grid array packaging technology where the die is exposed on the package substrate. |
| $T_{JUNCTION-MAX}$ | Maximum allowed component (junction) temperature. Also referred to as $T_{J-MAX}$ |
| TDP | Thermal Design Power. Thermal solutions should be designed to dissipate this target power level. |
| $T_{LA}$ | Local ambient temperature. This is the temperature measured inside the chassis, approximately 1 inch upstream of a component heatsink. Also referred to as $T_A$. |
| $\Psi_{JA}$ | Junction-to-ambient thermal characterization parameter. A measure of heatsink thermal performance using the total package power. Defined as ($T_{JUNCTION} - T_{LA}$) / Total Package Power |
| $\Psi_{TIM}$ | Thermal interface material thermal characterization parameter. A measure of thermal interface material performance using total package power. Defined as ($T_{CASE} - T_{JUNCTION}$)/ Total Package Power. Also referred to as $\Psi_{JS}$. |
| $\Psi_{SA}$ | Sink-to-ambient thermal characterization parameter. A measure of heatsink thermal performance using total package power. Defined as ($T_{SINK} - T_{JUNCTION}$)/ Total Package Power. |
| °C | Degrees in Celsius |
| CFM | Volumetric airflow rate in cubic feet per minute |
| in. | Inches |
| LFM | Airflow velocity in linear feet per minute |
| PCB | Printed circuit board |
| $T_{SINK}$ | Heatsink temperature measured on the underside of the heatsink base. |
| TIM | Thermal Interface Material – the thermally conductive compound between the heatsink and die. This material fills air gaps and voids, and enhances spreading of the heat from the die to the heatsink. |

**Table 1. Definition of Terms (Sheet 2 of 2)**

| Term | Definition |
|---|---|
| U | A unit of measure used to define server rack spacing height. 1U is equal to 1.75 inches, 2U equals 3.50 inches, etc. |
| W | Watt |
| $T_{FAN}$ | Represents the temperature at which fans must be at full speed |

## 1.3 Referenced Documents

Readers should also be familiar with material and concepts presented in the following documents:

- *2nd Generation Intel® Core™ Processor Family Mobile Datasheet- Volume One Doc#324692-001*
- *2nd Generation Intel® Core™ Processor Family Mobile Datasheet- Volume Two Doc#324803-001*
- *Huron River Thermal Mechanical Design Guide - Doc#445771*
- *rPGA988/989 Socket Application Guide* - D*oc#419940*
- Huron River Thermal Models (FloTHERM*/Icepak*)- Doc*# 439914*

## 1.4 Thermal Design Tool Availability

Intel provides thermal simulation models of the device and a thermal model user's guide to aid system designers in simulating, analyzing, and optimizing thermal solutions in an integrated, system-level environment. The models are for use with commercially available Computational Fluid Dynamics (CFD)-based thermal analysis tools including FloTHERM* (version 8.1 or higher) by Mentor Graphics or Icepak* by ANSYS.

# 2.0 Package Information

The 2nd Generation Intel® Core™ Processor Family Mobile utilizes a 31X24 mm, 1023-ball micro-FCBGA (BGA1023) package and 37.5 x 37.5 mm, 988-pin micro-FCPGA (rPGA988) package. For both micro-FCPGA and micro-FCBGA processors, there will be two different package designs that either have a 2C (2-Core) or a 4C (4-Core) die with the only difference being the die size. Also included in the package designs are 2CF (2-Core Fused) die, meaning a 2C fused from a 4C die. A 2CF die is the same size as a 4C die therefore, it is important to discern between 2C and 2CF before integrating the processor into a system design. Refer to Table 2 for core count vs. active core list. Refer to the device's most recent datasheet for up-to-date information. In the event of conflict, the device's datasheet supersedes data presented in this document.

The processors in the micro-FCPGA package connect to the motherboard through a 988-pin surface mount, Zero Insertion Force (ZIF) socket. A description of the socket can be found in the *rPGA988/989 Socket Application Guide*.

The land-side capacitors are electrically conductive, so avoid contacting the capacitors with any other electrically conductive materials. Doing so may short the capacitors and possibly damage the device or render it inactive.

The processor package has mechanical load limits that are specified in the processor datasheet. These load limits should not be exceeded during heatsink installation, removal, mechanical stress testing, or standard shipping conditions. The heatsink mass can also add additional dynamic compressive load to the package during a mechanical shock event. Amplification factors due to the impact force during shock must be taken into account in dynamic load calculations. The total combination of dynamic and static compressive load should not then exceed the processor datasheet compressive dynamic load specification during a vertical shock. It is not recommended to use any portion of the processor substrate as a mechanical reference or load bearing surface in either static or dynamic compressive load conditions.

Figure 2 through Figure 5 show 3-dimensional, top and bottom views of the 2nd Generation Intel® Core™ Processor Family Mobile rPGA988 and BGA1023 packages in 2C and 4C/2CF designs. Figure 6 through Figure 13 contain:

- Detailed mechanical dimensions for all packages
- Keep-out zones for thermal attach hardware corresponding to each of the packages outline.

**Figure 2. 3-D View of Top/ Bottom of BGA1023 2C Package for the 2nd Generation Intel® Core™ Processor Family Mobile**

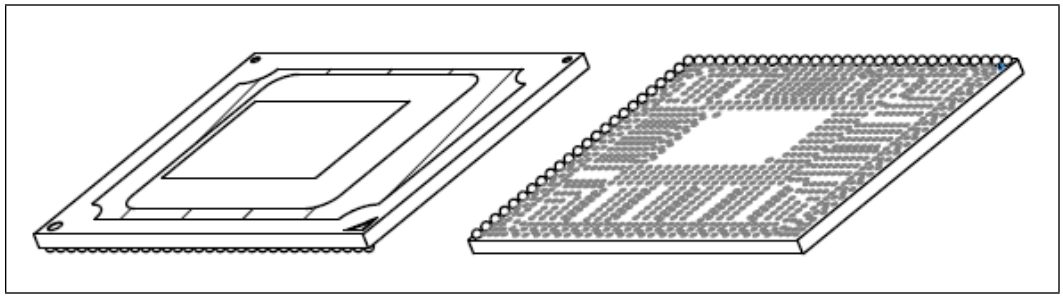


**Figure 3. 3-D View of Top/ Bottom of BGA1023 4C/2CF Package for the 2nd Generation Intel® Core™ Processor Family Mobile**

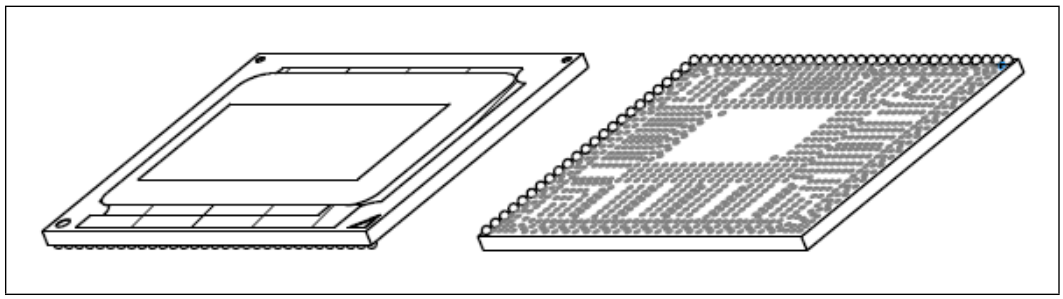


**Figure 4. 3-D View of Top/ Bottom of rPGA988 2C Package for the 2nd Generation Intel® Core™ Processor Family Mobile**

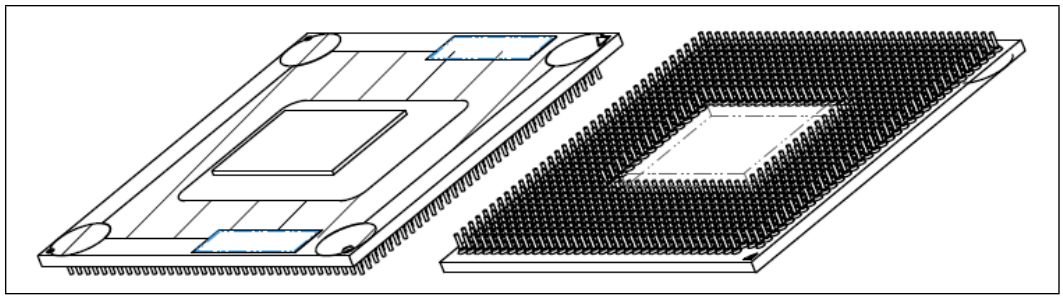
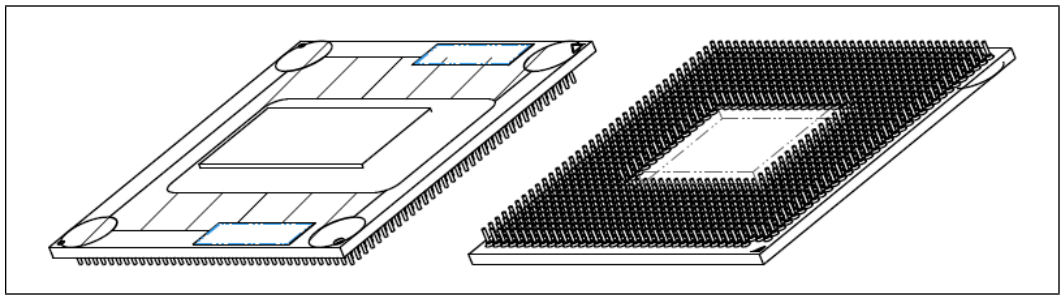
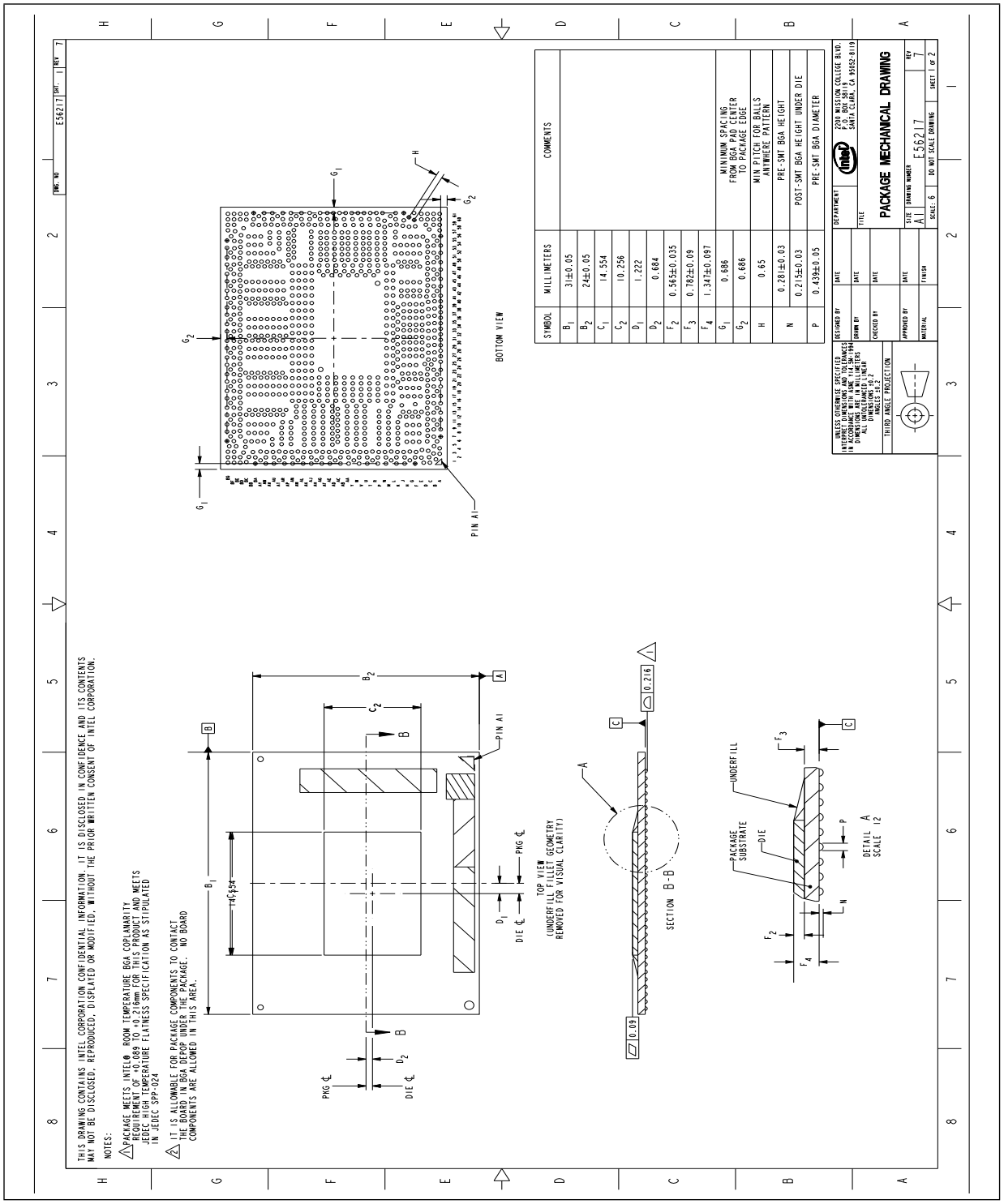


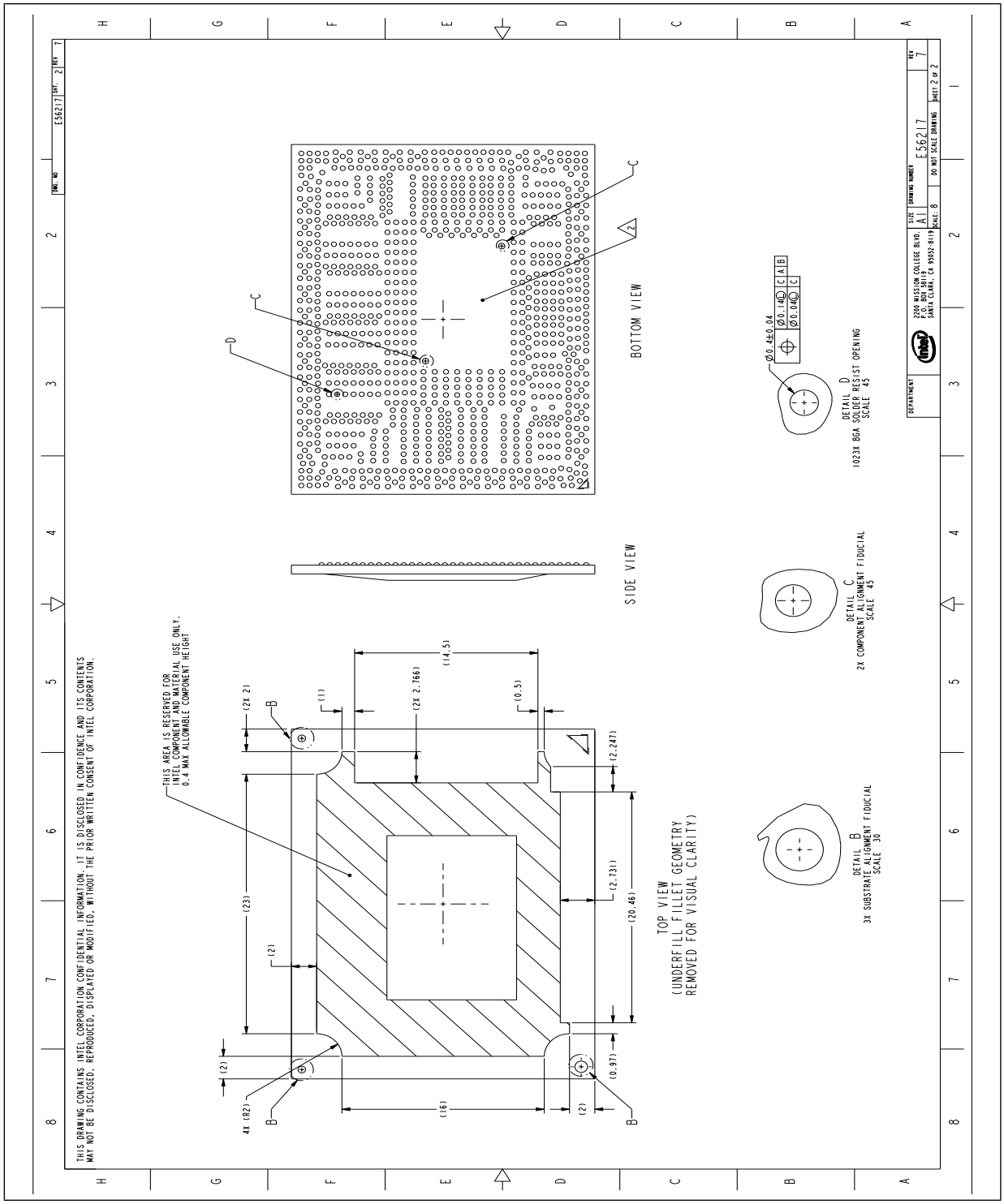
**Figure 5. 3-D View of Top/ Bottom of rPGA988 4C/2CF Package for the 2nd Generation Intel® Core™ Processor Family Mobile**



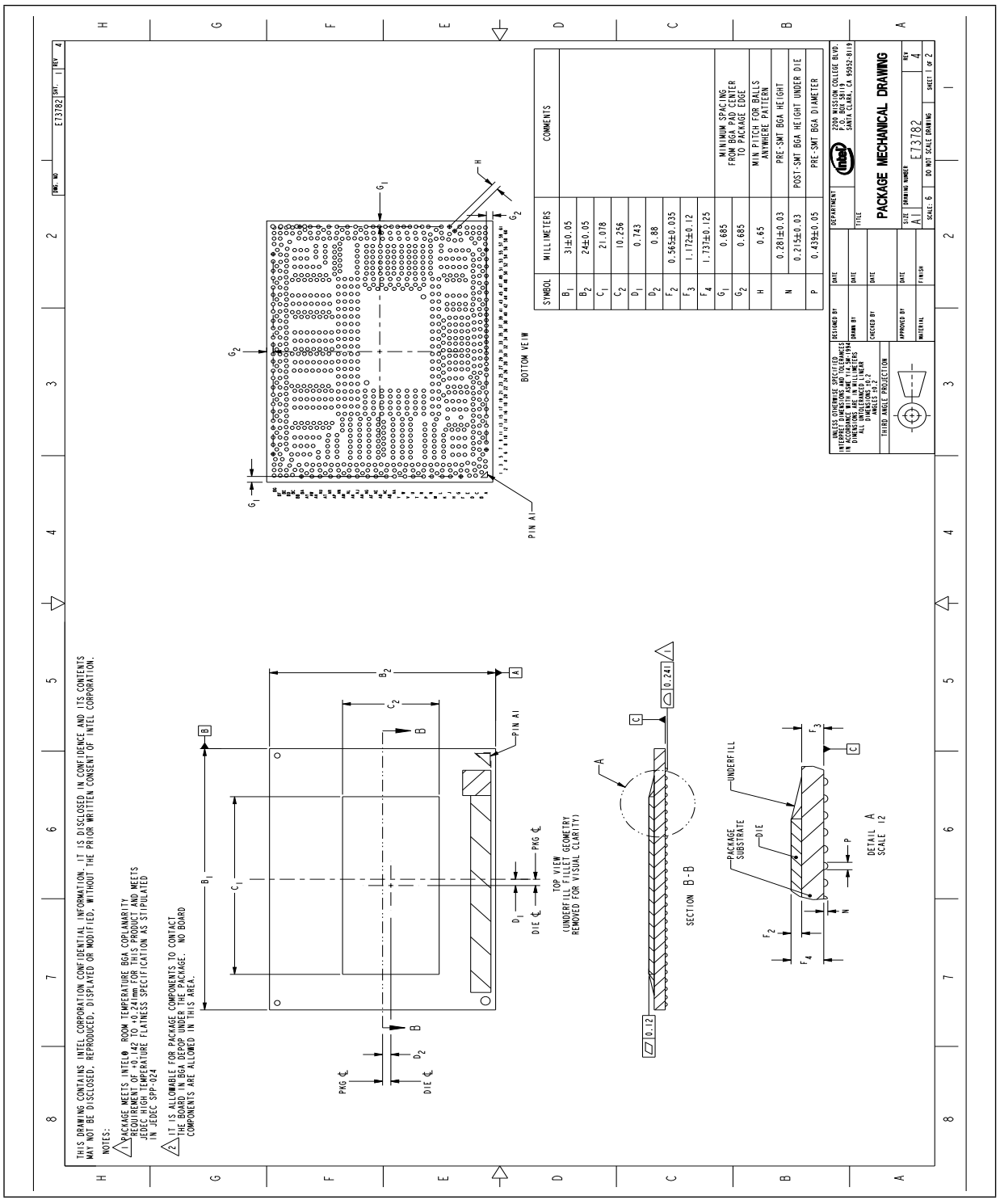
## Figure 6. 2nd Generation Intel® Core™ Processor Family Mobile BGA1023 2C Package



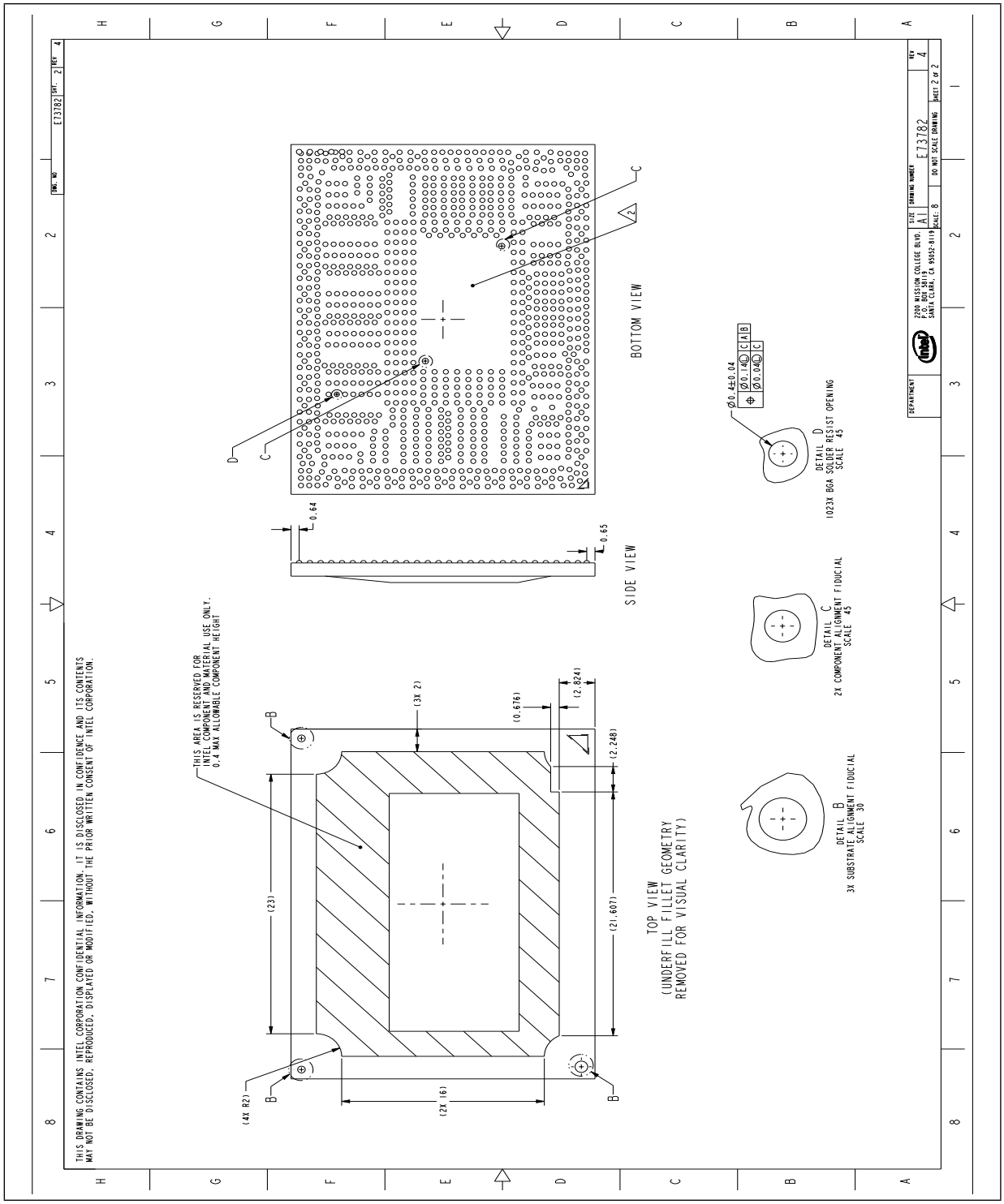
## Figure 7. 2nd Generation Intel® Core™ Processor Family Mobile BGA1023 2C Package Keep-Out Zones



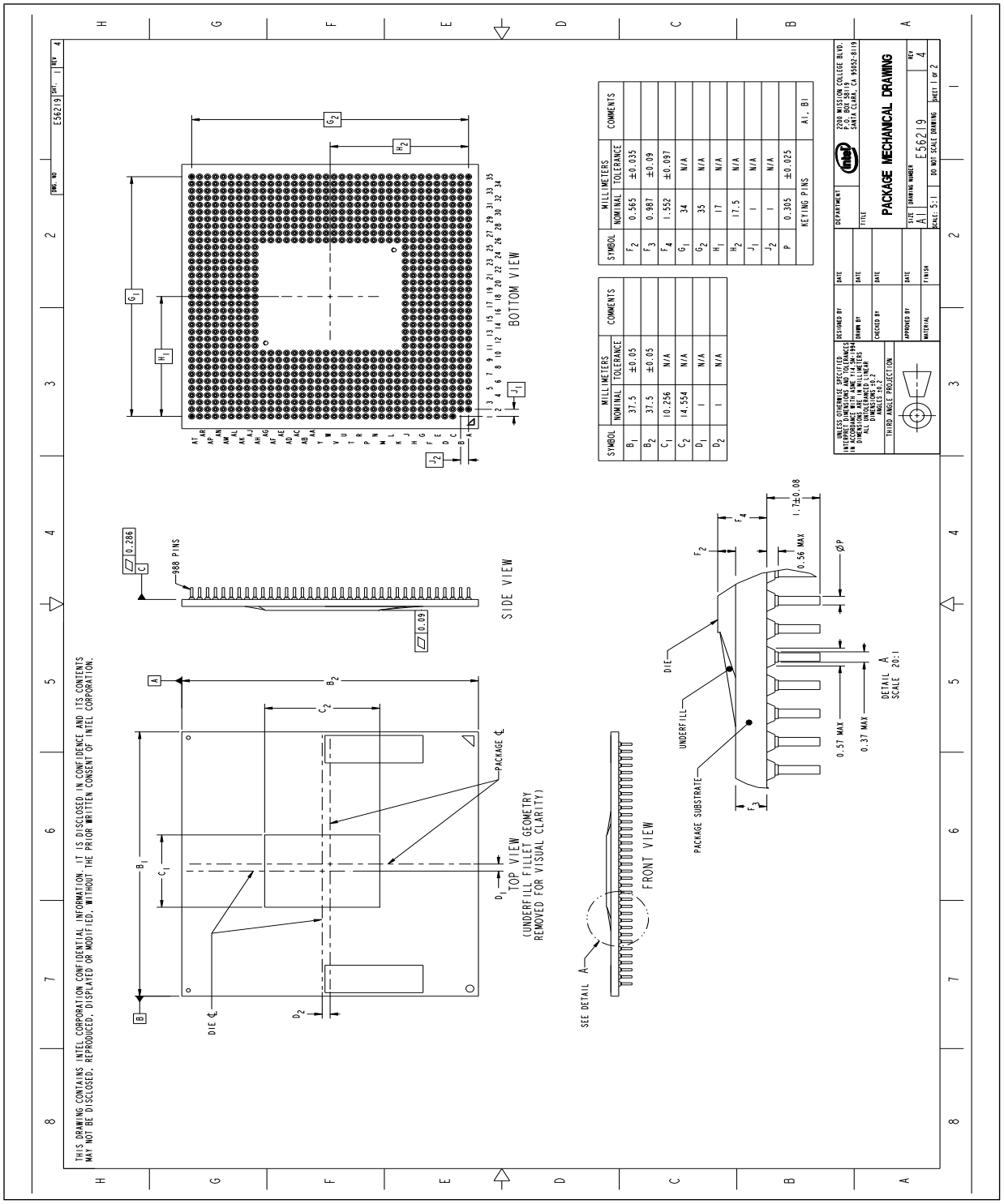
## Figure 8. 2nd Generation Intel® Core™ Processor Family Mobile BGA1023 4C/2CF Package



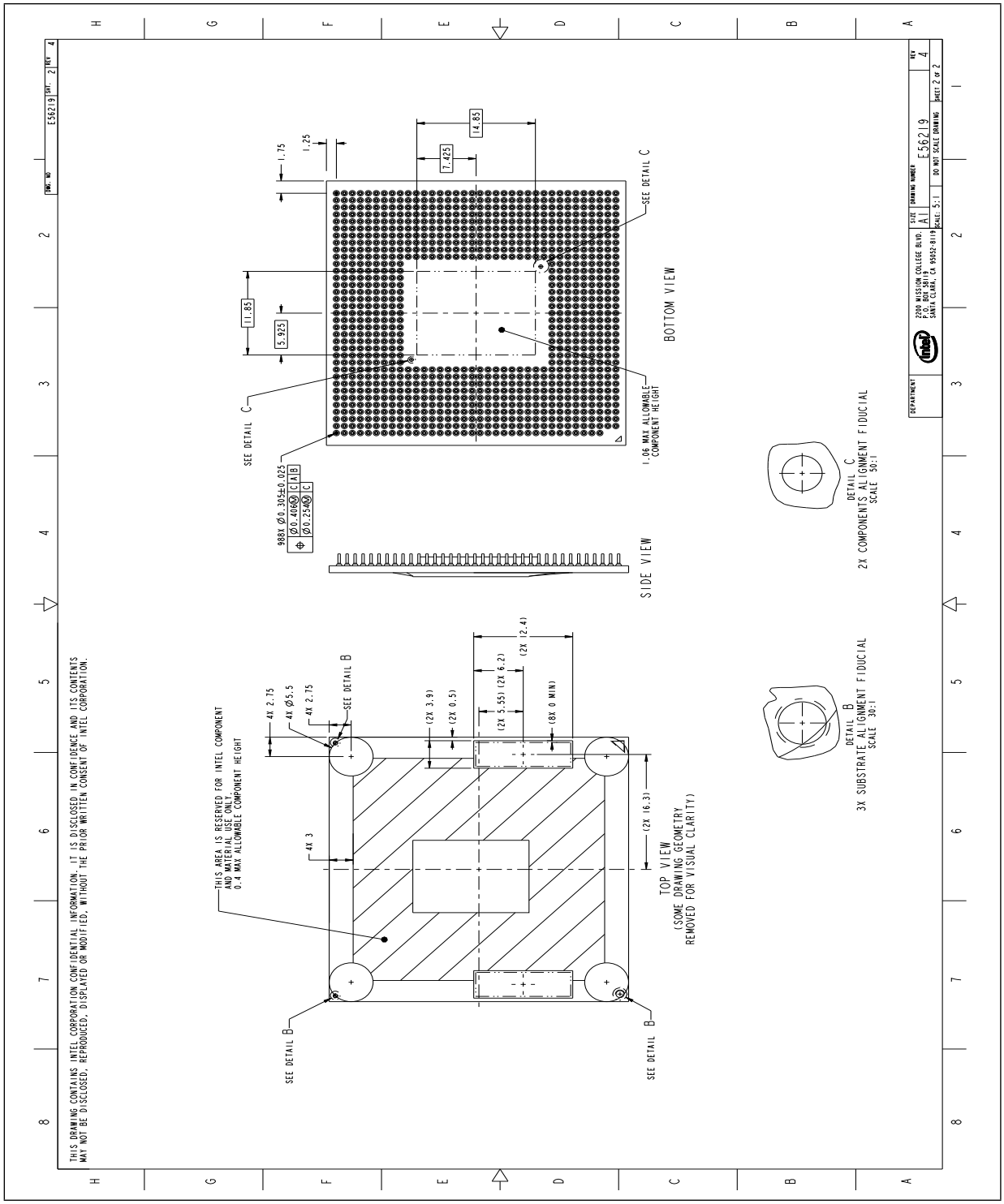
## Figure 9. 2nd Generation Intel® Core™ Processor Family Mobile BGA1023 4C/2CF Package Keep-Out Zones



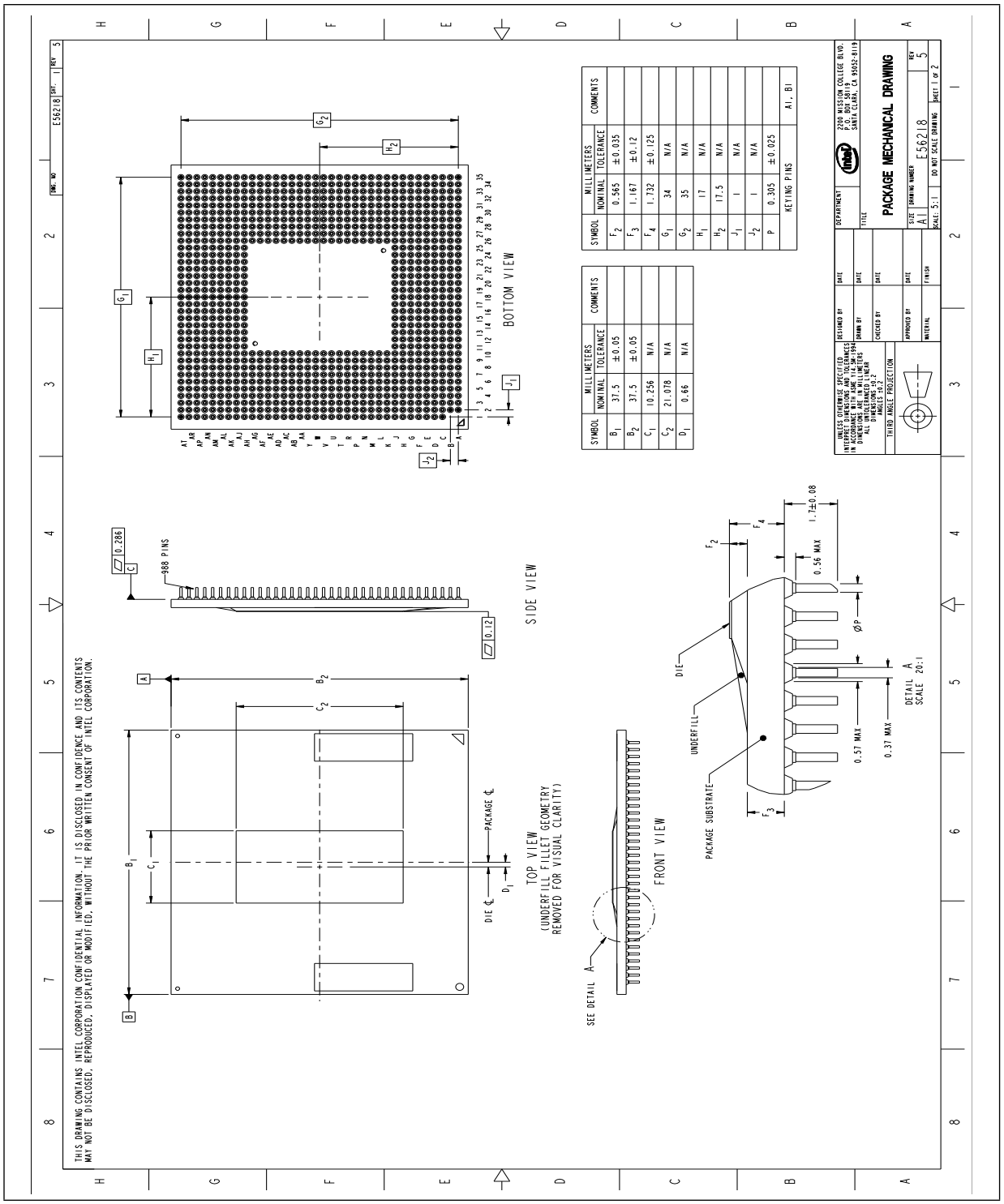
## Figure 10. 2nd Generation Intel® Core™ Processor Family Mobile rPGA988 2C Package



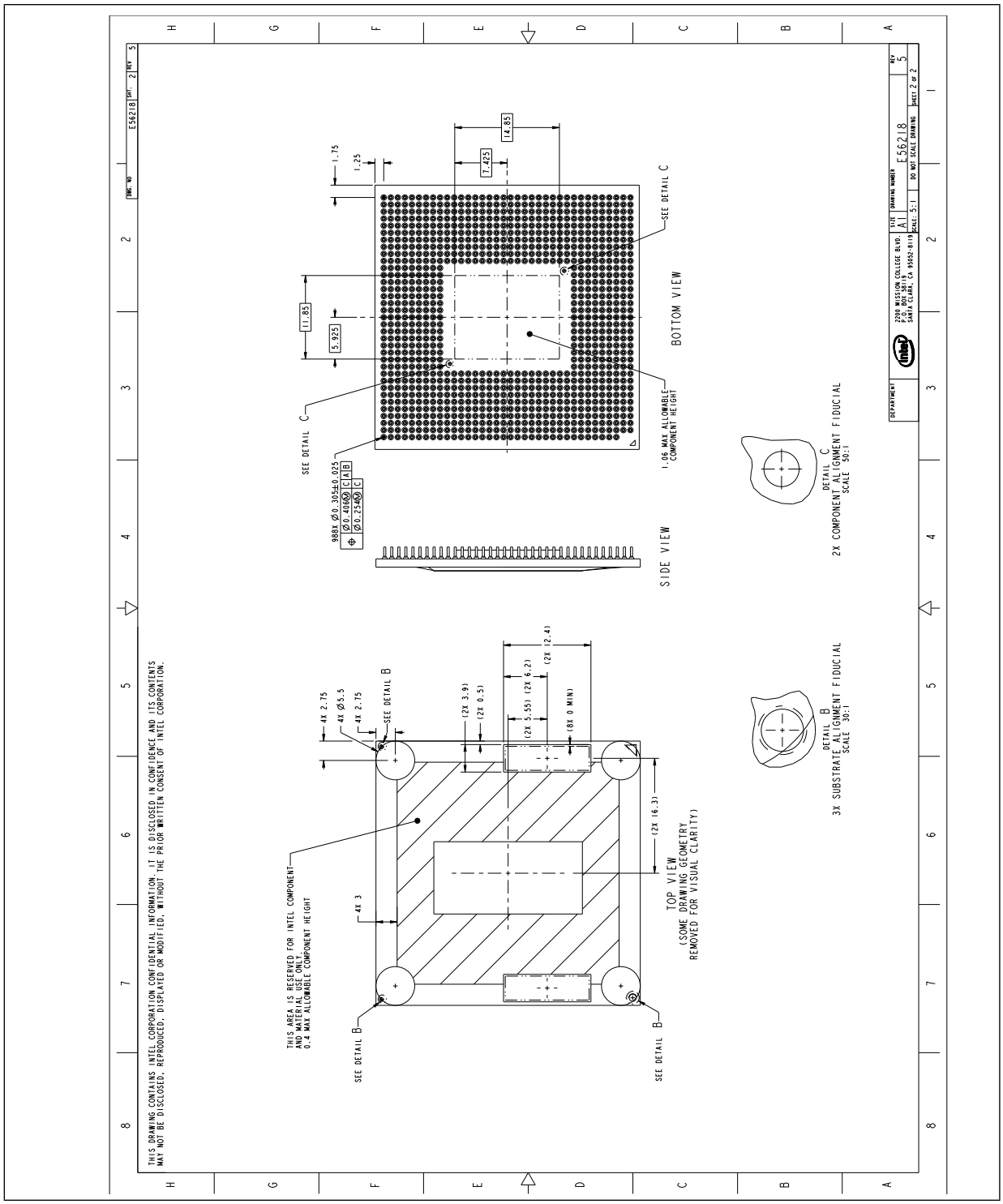
## Figure 11. 2nd Generation Intel® Core™ Processor Family Mobile rPGA988 2C Package Keep-Out Zones



## Figure 12. 2nd Generation Intel® Core™ Processor Family Mobile rPGA988 4C/2CF Package



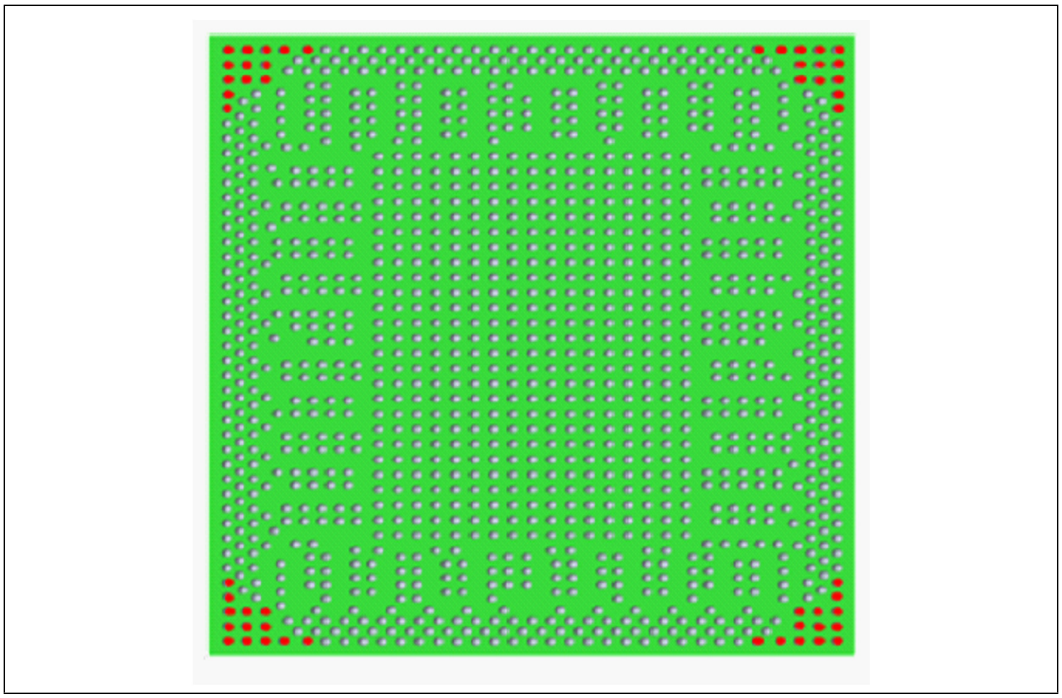
## Figure 13. 2nd Generation Intel® Core™ Processor Family Mobile rPGA988 4C/2CF Package Keep-Out Zones



## 2.1 Sacrificial Corner Balls

With the shift to lead-free solder, the higher reflow temperature (typically required by lead-free surface mount packages) and the increase in moisture content are both inherent in lead-free designs. These factors are expected to cause a decrease in the shock or vibration performance of Intel packages. Intel is using the concept of "sacrificial corner balls" (also referred to as non-critical to function, nCTF) to improve the solder joint reliability performance in shock and vibration where board bending occurs. Sacrificial corner balls are the corner-most lead-free solder balls included in Intel's BGA packages that are not used for any critical to function (CTF) signal routing. Corner solder balls are most susceptive to stress concentrations because of printed circuit board (PCB) layout shock, vibration, and bending. The concept of using sacrificial corner balls replaces "active" solder balls with mechanical solder balls which absorb maximum flexure stresses without negatively impacting electrical performance. Although using sacrificial corner balls provide about a 30 percent incremental shock margin, they are not a comprehensive platform solution; board flexure minimization techniques must still be considered. The corner-most solder balls provide a mechanical buffer to the CTF solder balls. Figure 14 shows an example of corner-most sacrificial solder balls on a BGA package.

**Figure 14. Example of Sacrificial Corner Balls**

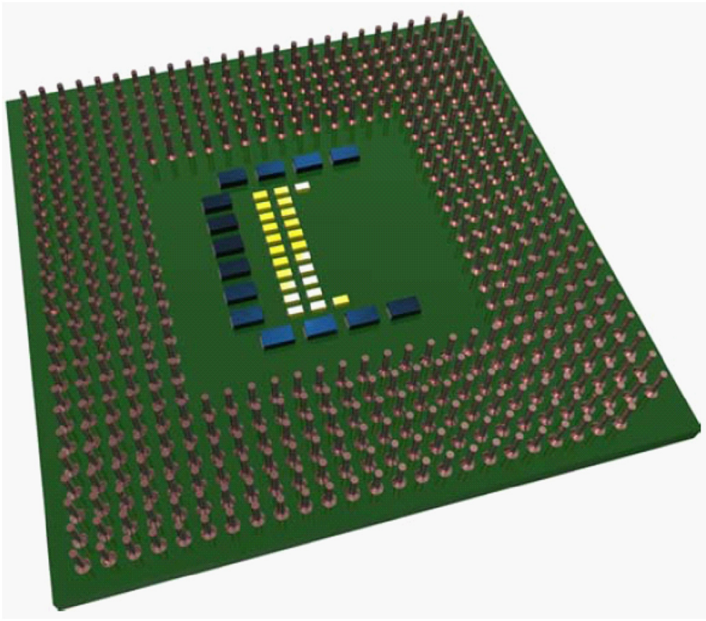


## 2.2 Land Side Capacitors (LSC)

A land side capacitor (LSC) is a device mounted on the back of a package. Refer to Figure 15 for an example of land side capacitors mounted on the back and at center of the pin side of a rPGA Package. Both rPGA988 and BGA1023 packages have LSC present. For the rPGA988 package, the maximum LSC height specification is 1.06mm.and side capacitors are only on the 2nd Generation Intel® Core™ Processor Family Mobile rPGA988 processor.

*Note:* For enabled loading of the BGA1023 package, there can be contact between the LSC and board. Board designs will need to keep this into consideration to prevent LSC shorting.

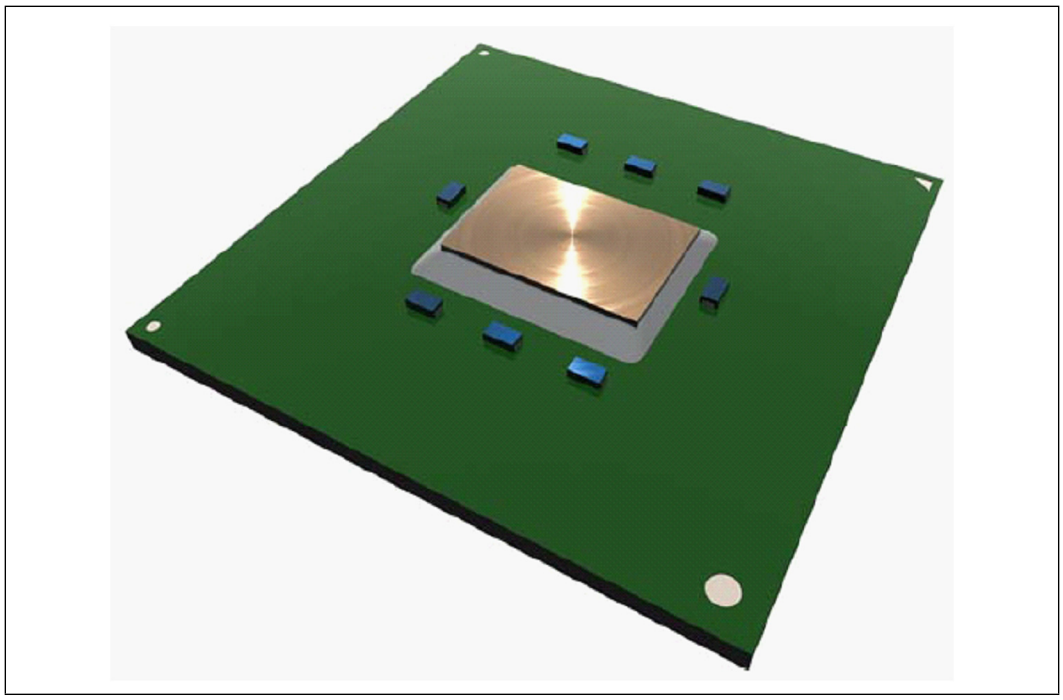
**Figure 15. Example of Land Side Capacitors Located on the Bottom of a PGA Package**



## 2.3 Die Side Capacitors (DSC)

A die side capacitor (DSC) is a device mounted on the top side of a package. Both rPGA988 and BGA1023 2nd Generation Intel® Core™ Processor Family Mobile have Die Side Capacitors. These capacitors have a maximum height specification of 0.40 mm for all of the packages from the top of the substrate of the package. See Figure 16 for an example of a capacitor mounted on the die side of a package.

**Figure 16. Example of Die Side Capacitors Located on the Die Side of a Package**



# 3.0 Thermal Management

The thermal solution provides both the component-level and the system-level thermal management. To allow for the optimal operation and long-term reliability of Intel processor-based systems, the system/processor thermal solution should be designed so that the processor:

- Remains below the maximum junction temperature ($T_{J\text{-}Max}$) specification at the maximum thermal design power (TDP).
- Conforms to system constraints, such as system acoustics, system skin-temperatures, and exhaust-temperature requirements.

***Caution:*** Thermal specifications in this chapter are on the component and package level and apply specifically to the Sandy Bridge processor. Operating the processor outside the specified limits may result in permanent damage to the processor and potentially other components in the system.

## 3.1 Thermal Design Power and Junction Temperatures

The processor Thermal Design Power (TDP) is the maximum sustained power that should be used for design of the processor thermal solution. TDP represents an expected maximum sustained power from realistic applications. TDP may be exceeded for short periods of time or if running a "power virus" workload. Due to Intel® Turbo Boost Technology, applications are expected to run closer to TDP more often as the processor attempts to take advantage of available headroom in the platform to maximize performance.

The processor may also exceed the TDP for short durations after a period of lower power operation due to its turbo feature. This feature is intended to take advantage of available thermal capacity in the thermal solution for momentary high power operation. The duration and time of such operation can be controlled to match the thermal response of the system by platform runtime configurable registers within the processor. Please see the *Sandy Bridge Turbo Implementation Guide* and *Sandy Bridge BIOS Writers Guide* for details.

The processor integrates multiple CPU and graphics cores on a single die. This may result in differences in the power distribution across the die and must be considered when designing the thermal solution. The thermal solution, at a minimum, needs to ensure that the junction temperatures of both CPU and graphics cores do not exceed the maximum junction temperature ($T_{J\text{-}Max}$) limit while running TDP applications. Thermal management considerations can be found in the processor datasheet.

The $T_{J\text{-}Max}$ and Thermal Design Power (TDP) specifications are listed in Table 2. The cooling capacity without a thermal solution is also minimal, so **Intel requires the use of a heatsink for all usage conditions**.

**Table 2. Thermal Specifications for 2nd Generation Intel® Core™ Processor Family Mobile**

| Segment | # of on Die Cores | # of Functional Cores | TDP [1,2,6] (W) | $T_{J-MAX}$ [3,4,5] (°C) | $T_{J-MIN}$ [3,4,5] (°C) |
|---|---|---|---|---|---|
| Standard Voltage | 4 | 4 | 45 | 100 | 0 |
| Standard Voltage | 4 | 2 | 35 | 100 | 0 |
| Standard Voltage | 2 | 2 | 35 | 100 | 0 |
| Low Voltage | 4 | 2 | 25 | 100 | 0 |
| Ultra Low Voltage | 4 | 2 | 17 | 100 | 0 |
| Ultra Low Voltage | 2 | 2 | 17 | 100 | 0 |
| Ultra Low Voltage | 2 | 1 | 17 | 100 | 0 |

***Notes:***
1. The component TDPs given are not the maximum power the components can generate. Analysis indicates that real applications are unlikely to cause the processor to consume the theoretical maximum power dissipation for sustained periods of time.
2. TDP workload may consist of a combination of a CPU-core intensive and a graphics-core intensive applications.
3. The thermal solution needs to ensure that the processor temperature does not exceed the maximum junction temperature (TJ-Max) limit, as measured by the DTS and the critical temperature bit.
4. The processor junction temperature is monitored by Digital Temperature Sensors (DTS). For DTS accuracy please refer to the 2nd Generation Intel® Core™ Processor Family Mobile *Datasheet.*
5. Digital Thermal Sensor (DTS) based fan speed control is required to achieve optimal thermal performance. Intel recommends full cooling capability well before the DTS reading reaches TJ-Max. An example of this would be Tj,Max - 10ºC.
6. At Tj of TJ-Max

### 3.1.1 Turbo Considerations

Intel® Turbo Boost Technology allows processor cores and integrated graphics cores to run faster than the baseline frequency. During a turbo event the processor can consume close to its maximum thermal power limit for sustained period. More importantly, processor thermal power can also briefly exceed its TDP power level. Turbo is invoked opportunistically and automatically as long as the processor is conforming to its temperature, power delivery, and current specification limits. Thus, thermal solutions and platform cooling that are designed to less than thermal design guidance might experience thermal and performance issues since more applications will tend to run at or near the maximum power limit for significant periods of time. Please see the *Sandy Bridge Turbo Implementation Guide* and *Sandy Bridge BIOS Writers' Guide.*

### 3.1.2 Platform Environment Control Interface (PECI)

The Platform Environment Control Interface (PECI) is a one-wire interface that provides a communication channel between the Intel processor and chipset components to external monitoring devices. The processor uses a PECI interface for communication of processor thermal information to other devices on the platform. The processor provides a digital thermal sensor (DTS) for fan speed control. The DTS is calibrated at the factory to provide a digital representation of relative processor temperature. Averaged DTS values are read via the PECI interface.

The PECI physical layer is a self-clocked one-wire bus that begins each bit with a driven, rising edge from an idle level near zero volts. The duration of the signal driven high depends on whether the bit value is a Logic 0 or Logic 1. PECI also includes the variable data transfer rate established with every message. The single wire interface provides low board routing overhead for the multiple load connections in the congested

routing area near the processor and chipset components. Bus speed, error checking, and low protocol overhead provides adequate link bandwidth and reliability to transfer critical device operating conditions and configuration information.

#### 3.1.2.1 Fan Speed Control with Digital Thermal Sensor

Digital Thermal Sensor (DTS) based fan speed control is a recommended feature to achieve optimal thermal performance. As the temperature of the processor increases, a controller can read the DTS and then increase the speed of the thermal solution fan accordingly. The temperature at which the fan is programmed to run at maximum speed is called "TFAN". Intel recommends reaching full fan speed well before the DTS reading reaches $T_{J\text{-}Max}$. An example of this would be $T_{FAN} = T_{J\text{-}Max} - 10^{o}C$.

# 4.0 Mechanical Specifications

This section includes specifications, package attributes, and mechanical drawings of the mobile 2nd Generation Intel® Core™ Processor Family Mobile. Also highlighted are key mechanical dimensions compatible with the reduced pitch pin grid array (rPGA989/988) socket to the corresponding family of CPU packages. These drawings can be used to determine printed circuit board (PCB) keep-out zones, the placement of discrete electronics and to gauge contact area and stack-up tolerances for thermal solution design.

## 4.1 Package Mechanical Requirements

### 4.1.1 Die Pressure (Load Upper/Lower Limit)

From a die mechanical integrity standpoint, the maximum allowable normal die load is the lower of 15 lbs or 100 psi. For example, considering the 15 lbs load limit and the nominal die area of 1.45 $cm^2$ (0.22 $in^2$), this equates to a die pressure of 66.7 psi (below 100 psi specification). Considering the maximum pressure specification, the die load at this pressure would be 22.4 lbs, exceeding the 15 lbs. load limit. Thus, the heatsink clamping mechanism (spring loaded fasteners, spring clips, etc.) should not exceed 15 lbs specification.

From a Thermal Interface Material (TIM) performance standpoint, a minimum die pressure is required to ensure consistent and minimal TIM thermal resistance. This lower value is a function of the TIM used.

## 4.2 Package Keep-Out Zones Requirements

The heatsink must not touch the package in the areas shown in Figure 7 and Figure 9. The heatsink should include a means to prevent the heatsink from forming an electrical short with the capacitors placed on the top side of the package. Reference thermal solutions could include machined z-stops into the base of the heatsink to prevent such an occurrence. The z-stops prevent the heatsink from inadvertently tilting when installed. Other methods are suitable including using electrically insulated gasket material at the base of the heatsink.

## 4.3 Board Level Keep-Out Zone Requirements

A general description of the keep-out zones and mounting hole pattern for the reference thermal solutions are shown in Figure 17 and Figure 18 for the rPGA988 and BGA1023 packages. Detailed drawings for the PCB keep out zones for Mini-ITX and CompactPCI* form factors are in Appendix B, “Mechanical Drawings”.

Components placed between the underside of the heatsink and motherboard cannot exceed 4.25 mm in height when using heatsinks that extend beyond the rPGA 988/989 socket envelope for the micro-FCPGA package.

**Figure 17. 2nd Generation Intel® Core™ Processor Family Mobile BGA Board Keep-Out Zones**

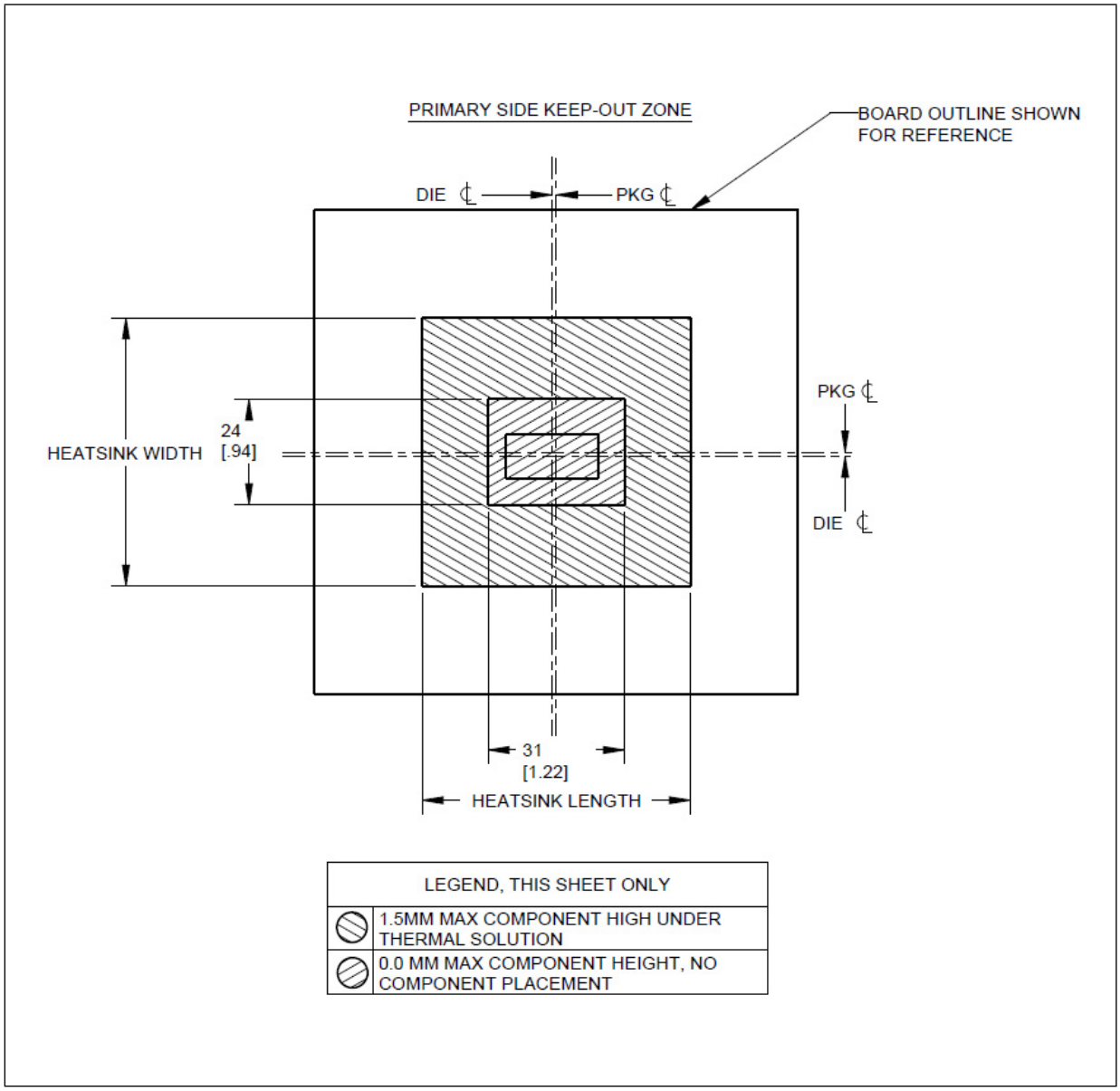
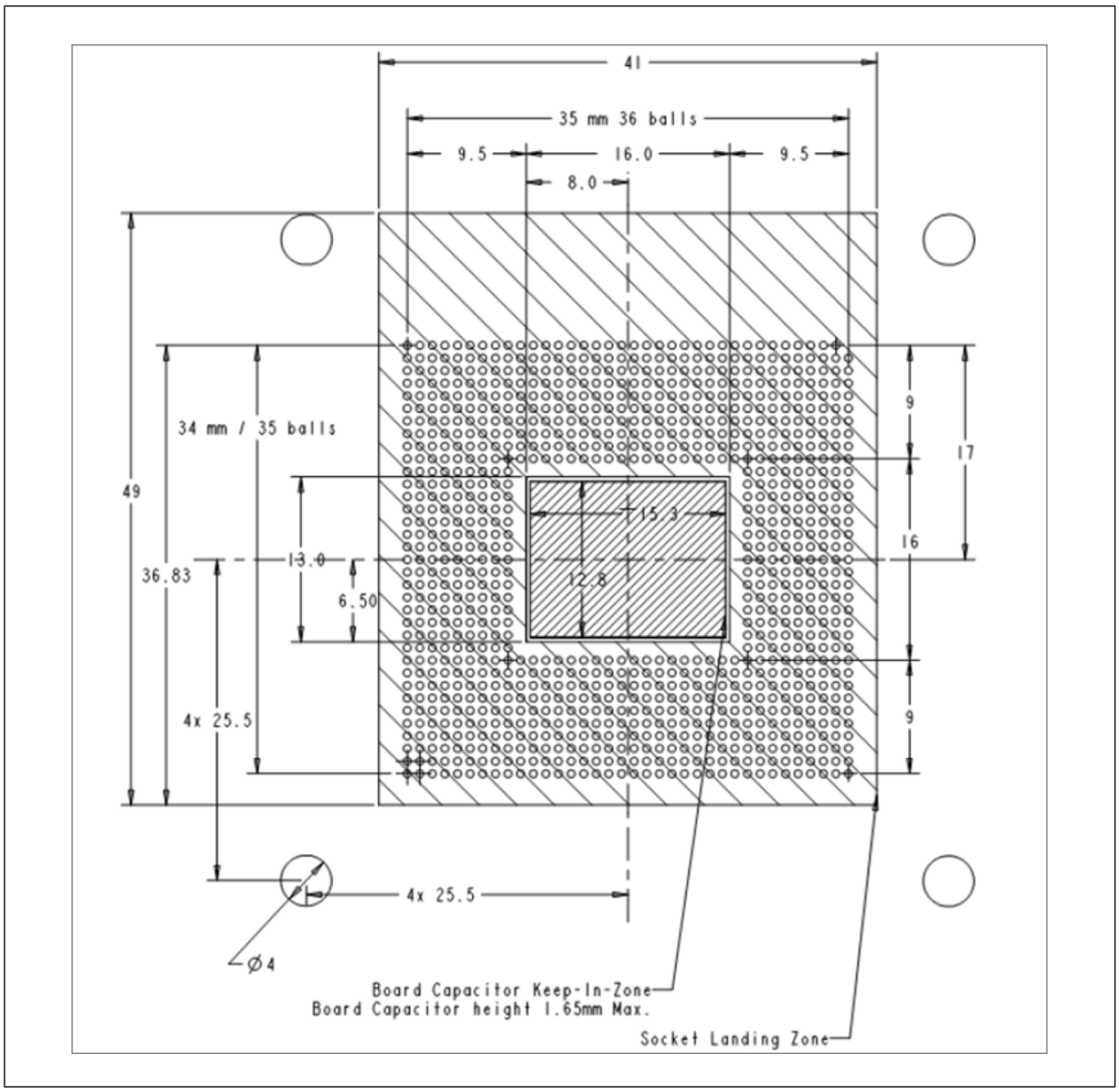


**Figure 18. 2nd Generation Intel® Core™ Processor Family Mobile rPGA Board Keep-Out Zones**



# 5.0 Thermal Solution Requirements

## 5.1 Thermal Solution Characterization

The thermal characterization parameter, $\Psi$ ("psi"), is used to characterize thermal solution performance, as well as compare thermal solutions in identical situations (i.e., heating source, local ambient conditions, etc.). It is defined by the following equation:

**Equation 1. Junction-to-Local Ambient Thermal Characterization Parameter ($\Psi_{JA}$)**

$$\Psi_{JA} = \frac{T_{J-MAX} - T_A}{TDP}$$

where,

$\Psi_{JA}$ = Junction-to-local ambient thermal characterization parameter (°C/W)

$T_{J\text{-}Max}$ = Maximum allowed device temperature (°C)

$T_A$ = Local ambient temperature near the device (°C) (see Section 7.0 for measurement guidelines)

TDP = Thermal Design Power (W) at the socket level

The thermal characterization parameter assumes that all package power dissipation is through the thermal solution (heatsink), and is equal to TDP. A small percentage of the die power (< 5%) is dissipated through the package/socket/motherboard stack to the environment, and should not be considered as a means of thermal control.

The junction-to-local ambient thermal characterization parameter, $\Psi_{JA}$, is comprised of $\Psi_{JS}$, which includes the thermal interface material thermal characterization parameter, and of $\Psi_{SA}$, the sink-to-local ambient thermal characterization parameter:

**Equation 2. Junction-to-Local Ambient Thermal Characterization Parameter**

$$\Psi_{JA} = \Psi_{JS} + \Psi_{SA}$$

Where:

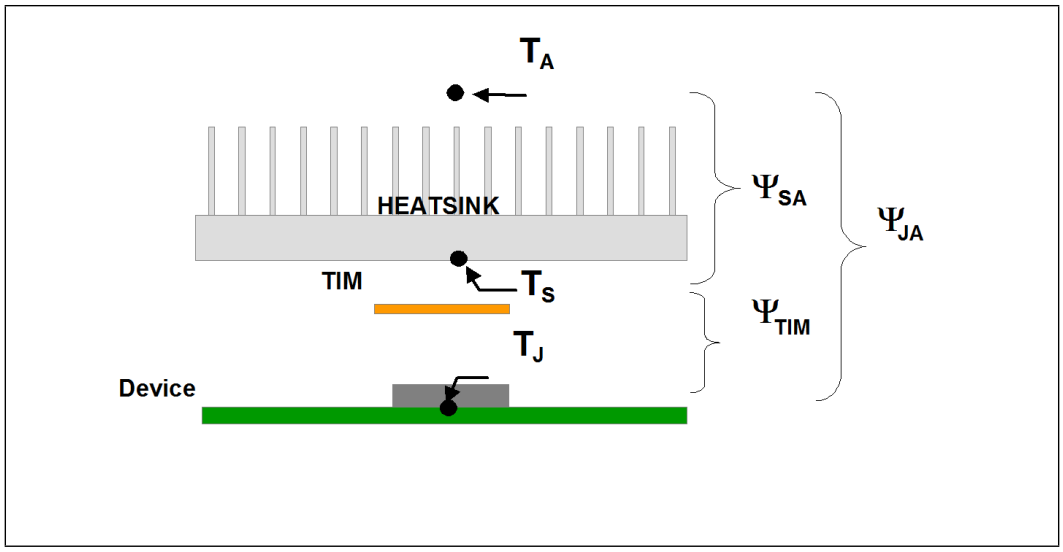
$\Psi_{JS}$ = Thermal characterization parameter from junction-to-sink, this also includes thermal resistance of the thermal interface material ($\Psi_{TIM}$) (°C/W).

$\Psi_{SA}$ = Thermal characterization parameter from sink-to-local ambient (°C/W)

$\Psi_{SA}$ is a measure of the thermal characterization parameter from the bottom of the heatsink to the local ambient air. $\Psi_{SA}$ is dependent on the heatsink material, thermal conductivity, and geometry. It is also strongly dependent on the air velocity through

the fins of the heatsink. Figure 19 illustrates the combination of the different thermal characterization parameters.

**Figure 19. Processor Thermal Characterization Parameter Relationships**




### 5.1.1 Calculating the Required Thermal Performance for the 2nd Generation Intel® Core™ Processor Family Mobile

Overall thermal performance, $\Psi_{JA,}$ is then defined using the thermal characterization parameter:

- Define a target component temperature $T_{JUNCTION}$ and corresponding TDP.
- Define a target local ambient temperature, $T_A$.

The following provides an illustration of how to determine the appropriate performance targets.

Assume:

- TDP = 35W and $T_{JUNCTION}$ = 100° C
- Local processor ambient temperature, $T_A$ = 55° C.

Using Equation 1, the maximum allowable resistance, junction-to-ambient, is calculated as:

**Equation 3. Maximum Allowable Resistance**

$$\Psi_{JA} = \frac{T_{J-MAX} - T_A}{TDP} = \frac{100 - 55}{35} = 1.29 \frac{^oC}{W}$$

To determine the required heatsink performance, a heatsink solution provider would need to determine $\Psi_{JA}$ performance for the selected TIM and mechanical load configuration. If the heatsink solution were designed to work with a TIM material performing at $\Psi_{TIM} \leq$ 0.3°C/W, solving from Equation 2, the performance of the heatsink required is:

**Equation 4. Required Performance of the Heatsink**

$$\Psi_{SA} = \Psi_{JA} - \Psi_{JS} = 1.29 - 0.30 = 0.99 \frac{^{\circ}C}{W}$$

It is evident from the above calculations that a reduction in the local ambient temperature can have a significant effect on the junction-to-ambient thermal resistance requirement. This effect can contribute to a more reasonable thermal solution including reduced cost, heatsink size, heatsink weight, or a lower system airflow rate.

# 6.0 Reference Thermal Solutions

Intel has developed reference thermal solutions designed to meet the cooling needs of embedded form factor applications. This chapter describes the overall requirements for the reference thermal solution including critical-to-function dimensions, operating environment, and verification criteria. This document details solutions that are compatible with Mini-ITX and CompactPCI* form factors.

The data in this section is based on test data of the reference thermal solutions. The mini-ITX* heatsink was tested as an assembly with a thermal test vehicle (TTV), thermal interface material, socket and test board. For the passive CompactPCI* thermal solution, test assemblies are placed in a rectangular duct connected to a wind tunnel with no upstream obstructions. Air flow is measured by means of a calibrated nozzle downstream of the unit under test. The thermal performance values shown in the charts to follow represent the mean resistance values plus the one-sided, 99% confidence interval.

## 6.1 Performance Targets

Table 3 provides boundary conditions and performance targets for Mini-ITX* and CompactPCI* form factors. These values are used to generate processor thermal specifications and to provide guidance for heatsink design.

**Table 3. Boundary Conditions and Performance Targets for 2nd Generation Intel® Core™ Processor Family Mobile**

| | Form Factor | |
|---|---|---|
| **Parameter** | **Mini-ITX** | **CompactPCI*** |
| Altitude, system ambient Temp Nominal/ Short-term[1] | Sea level, 40° C | Sea level, 40° C/55°C |
| Enabled TDP[2] | 45, 35, 25, 17W | 35, 25, 17W |
| $\Psi_{JA}$[3] | (1.33/1.71/2.40/3.52)°C/W | (1.29/1.8/2.65) °C/W |
| Heatsink volumetric | (60 x 60 x 27) mm | (90 x 60 x 11.6) mm |
| Heatsink Technology[4] | Al Fins/ Al Base | Cu Fins/ Cu Base |

***Notes:***
1. Ambient temperature of the air entering the system.
2. Refers to the TDP skus that can be cooled in each embedded form factors.
3. Represents the $\Psi_{JA}$ max for each sku based on the thermal specifications outlined in Table 2 and an local ambient of 55°C.
4. Mini-ITX and CompactPCI* are active fan and passive thermal solution respectively.

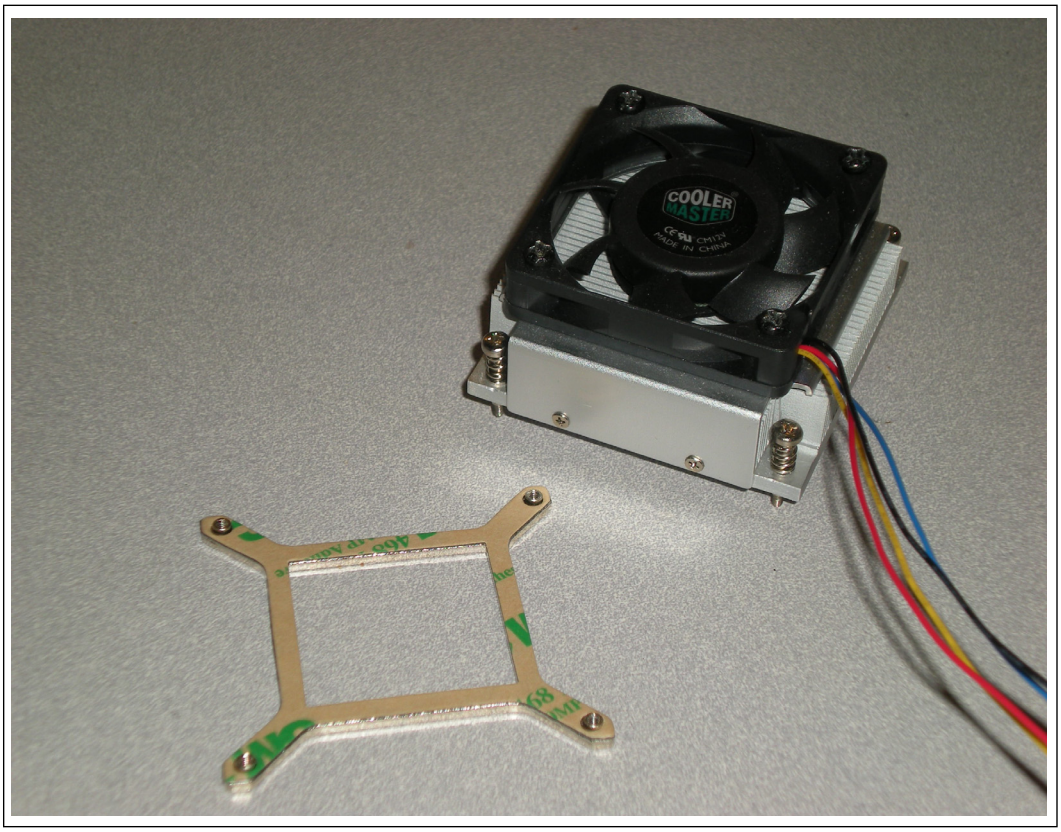
## 6.2 Mini-ITX* Reference Heatsink

This reference active heatsink is compatible with the Mini-ITX* and larger form factors. The thermal performance shown in Table 4 is at full fan speed and 12 V is supplied to the fan. The equations shown in Section 5.1.1 can be used to determine the acceptable ambient temperature range in which this heatsink can be used.

### 6.2.1 Mechanical Design

The reference heatsink is shown in the figure below. The reference solution is an aluminum skived finned active fan solution with overall dimension of 60mm x 60mm x. The maximum heatsink height was constrained so that the total package height plus heatsink will not exceed maximum component height for the Mini-ITX* Form Factor. The heatsink uses spring fasteners and a backplate assembly (refer to Section 6.7) to mount to the PCB. Detailed drawings of this heatsink are provided in Appendix B.

**Figure 20. Mini-ITX Reference Heatsink**




### 6.2.2 Keep-Out Zone Requirements

The keep-out zone requirements on the PCB to use the enabled reference heatsinks are detailed in Appendix B, "Mechanical Drawings" for CompactPCI* because it extends beyond the footprint of the device, it is critical for the board designer to allocate space on the board for the heatsink foot print.

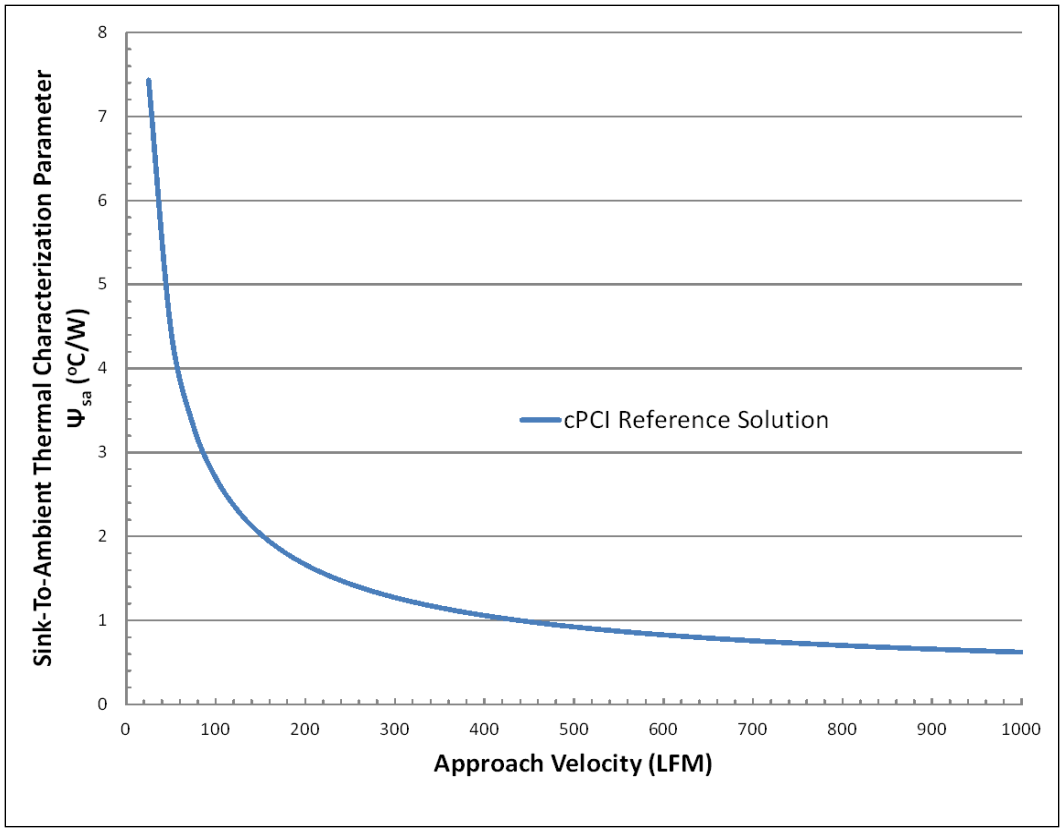
### 6.2.3 Thermal Performance

The performance of the heatsink is shown below. Based on the target boundary conditions, this heatsink can meet the thermal performance needed to cool the processor in the Mini-ITX form factor. However, it is up to the system designer to validate the entire thermal solution (heatsink, attach method, TIM) in its final intended system. The performance data is based on lab verification testing.

## 6.3 CompactPCI* Reference Thermal Solutions

This reference heatsink is compatible with CompactPCI* form factor and other small embedded blade form factor. Figure 21 outlines the heatsink thermal performance at various airflow rates. The equations shown in Section 5.1 can be used to determine the acceptable ambient temperature range at which this heatsink can be used based on available airflow.

**Figure 21. CompactPCI* Reference Heatsink Thermal Performance vs. Approach Velocity**




## 6.4 Keep-Out Zone Requirements

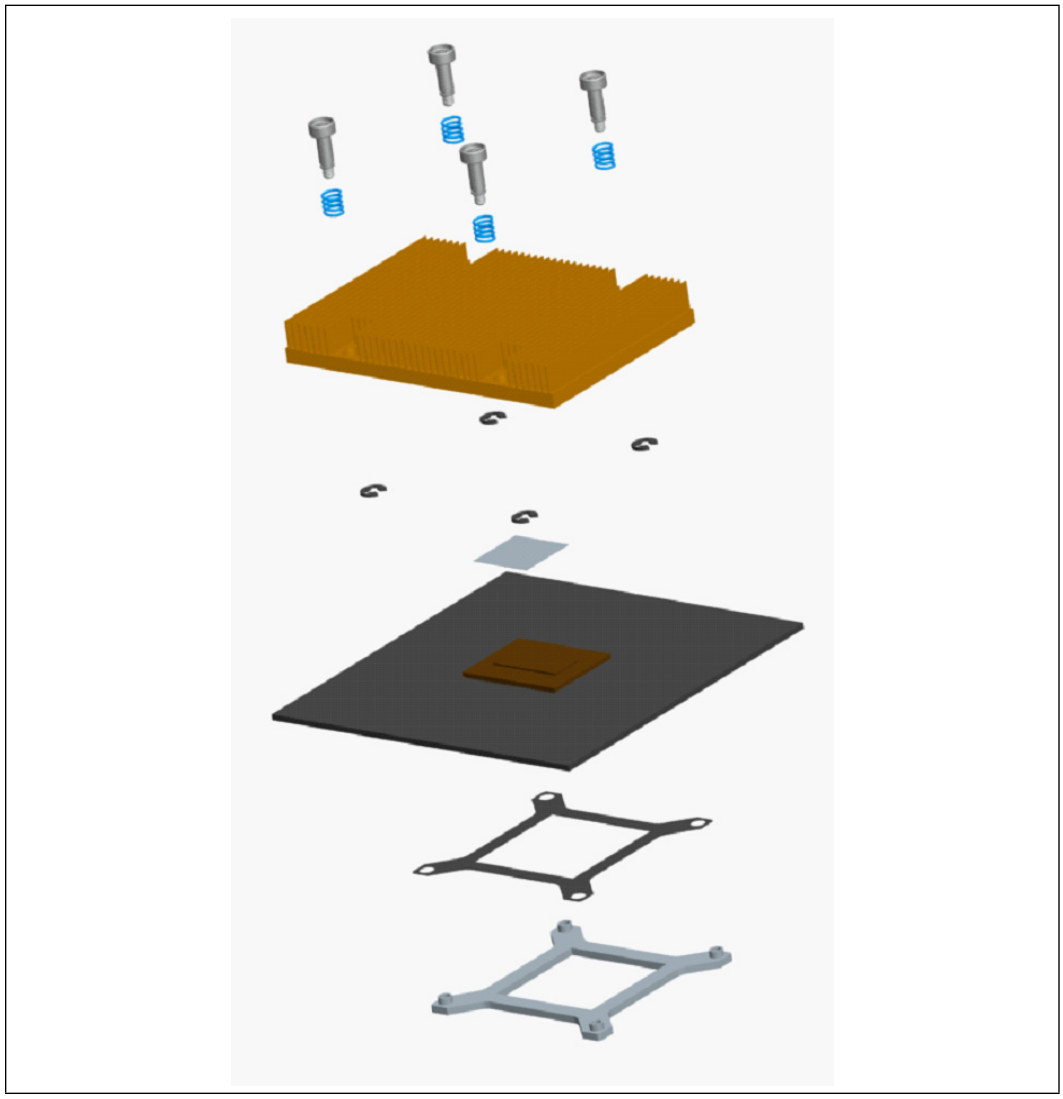
The keep-out zone requirements on the PCB to use the enabled reference heatsinks are detailed in Appendix B, "Mechanical Drawings" for CompactPCI* because it extends beyond the footprint of the device, it is critical for the board designer to allocate space on the board for the heatsink foot print.

## 6.5 Heatsink Fastener Assembly

The reference solutions use a screw, spring, and back plate assembly to attach the heatsink to the PCB as shown in Figure 22 for the CompactPCI* reference heat sink. The fastener assembly used on the reference heatsink must apply the load conditions

described in Section 4.0. The fastener assembly must comply with all of the keep out zone requirements described in this document, and should not degrade the thermal performance of the reference heatsinks.

**Figure 22. CompactPCI* Reference Heatsink Assembly**



## 6.6 Thermal Interface Material (TIM)

The thermal interface material provides improved conductivity between the die and heatsink. It is important to understand and consider the impact of the interface between the die and heatsink base to the overall thermal solution. Specifically, the bond line thickness, interface material area, and interface material thermal conductivity must be selected to optimize the thermal solution.

It is important to minimize the thickness of the thermal interface material (TIM), commonly referred to as the bond line thickness. A large gap between the heatsink base and the die yields a greater thermal resistance. The thickness of the gap is determined by the flatness of both the heatsink base and the die, plus the thickness of

the thermal interface material, and the clamping force applied by the heatsink attachment method. To ensure proper and consistent thermal performance, the TIM and application process must be properly designed.

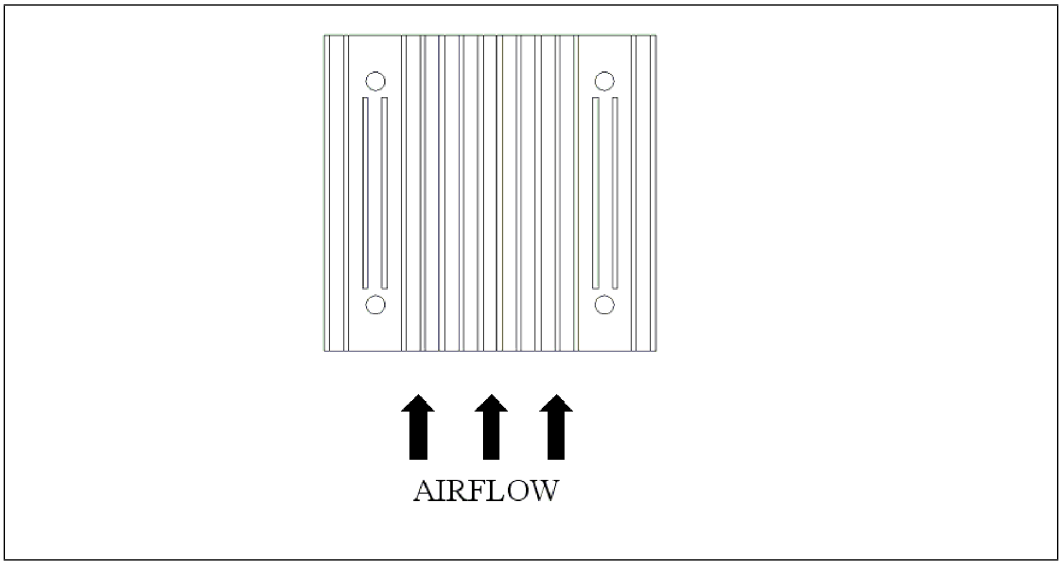
Thermal interface materials have thermal impedance (resistance) that will increase over time as the material degrades. It is important for thermal solution designers to take this increase in impedance into consideration when designing a thermal solution. It is recommended that system integrators work with TIM suppliers to determine the performance of the desired thermal interface material. If system integrators wish to maintain maximum thermal solution performance, the TIM could be replaced during standard maintenance cycles.

Some of the Thermal Interface materials that Intel recommends are Shin-Etsu* PCS-LT-30, Honeywell* PCM45F, and Chromerics* T777 phase change material. Alternative materials can be used at the user's discretion. Regardless, the entire heatsink assembly, including the heatsink, and TIM (including attach method), must be validated together for specific applications.

## 6.7 Heatsink Orientation

All of the heatsinks were designed to maximize the available space within the volumetric keep out zone and their respective form factor limitations. These heatsinks must be oriented in a specific direction relative to the processor keep-out zone and airflow. In order to use these designs, the processor must be placed on the PCB in an orientation so the heatsink fins will be parallel to the airflow. Figure 23 illustrates this orientation.

**Figure 23. Heatsink Orientation Relative to Airflow Direction**



# 7.0 Thermal Metrology

The system designer must make temperature measurements to accurately determine the performance of the thermal solution. Validation of the processor's thermal solution should be done using a thermal test vehicle (TTV). The TTV allows for an accurate junction temperature measurement as well as input power control. For more information, contact your Intel field sales representative.

In addition, the processors heatsink should be verified in a system environment. Intel has established guidelines for techniques to measure the component temperature. Section 7.1 and Section 7.2 provide guidelines on how to accurately measure the component temperature and information on running an application program that will emulate anticipated maximum thermal design power.

## 7.1 Die Temperature Measurements

The component $T_{JUNCTION}$ must be maintained at or below the maximum temperature specification as noted in Table 2. The best way to measure die temperature is to use the Digital Thermal Sensor as described in the 2nd Generation Intel® Core™ Processor Family Mobile *External Design Specification*. Refer to the processor datasheet for more information on the DTS.

## 7.2 Power Simulation Software

The power simulation software called Thermal Analysis Tool "TAT" is a utility designed to dissipate the thermal design power on a processor. To assess the thermal performance of the processor thermal solution under "worst-case realistic application" conditions, Intel is developing a software utility that operates the processor at near worst-case power dissipation.

The power simulation software should only be used to test customer thermal solutions at or near the thermal design power. For power supply current, please refer to each component's datasheet for the $I_{CC}$ (Max Power Supply Current) specification. For information on how to obtain the Thermal Analysis program, contact your Intel field sales representative

## 7.3 Additional Thermal Features

The 2nd Generation Intel® Core™ Processor Family Mobile supports other thermal features including the Intel® Thermal Monitor, PROCHOT# and THERMTRIP# signal pins. Details for using these features are contained in the processor datasheet.

## 7.4 Local Ambient Temperature Measurement Guidelines

The local ambient temperature ($T_{LA}$) is the temperature of the ambient air surrounding the processor.  For a passive heatsink, $T_A$ is defined as the heatsink approach air temperature; for an actively cooled heatsink, it is the temperature of inlet air to the active cooling fan.

It is worthwhile to determine the local ambient temperature in the chassis around the processor to understand the effect it may have on the case temperature. $T_{LA}$ is best measured by averaging temperature measurements at multiple locations in the heatsink inlet airflow. This method helps reduce error and eliminate minor spatial variations in temperature. The following guidelines are meant to enable accurate determination of the localized air temperature around the processor during system thermal testing.

### 7.4.1 Active Heatsink Measurements

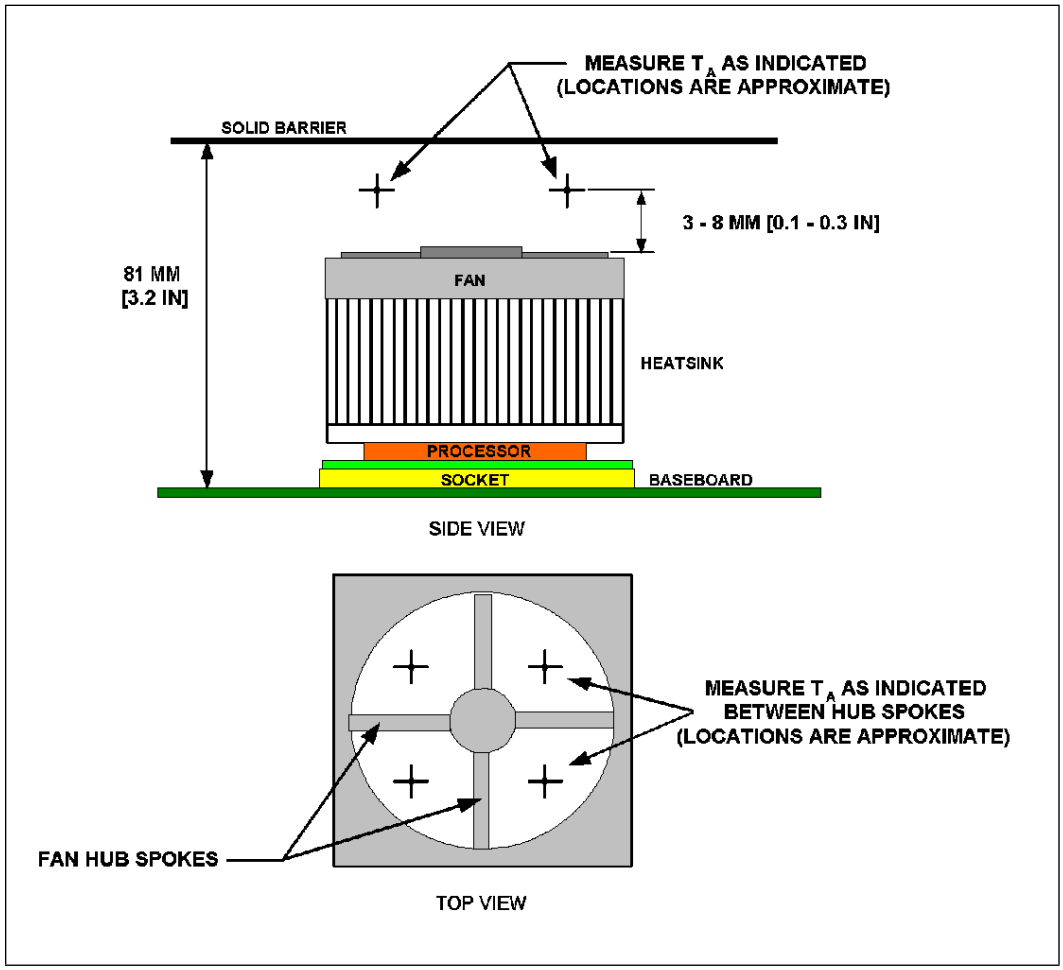
- It is important to avoid taking measurements in the dead flow zone that usually develops above the fan hub and hub spokes. Measurements should be taken at four different locations uniformly placed at the center of the annulus formed by the fan hub and the fan housing to evaluate the uniformity of the air temperature at the fan inlet. The thermocouples should be placed approximately 3 mm to 8 mm [0.1 to 0.3 in] above the fan hub vertically and halfway between the fan hub and the fan housing horizontally as shown in Figure 24 (avoiding the hub spokes).
- Using an open bench to characterize an active heatsink can be useful, and usually ensures more uniform temperatures at the fan inlet. However, additional tests that include a solid barrier above the test motherboard surface can help evaluate the potential impact of the chassis. This barrier is typically clear Plexiglas*, extending at least 100 mm [4 in.] in all directions beyond the edge of the thermal solution. Typical distance from the motherboard to the barrier is 81 mm [3.2 in.]. If a barrier is used, the thermocouple can be taped directly to the barrier with clear tape at the horizontal location as previously described, halfway between the fan hub and the fan housing.
- For even more realistic airflow, the motherboard should be populated with significant elements like memory cards, graphic card, and chipset heatsink. If a variable speed fan is used, it may be useful to add a thermocouple taped to the barrier above the location of the temperature sensor used by the fan to check its speed setting against air temperature. When measuring $T_{LA}$ in a chassis with a live motherboard, add-in cards, and other system components, it is likely that the $T_{LA}$ measurements will reveal a highly non-uniform temperature distribution across the inlet fan section.

*Note:* Testing an active heatsink with a variable speed fan can be done in a thermal chamber to capture the worst-case thermal environment scenarios. Otherwise, when doing a bench top test at room temperature, the fan regulation prevents the heatsink from operating at its maximum capability. To characterize the heatsink capability in the worst-case environment in these conditions, it is then necessary to disable the fan regulation and power the fan directly, based on guidance from the fan supplier.

### 7.4.2 Passive Heatsink Measurements

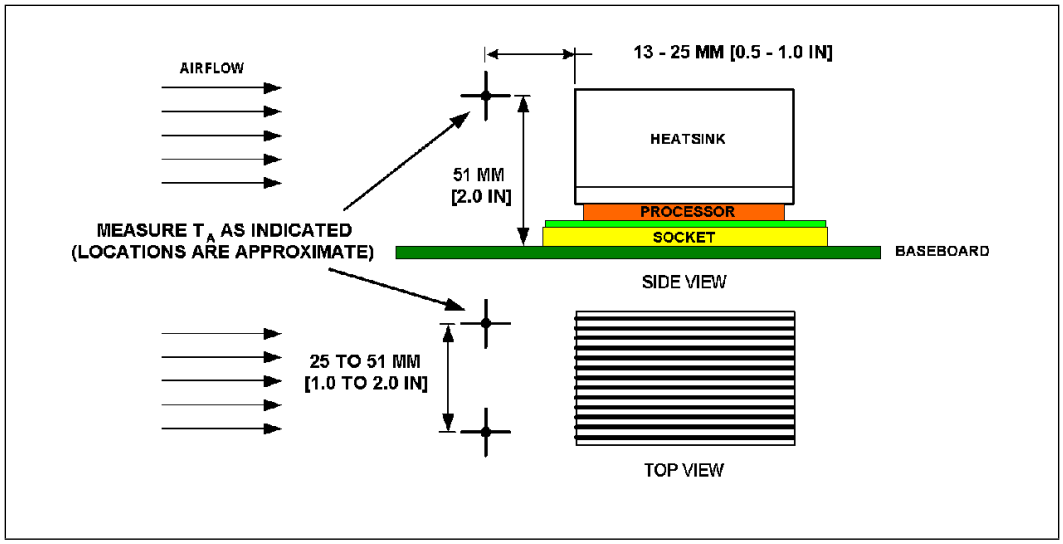
- Thermocouples should be placed approximately 13 mm to 25 mm [0.5 to 1.0 in] away from processor and heatsink as shown in Figure 25.
- The thermocouples should be placed approximately 51 mm [2.0 in] above the baseboard. This placement guideline is meant to minimize the effect of localized hot spots from baseboard components. The height above the board may vary depending on the height of the thermal solution and form factor.

**Figure 24. Measuring $T_{LA}$ with an Active Heatsink**




*Note:* Drawing not to scale.

**Figure 25. Measuring $T_{LA}$ with a Passive Heatsink**




*Note:* Drawing not to scale.

# Appendix A Thermal Solution Component Suppliers

These vendors and devices are listed by Intel as a convenience to Intel's general customer base. Intel does not make any representations or warranties whatsoever regarding quality, reliability, functionality, or compatibility of these devices. This list and/or these devices may be subject to change without notice.

*Note:* The enabled components may not be currently available from all suppliers. Contact the supplier directly to verify availability.

**Table 4. Suppliers**

| Part | Intel Part Numbers | Supplier Part Number | Supplier Contact Information |
|---|---|---|---|
| Mini-ITX Heatsink Assembly | G32223-001 | CHE-00032-01-GP | Cooler Master USA, Inc.<br>Chester Liao<br>chester_liao@coolermaster.com<br>(510) 770-8566 x212 |
| CompactPCI* Assembly | G32222-001 | 1A01PS100 | Foxconn/FTC Technology, Inc.<br>Cary Huang<br>cary.huang@foxconn.com<br>(512) 670-2638 x191 |
| Thermal Interface Material | N/A | PCS-LT-30 | Shin-Etsu MicroSi<br>Randy Isaacson<br>RIsaacson@MicroSi.com<br>(480) 584-3887 |
| Thermal Interface Material | N/A | PCM45F | Honeywell<br>Judy Oles<br>Judy.Oles@Honeywell.com<br>(509)252-8605 |

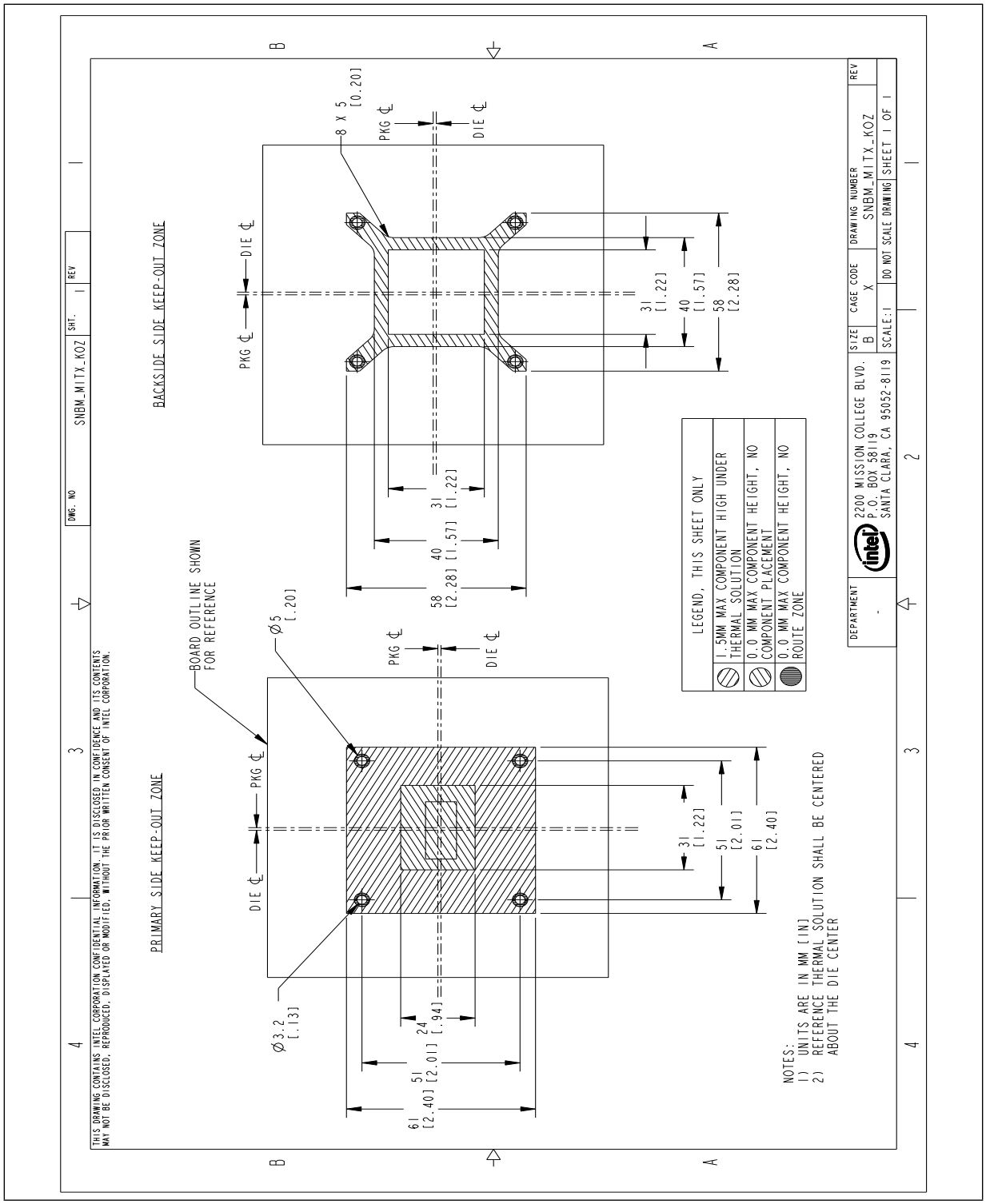
# Appendix B Mechanical Drawings

The table below lists the mechanical drawings included in this appendix.

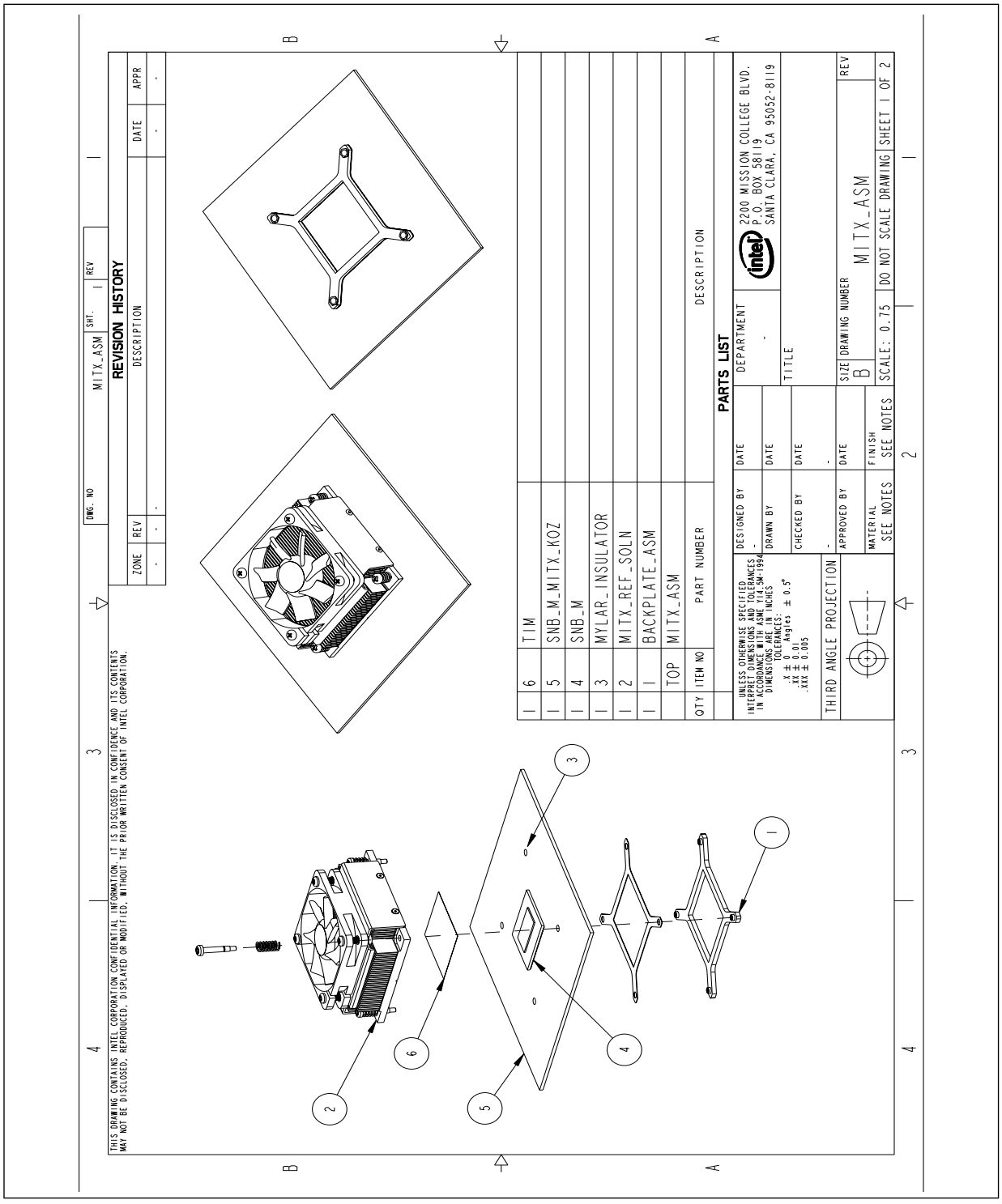
**Table 5. Mechanical Drawings**

| Description | Figure |
|---|---|
| Mini-ITX* Reference Heatsink PCB Keep Out Zone Requirements | Figure 26 |
| Mini-ITX* Reference Heatsink Assembly (Sheet 1 of 2) | Figure 27 |
| Mini-ITX* Reference Heatsink Assembly (Sheet 2 of 2) | Figure 28 |
| cPCI* Reference Heatsink PCB Keep Out Zone Requirements | Figure 29 |
| cPCI* Reference Heatsink Assembly (Sheet 1 of 2) | Figure 30 |
| cPCI* Reference Heatsink Assembly (Sheet 2 of 2) | Figure 31 |
| cPCI* Reference Heatsink | Figure 32 |

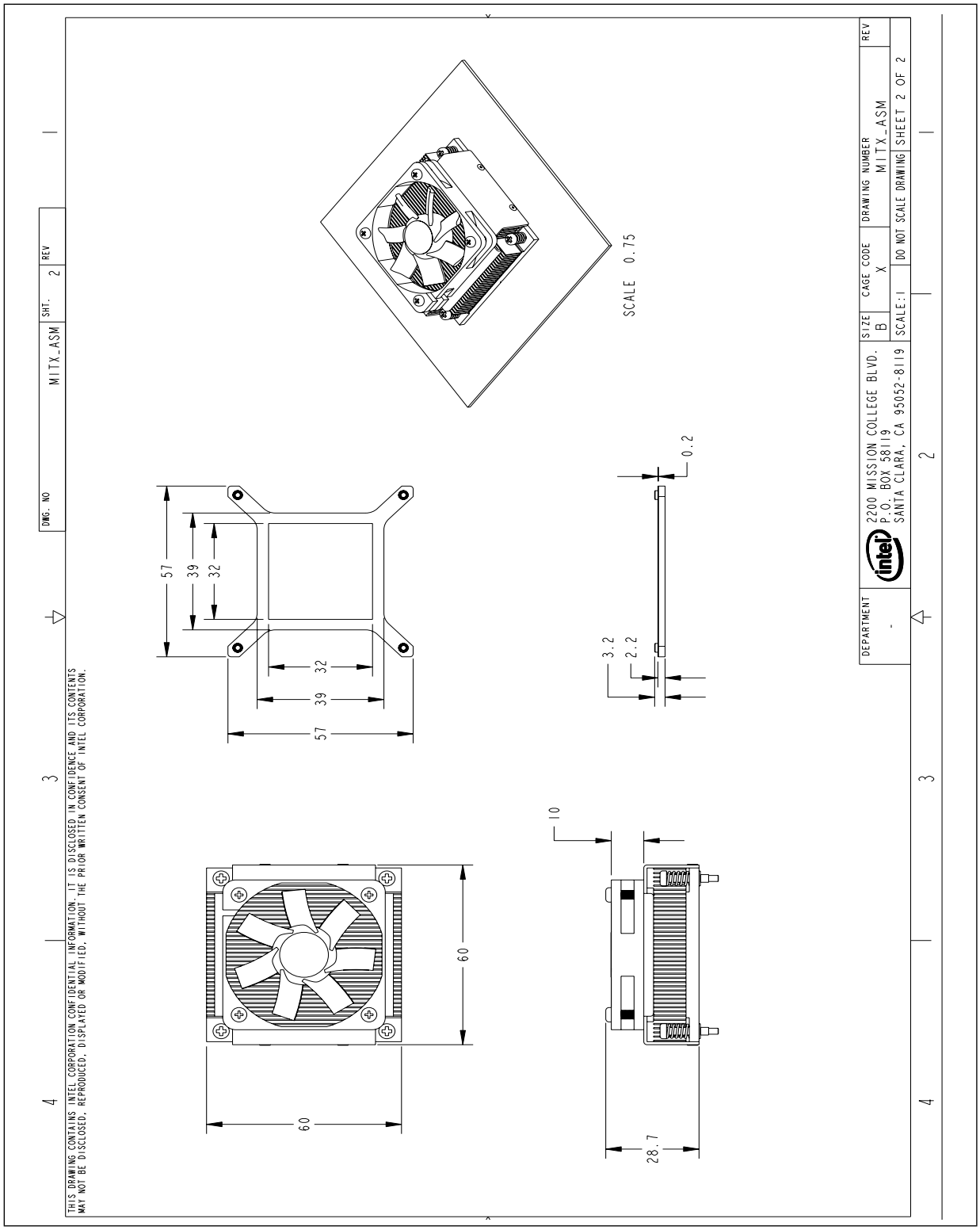
## Figure 26. Mini-ITX* Reference Heatsink PCB Keep Out Zone Requirements



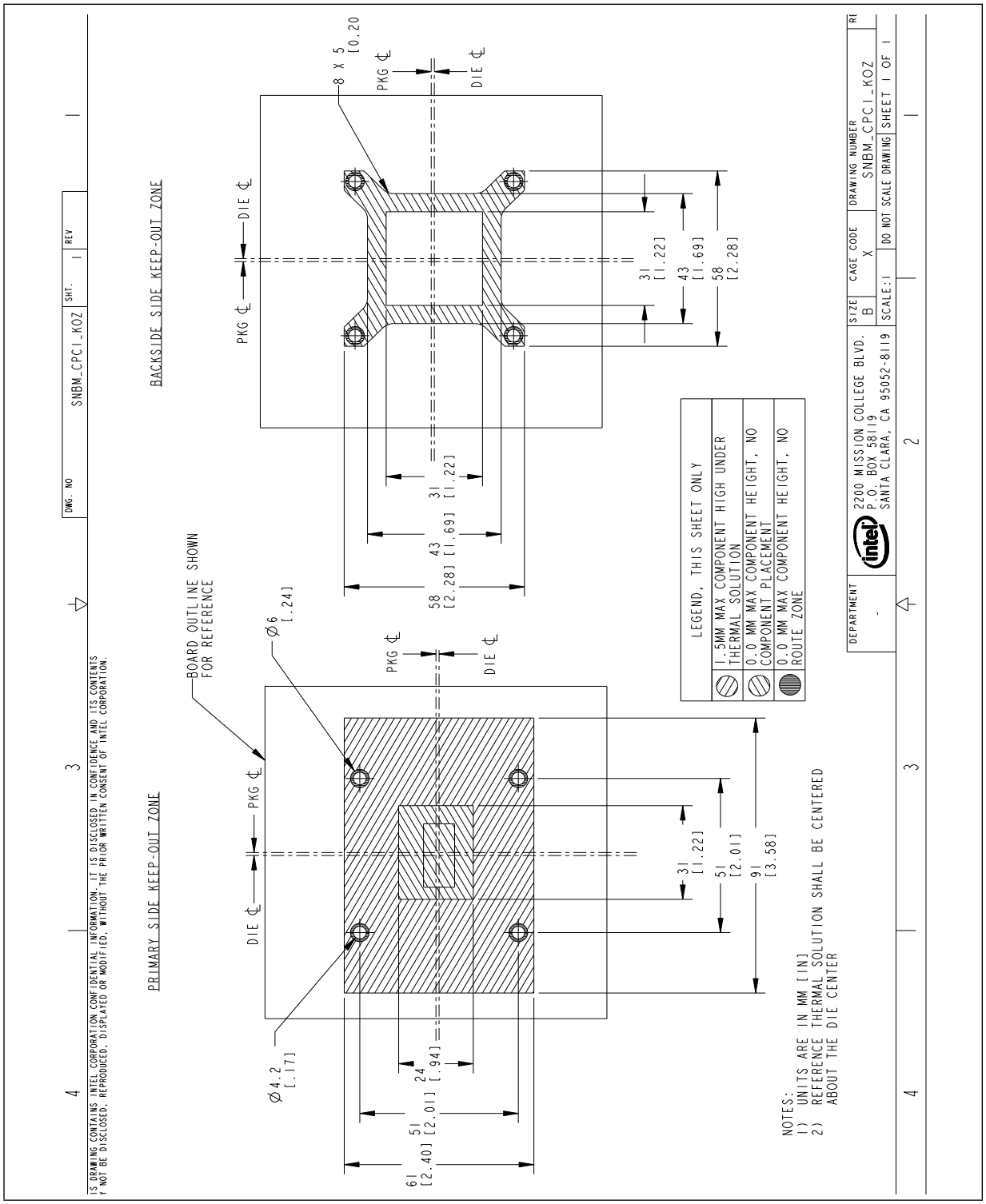
## Figure 27. Mini-ITX* Reference Heatsink Assembly (Sheet 1 of 2)



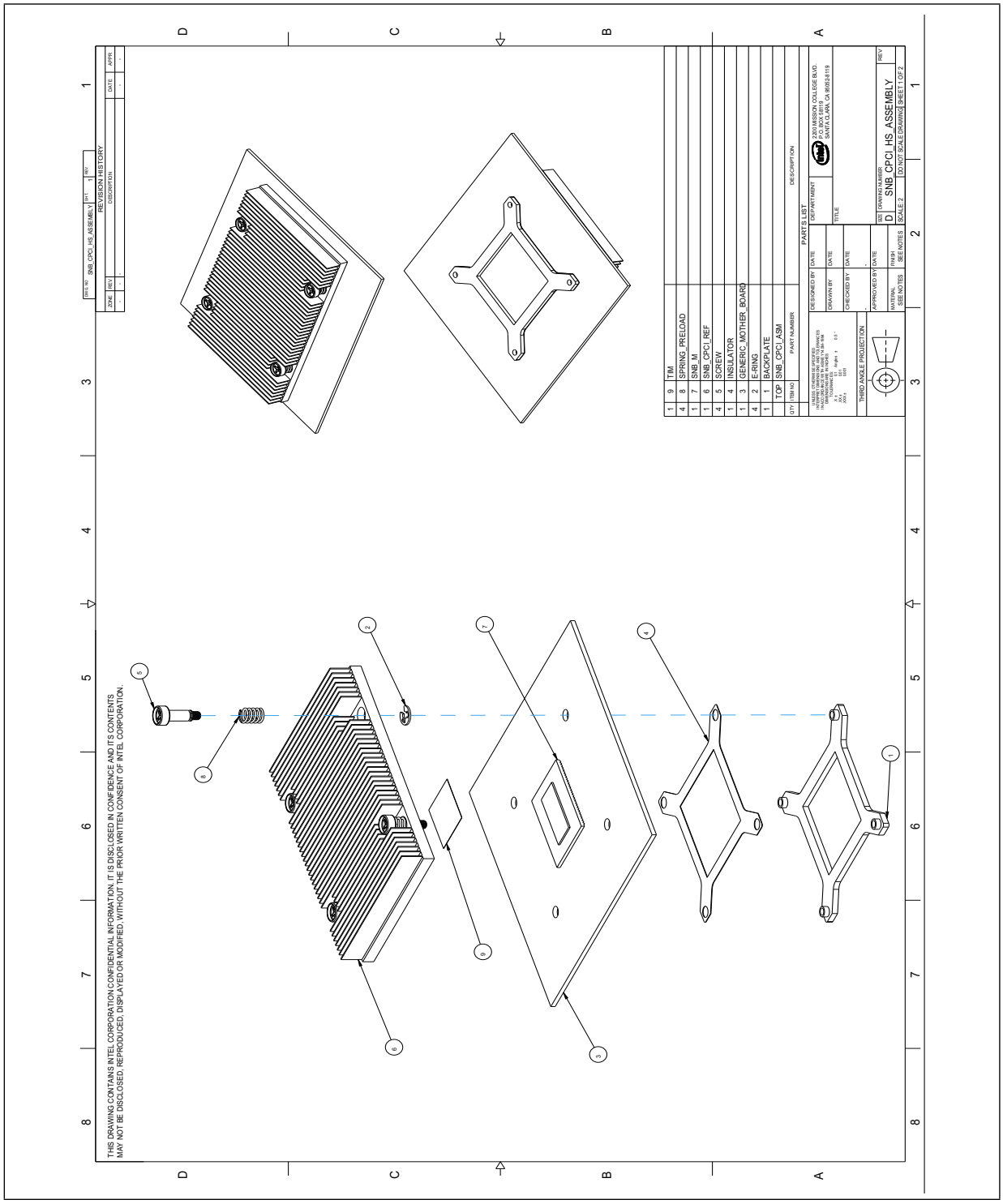
## Figure 28. Mini-ITX* Reference Heatsink Assembly (Sheet 2 of 2)



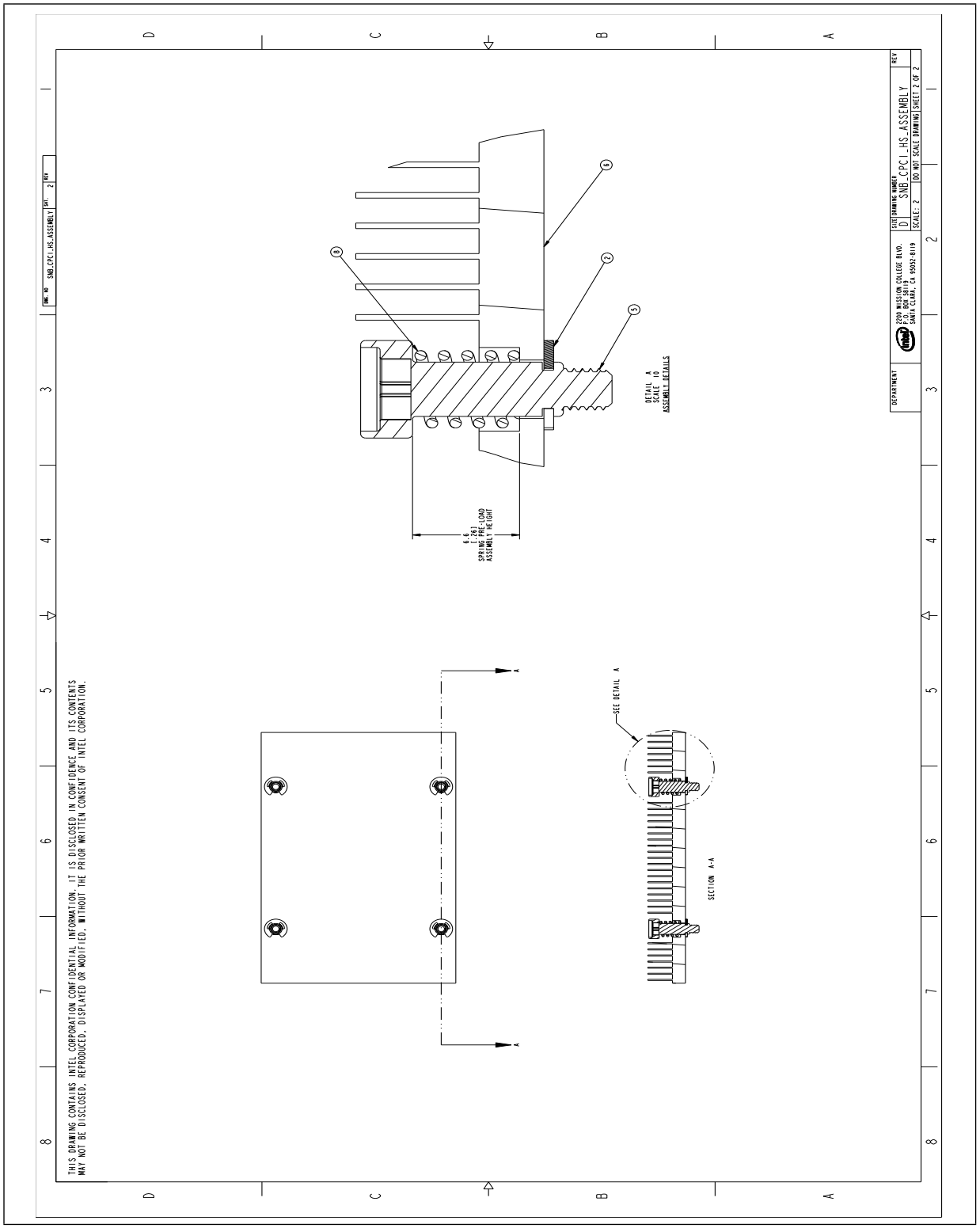
## Figure 29. cPCI* Reference Heatsink PCB Keep Out Zone Requirements



## Figure 30. cPCI* Reference Heatsink Assembly (Sheet 1 of 2)



## Figure 31. cPCI* Reference Heatsink Assembly (Sheet 2 of 2)



## Figure 32. cPCI* Reference Heatsink