

Product Brief

BridgeBuilder

High performance solutions with the lowest cost of ownership

Target Applications

- Core and edge routers
- Enterprise backbone switches
- 3G wireless aggregation routers
- VPN switches/routers
- Multiservice switches/routers
- SAN switches/routers
- Bus bridges

Features

1GHz Silicon Object Array

- Highest performance programmable logic device available
- Fully programmable field/feature upgradeable

High Speed Parallel I/O

- 50Gbps peak aggregate bandwidth per interface
- 8/16-bit LVDS
 - 800MHz DDR - 1600 MT/s
 - Configurable bit/byte deskew
- 32-bit, 350MHz SDR HSTL
 - 1.5V or 1.8V Class I
- Independent transmit PLLs

DDR Memory Controller

- 250MHz DDR - 500 MT/s
- Support for RDRAM, DDR, DDRII, SRAM and Σ SRAM

General Purpose I/O

- 2.5V, 3.3V tolerant
- PCI compatible
- Programmable clocking

High Speed Serial I/O

- PCI Express, XAUI, Fibre Channel, 10G Fibre Channel, Gigabit Ethernet compatible
- 1 - 4.25Gbps

NoGATES Development Tools

- No synthesis or timing closure
- Precoded library elements
- JTAG debugger
- Comprehensive evaluation board

Overview

The BridgeBuilder™ series of products combine the MathStar FPOA™ (Field Programmable Object Array) with high speed I/O and memory interfaces to create a programmable communications platform. These devices have the performance to support the advanced network services required by next generation networking applications running at 10Gbps or faster. The programmability and 1GHz clock of the FPOA make the devices ideally suited for a wide variety of network, computing, and bus bridging applications. With MathStar's NoGATES™ tool flow and BridgeBuilder library elements, custom solutions can be realized in a very short development that preserves your architecture and software.

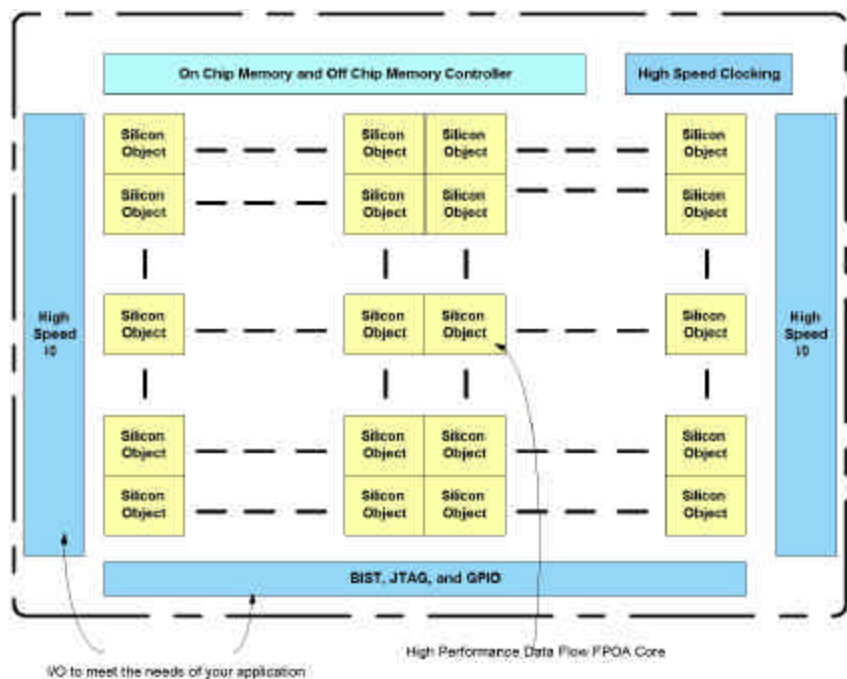
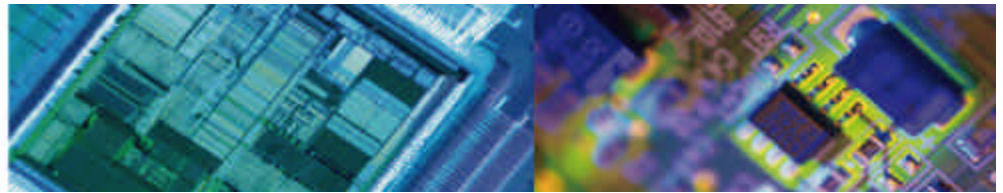


Figure 1. BridgeBuilder Device

Builder Family Silicon

Device	Number of Silicon Objects	High Speed Parallel IO Interfaces	Serial IO Transceivers	GPIO	36-bit Memory Controllers
SOA13C20	200	0-1	0 or 4	50-200	0-2
SOA13C40	400	0-2	0 - 16	50-200	0-2
SOA13C80	800	0-2	0 - 16	50-200	2-4
SOA13C120	1200	0-3	16	50-200	4



Applications

- Packet Parsing
- Subport Aggregation
- Hashing
- Classification
- Policing
- Accounting, Statistics Collection
- Admission Control, Packet Filtering
- Control Plane Bridge
- Fabric Interface

BridgeBuilder Application Library

The BridgeBuilder application library provides production ready interfaces and packet processing elements. Since they are implemented in the FPOA, they are fully customizable enabling feature enhancement and product differentiation. All of the library elements support MathStar's *SOBus* (Silicon Object Bus) application interface allowing users to seamlessly mix and match BridgeBuilder library elements and custom designed functions.

OIF SPI4.2

- 800MHz, 51.2Gbps peak bandwidth
- Dynamic deskew
- 1-256 Subports
- Packet segmentation and reassembly

HyperTransport

- Configurable 800MHz 2/4/8/16-bit interface, 51.2Gbps peak bandwidth
- Tunnel or end point
- Double hosted chains

Unified Memory Controller

- Combines independent 36-bit memory controllers into a unified 72-bit controller

PCI-X

- 133MHz PCI-X 1.0 compatible
- 32 or 64-bit AD bus
- Configurable Tx and Rx FIFO depths

SPI3

- 150MHz 32-bit interface
- Packet and byte modes

Multichannel FIFO

- Configurable from 1-256 channels
- Static or dynamic memory allocation
- Target internal or external RAM

RapidIO

- 8-bit interface
- 250MHz or 500MHz operation
- Compliant with RapidIO interconnect specification 1.2

Packet Parser

- Configurable Start of Packet offset and extraction size
- Chainable for multifield and recursive extraction

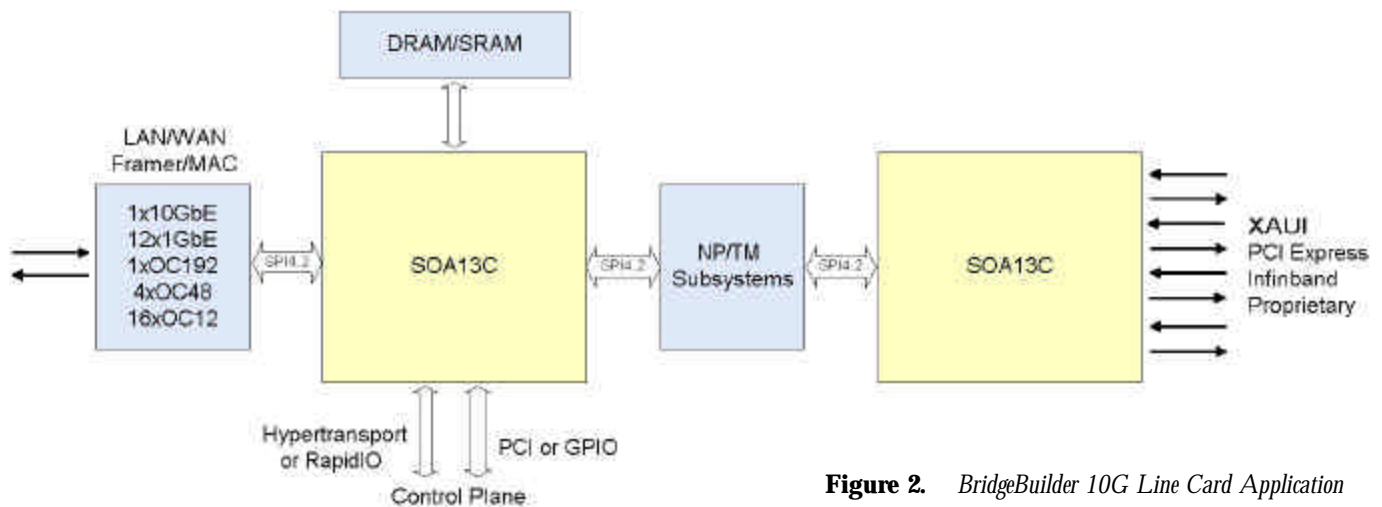


Figure 2. BridgeBuilder 10G Line Card Application

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