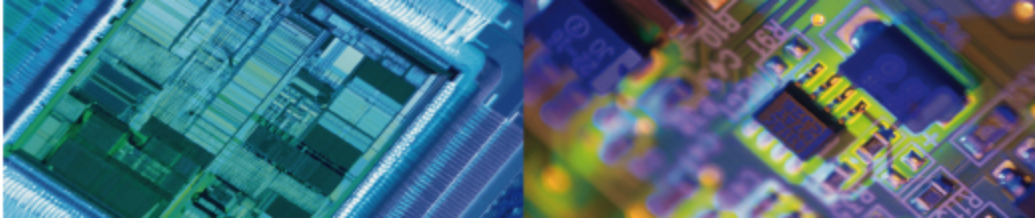
MATHSTAR™

Fast Silicon, Faster Solutions



Technology Overview

MathStar FPOA Architecture

A New Approach to High Throughput, Scalable, and Reprogrammable Design

Features

Ultra High Performance
- 1GHz clock rate

Rapid Time-to-Market
- Fast design cycle, no timing closure
- Extensive pre-coded application libraries
- Off-the-shelf field programmable

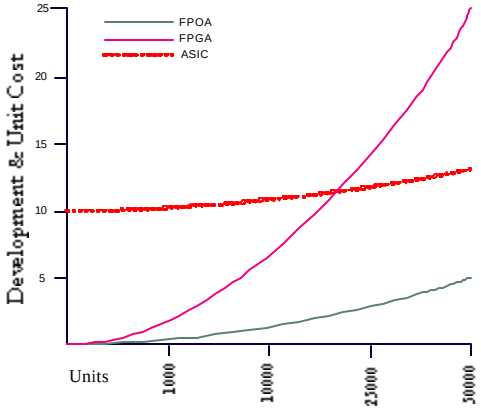
Lowest Cost-to-Market
- Fast design cycle
- Inexpensive development tools
- No ASIC mask or tooling charges

Longest Time-in-Market
- Reprogrammable device
- Ability to be modified in system to meet standards changes

High Functional Density
- Performance density >5x FPGA

Simplified Design Process
- No gate level synthesis, no layout timing closure

Low Unit Cost Compared to FPGA



Solution Cost Comparison

Overview

MathStar's Field Programmable Object Array (FPOA™) is a new approach to a reprogrammable platform that offers unheralded performance advantages. FPOA products are large parallel heterogeneous arrays with 1GHz internal clock speed, flexible I/O interconnect, and powerful high-level software tools. Initial products are aimed at multi-gigabit line rate processing and high-performance DSP applications.

Why Reprogrammable?

Transistor density is increasing at a tremendous rate as the industry marches toward 90 and 65nm technologies. Often, the processing potential of these technologies remains locked due to prohibitively high-development complexity, time, and cost. Currently, ASIC development costs in 0.13µm can reach as high as $10M[1]. While traditional microprocessor and Field Programmable Gate Array (FPGA) based designs avoid these high Non-Recurring Engineering (NRE) expenses, the overhead required creates a significant performance and area penalty leading to high unit cost. In certain cases, such as multi-gigabit line rate communications processing, performance constraints render these solutions untenable.

To fill the void, MathStar created the FPOA using our NoMASK™ technology. These application-targeted arrays minimize design time and NRE cost while improving overall performance and reducing per-chip cost. Reprogrammable silicon arrays provide the additional benefit of allowing vendors to begin design before specifications (standards) are finalized, allowing changes to be made through software upgrades. The FPOA time-to-market and time-in-market provide significant advantages over custom silicon. Commercial reprogrammable platforms are now poised to bring substantial value to the marketplace.

Initial design work indicates performance density to be greater than five times that of FPGAs. This density advantage means that designs implemented in FPOAs can go to high volume production and provide a cost effective solution for years.

Field Programmable Object Array (FPOA™): Massively parallel processor arrays with 1 GHz internal clock frequency and flexible high-bandwidth I/O.
Silicon Object™: Each individual element found in the FPOA™ is called a Silicon Object™.
NoMASK™: MathStar technology with no fabrication cycles, no physical timing to close and no expensive mask costs to pay.
NoGATES™: MathStar technology with no gate level synthesis and no timing closure.

[1] EE Times, "ASIC Slump Slows Transition to 130nm Technology." October 25, 2002.

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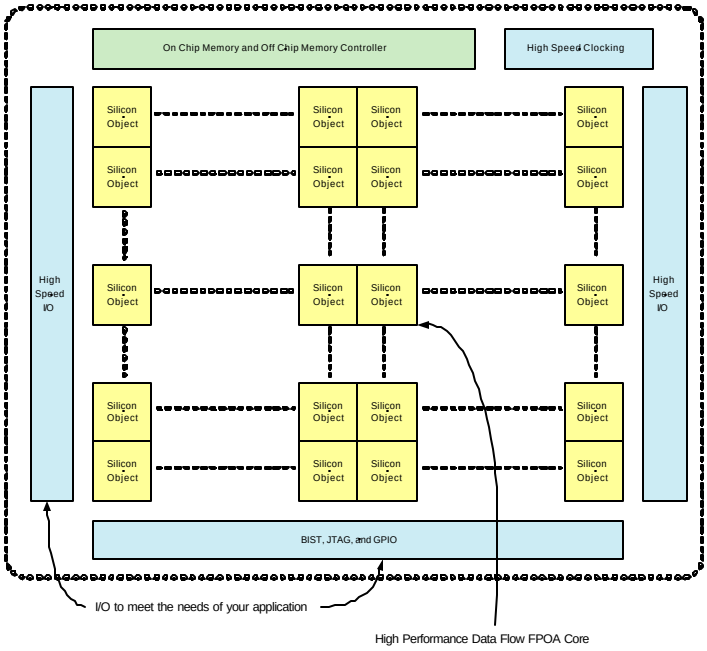
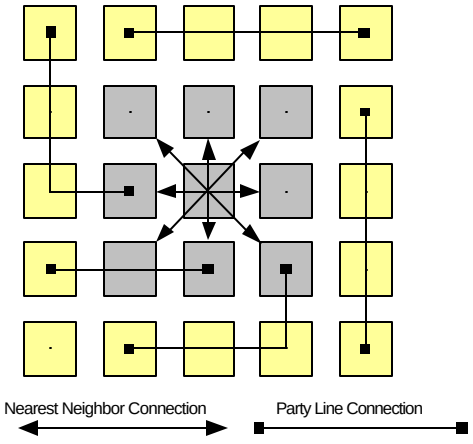
The Architecture

The Field Programmable Object Array or (FPOA) is a heterogeneous medium-grained array composed of hundreds of individual processing elements. Each element is called a Silicon Object™. Within the array, the data path and control path are loosely coupled, yet independently configured. The data path is 16 bits wide while the control path is bit-wise granular. Multiple objects can be utilized to create wider data paths. Each Silicon Object has its own program and data memories and operates without the aid of global control.

Silicon Objects

There are five Silicon Object types within the common Silicon Object array structure: the Arithmetic Logic Unit (ALU), the Content Addressable Memory (CAM), the Cyclic Redundancy Check (CRC), the Multiply Accumulator (MAC), and the Register File (RF). In addition to these five Silicon Object types, RAM memory resources are distributed in the array. The function and ratio of these different Silicon Objects are chosen based on detailed study of applications space for the product offerings.





Communication

Communication between Silicon Objects is primarily Nearest Neighbor, with our patent pending Party Line™ technology available to communicate longer distances. Objects are allowed to change communication patterns on a per-clock basis. Each ALU Silicon Object has a program memory of eight instructions that contain both operation and communication directions. The instructions are loaded at power up and can be reconfigured by the host system. Intelligent scheduling and routing tools deterministically allocate instructions to each object before run-time. The control path guides program execution while data is moved and operated upon via the 16-bit data path. From this view, instructions are the mechanisms that tie the independent control and data paths together within the array.

Using these object types and communications infrastructure, MathStar fabricates arrays of hundreds, to thousands, of objects. These arrays are matched with I/O and libraries to enable rapid custom designs

Silicon Object Types	Benefits
ALU • 16-bit add/sub, shift/rotate, AND/OR/XOR - Cascade larger words via status bit (SB) • Eight configured instructions per object • 4-way branch, conditional execution, data pass - Configurable to follow control bits	Flexible general purpose processor that can be cascaded for massive parallelism. Data and control processing State machines
Truth Function • Four 4:1 lookup tables • Shared object with ALU	Used to implement arbitrary control functions.
MAC • 16x16 single clock cycle multiplier • 40-bit accumulator - Up to 256 MACs before Overflow/Saturation	Supports DSP functions including high performance FFTs and FIRs. Cascade with ALUs for wider multiplications.
RF • 320 Bytes • Configurable 20 or 40-bit data. • Two operational modes - Dual-ported RAM, single-cycle access - Single-cycle FIFO	Data buffering, FIFOs, constants, queue memory and link lists
CRC • Single-cycle CRC-32 and CRC-16	Reconfigurable CRC unit for data integrity checking. Supported applications include Hyper Transport, RapidIO and PCI Express.
CAM • Sixteen 20-bit patterns with wildcards • 20-bit result • Output feedback	Variable width bit-field parsing and implementing state machines
Internal Block RAM (IRAM) • 1024 x 76b (9KB)	Internal data buffering

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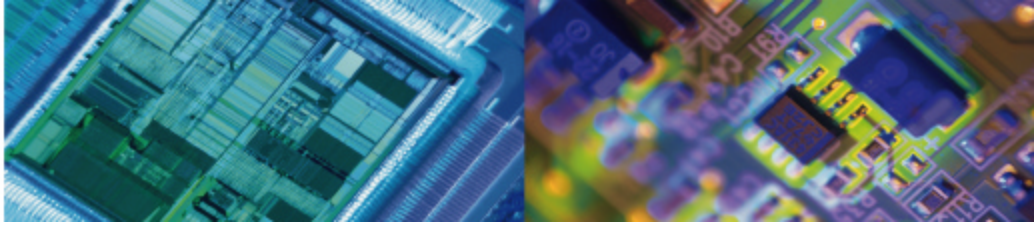

I/O Features	Benefits
DDR Memory Controller • 250 MHz DDR, support for RLDRAMII, DDRII SRAM and ΣSRAM • 36-bit datapath yielding 2.25GBps peak bandwidth per controller • Controllers can be cascaded to scale bandwidth	Memory subsystem to support high speed protocol and DSP applications.
High Speed Parallel I/O • 50Gbps peak aggregate bandwidth • Two modes of operation - 8/16 bit LVDS (800 MHz DDR - 1600 MT/s and Configurable bit/byte deskew) - 32 -bit, 250MHz SDR HSTL (1.5V or 1.8V Class I)	Compatible with Industry standard interfaces including SPI4.2, HyperTransport, RapidIO.
High Speed Serial (SerDes) • 1-4.25Gbps • Programmable pre-emphasis, transmit voltage, termination, equalization • Integrated 8B/10B and 64/66 encoders/decoders • Programmable link aggregation for 1-32 lanes	Compatible with Industry standard interfaces including PCI Express, Serial RapidIO, XAUI, Fibre Channel, and Gigabit Ethernet.
General Purpose IO • LVCMOS - 2.5V, 3.3V tolerant • Highly programmable clocking - Generate output clocks from core - Source Synchronous input or output	Compatible with Industry standard interfaces including PCI and SPI3.

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