Proven Track Record at 32/28nm
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- 32/28nm Market Driver

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- 32/28nm Process & Design Infrastructure
- 32/28nm Success Story

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Smart & Innovative Foundry Solution
32/ 28nm Market Driver
Mobile SoC Design Trend

- More integrated functionality in smaller area
- More performance at lower VDD

- Mobile CPU: > 25,000 DMIPS
- Multimedia Contents: > Full HD 1080P (w/ 3D & 3D GFX)
- DRAM Bandwidth: > 20GB/sec

Higher Speed & Higher Integration
Lower Power for Longer Battery Life & Thermal Management

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HKMG Process Benefits - Low Power

- **Reduced leakage and boosted performance**

  - 1.4x device performance or 1/10 total leakage over Poly-Si/SiON

![Graph showing comparison between Conventional Poly-Si/SiON and HKMG](image_url)
HKMG Process Benefits - The Big Leap

- Advanced 1st Gen HK/ MG
  - 1.4X Performance Improvement
  - 0.4X Area Reduction (Std. cell)
  - 0.6X Active power Reduction

*28nm comparison to 45nm*
32/ 28nm Process & Design Infra
Advanced Low Power HK/MG Process Technology

- **32LP**
  - Vdd Core: 1.0V
  - Logic CPP: 126nm
  - Device Offering: 4 Vth
  - SRAM Bitcell: 0.149um2
  - M1x pitch: 100nm

- **28LPP**
  - Vdd Core: 1.0V
  - Logic CPP: 113.4nm
  - Device Offering: 4 Vth
  - SRAM Bitcell: 0.120um2
  - M1x pitch: 90nm
**PDK Solution**

- Comprehensive PDK are proven in multiple complex SOCs in high volume

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<thead>
<tr>
<th></th>
<th>Synopsys</th>
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<th>Mentor Graphics</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPICE</td>
<td>V</td>
<td>V</td>
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<td>DRC</td>
<td>V</td>
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<td>LVS</td>
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<td>PEX</td>
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<td>P&amp;R Techfile</td>
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Library Solution

Product Proven Library

ARM Libraries with complementary Samsung IP

Logic Libraries
- Multi channel & multi Vt
- 9 and 12 tracks
- Power Management
- ECO Kits

Memory Compilers
- Superior SRAM Architecture
- HD, HS Memory Compilers
- Multi-Periphery Options

Programmable Options
- eFuse
- OTP

Interfaces
- DDR 3+
- General Purpose I/Os

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**IP Solution**

Collaboration is delivering industry leading solutions

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**Various silicon proven IP**

- **Processor Cores**
  - ARM7/9/11 Series
  - Cortex M/R/A Series

- **System IP**
  - Interconnect IP
  - Memory controllers
  - System Controllers
  - Peripherals
  - CoreSight

- **High Speed Interface IP**
  - SATA, PCIe
  - USB2/3, HSI C
  - LVDS, mini-LVDS, sub-LVDS
  - MIPI D/M-PHY
  - HDMI, DisplayPort

- **Multimedia IP**
  - JPEG Codec
  - NTSC/ PAL encoder

- **Standard Cell Library**
  - HD/HS
  - Multi Vth
  - Multi channel length
  - Power management kit

- **Embedded Memory**
  - (HD/HS/LP) SRAM, VROM
  - eFuse, OTP

- **I/O**
  - In-line, staggered, multi-row
  - Wide-range GPIO

- **Mixed-Signal Core**
  - ADC, DAC, AFE
  - PLL
  - Audio CODEC
  - Temp sensor, LDO
  - Memory Interface
    - DDR2/3, LPDDR2/3

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32LP – Mass Production
28LPP – Silicon Validation

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Smart & Innovative Foundry Solution
## Advanced DFM Solution

### Advanced IP & Chip-level DFM Methodology

<table>
<thead>
<tr>
<th>Family</th>
<th>Kit</th>
<th>IP</th>
<th>Chip</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>32/28nm</td>
<td>32/28nm</td>
</tr>
<tr>
<td><strong>Rule-based Verification</strong></td>
<td>DRC</td>
<td>M</td>
<td>M</td>
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<td></td>
<td>LUP (Litho Unfriendly Pattern)</td>
<td>M</td>
<td>M</td>
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<td></td>
<td>PHC pattern matching (Process Hotspot Check)</td>
<td>M</td>
<td>M</td>
</tr>
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<td></td>
<td>MCD/MAS (Recommended Rule Deck)</td>
<td>R</td>
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</tr>
<tr>
<td></td>
<td>VIA</td>
<td>M</td>
<td>M</td>
</tr>
<tr>
<td><strong>Model-based Verification</strong></td>
<td>LHC (Litho Hotspot Checker)</td>
<td>M</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>FLHC (Fast Litho Hotspot Checker)</td>
<td>M</td>
<td>M</td>
</tr>
<tr>
<td></td>
<td>CMP</td>
<td>R</td>
<td>M</td>
</tr>
<tr>
<td></td>
<td>CAA</td>
<td>R</td>
<td>R</td>
</tr>
<tr>
<td><strong>Layout Enhancement</strong></td>
<td>LUP-enabled router</td>
<td>M</td>
<td>M</td>
</tr>
<tr>
<td></td>
<td>PHR (Process Hotspot Repair)</td>
<td>M</td>
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<td>Dummy Fill</td>
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*M: Mandatory, R: Recommend*
Advanced Design Methodology

- Product proven DM through market leading products

- Advanced DM complemented by adaptive supply voltage (ASV) and adaptive body bias (ABB)
- ABB is beneficial to sustain thermal runaway by reducing leakage current and minimizing Freq drop
32/ 28nm Success Story
32nm HKMG AP with GHz multi-core CPU

- **Power comparison to 45nm AP**
  - On CPU (2D Flash play) : 45% ↓
  - On GPU (3D Cube rendering) : 48% ↓

![CPU Power Consumption](image1)

![GPU(3D) Power Consumption](image2)

32 HKMG

45 PSiON

32 HKMG

45 PSiON

**Smart & Innovative Foundry Solution**
Conclusion

**Product Proven** Design and Process Technology in 32nm/28nm

- High-K/Metal Gate
- PDK / Library / IP / Design Methodology

**Collaboration** is delivering industry leading solutions
Thank You