Samsung Foundry

Proven Track Record at 32/28nm

Smart & Innovative Foundry Solution

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32/28nm Market Driver

Mobile SoC Design Trend

- **More integrated functionality in smaller area**
- **More performance at lower VDD**

Mobile CPU

> 25,000 DMIPS

Multimedia Contents

> Full HD 1080P (w/ 3D & 3D GFX)

DRAM Bandwidth

> 20GB/sec

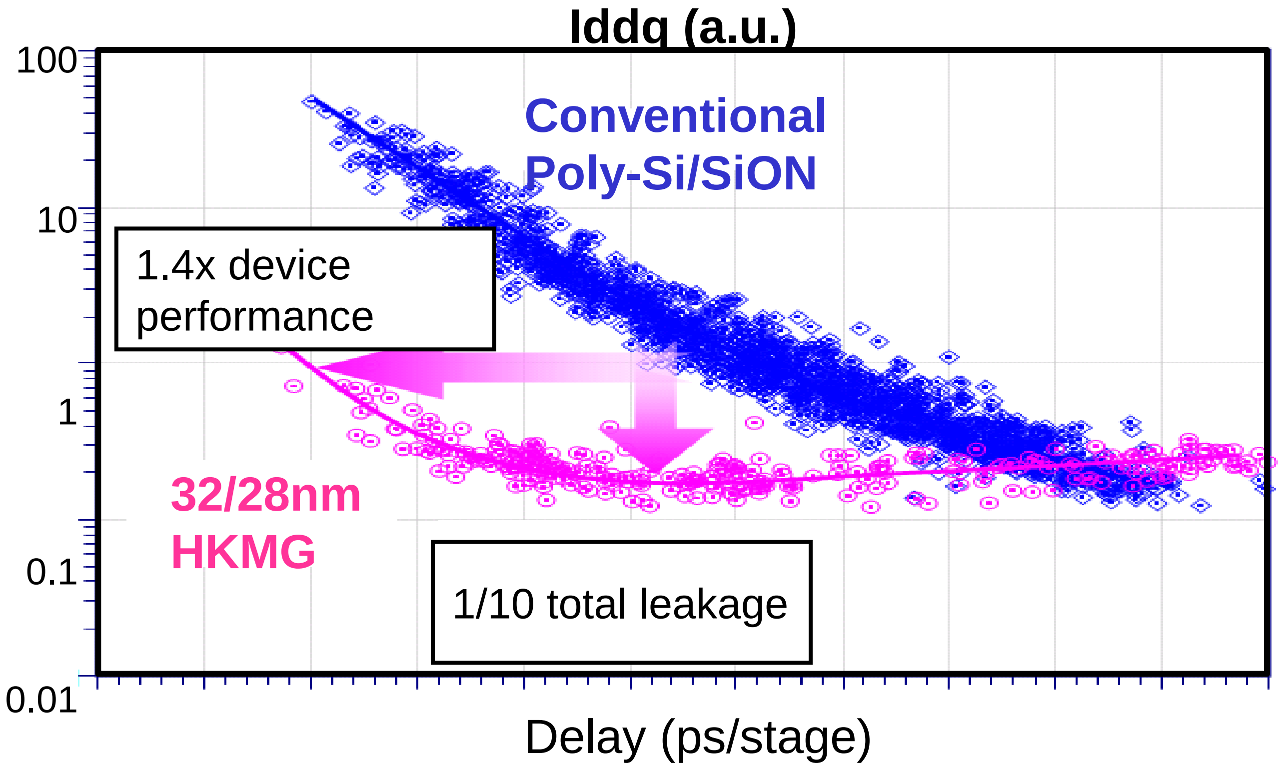
Higher Speed &
Higher Integration

Lower Power for
Longer Battery Life &
Thermal Management

HKMG Process Benefits – Low Power

- **Reduced leakage and boosted performance**

-1.4x device performance or 1/10 total leakage over Poly-Si/SION



HKMG Process Benefits – The Big Leap

Advanced 1st Gen
HK/MG

1.4X
Performance Improvement

0.6X
Active power Reduction

0.4X
Area Reduction (Std. cell)

*28nm comparison to 45nm

32/28nm
Process & Design Infra

Process Technology Solution

■ Advanced Low Power HK/MG Process Technology

	32LP	28LPP
Vdd Core	1.0V	
Logic CPP	126nm	113.4nm
Device Offering	4 Vth	4 Vth
SRAM Bitcell	0.149um2	0.120um2
M1x pitch	100nm	90nm

PDK Solution

- Comprehensive PDK are proven in multiple complex SOCs in high volume

	SYNOPSYS Predictable Success	cadence	Mentor Graphics www.mentor.com
SPICE	V	V	
DRC	V		V
LVS	V		V
PEX	V	V	V
P&R Techfile	V	V	

Library Solution

Product Proven Library

ARM Libraries with complementary Samsung IP

Logic Libraries
- Multi channel & multi Vt
- 9 and 12 tracks
- Power Management
- ECO Kits

Memory Compilers
- Superior SRAM Architecture
- HD, HS Memory Compilers
- Multi-Periphery Options

Programmable Options
- eFUSE
- OTP

Interfaces
- DDR 3+
- General Purpose I/Os

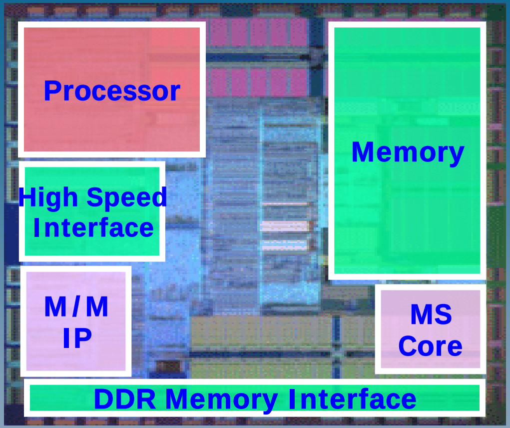
IP Solution

Collaboration is delivering industry leading solutions

From analog to processor cores

Various silicon proven IP

- **Processor Cores** ARM
  - : ARM7/9/11 Series
  - : Cortex M/R/A Series
- **System IP** ARM
  - : Interconnect IP
  - : Memory controllers
  - : System Controllers
  - : Peripherals
  - : CoreSight
- **High Speed Interface IP** SYNOPSYS
  - : SATA, PCIe
  - : USB2/3, HSIC
  - : LVDS, mini-LVDS, sub-LVDS
  - : MIPI D/M-PHY
  - : HDMI, DisplayPort
- **Multimedia IP**
  - : JPEG Codec
  - : NTSC/PAL encoder



32LP – Mass Production
28LPP – Silicon Validation

- **Standard Cell Library** ARM
  - : HD/HS
  - : Multi Vth
  - : Multi channel length
  - : Power management kit
- **Embedded Memory** ARM
  - : (HD/HS/LP)SRAM, VROM
  - : eFuse, OTP
- **I/O** ARM
  - : In-line, staggered, multi-row
  - : Wide-range GPIO
- **Mixed-Signal Core** ANALOG BITS
  - : ADC, DAC, AFE
  - : PLL
  - : Audio CODEC
  - : Temp sensor, LDO
- **Memory Interface** SYNOPSYS
  - : DDR2/3, LPDDR2/3

Advanced DFM Solution

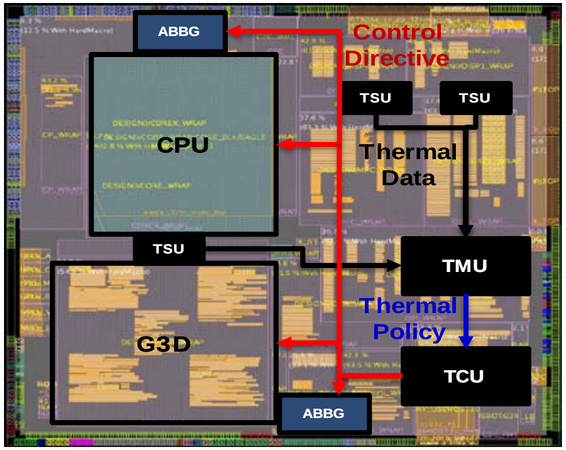
Advanced IP & Chip-level DFM Methodology

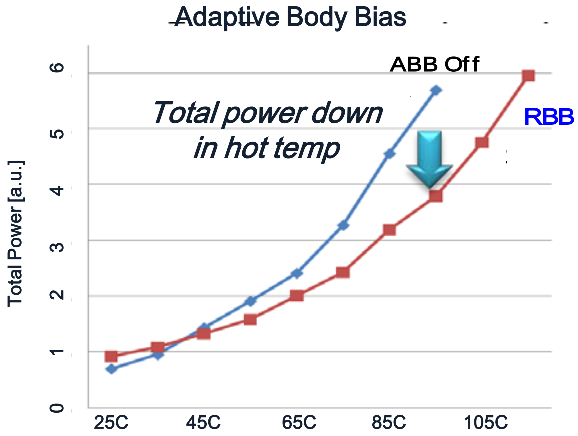
Family	Kit	IP	Chip
		32/28nm	32/28nm
Rule-based Verification	DRC	M	M
	LUP (Litho Unfriendly Pattern)	M	M
	PHC pattern matching (Process Hotspot Check)	M	M
	MCD/MAS (Recommended Rule Deck)	R	-
	VIA	M	M
Model-based Verification	LHC (Litho Hotspot Checker)	M	-
	FLHC (Fast Litho Hotspot Checker)	M	M
	CMP	R	M
	CAA	R	R
Layout Enhancement	LUP-enabled router	M	M
	PHR (Process Hotspot Repair)	M	M
	Dummy Fill	M	M

M : Mandatory, **R : Recommend**

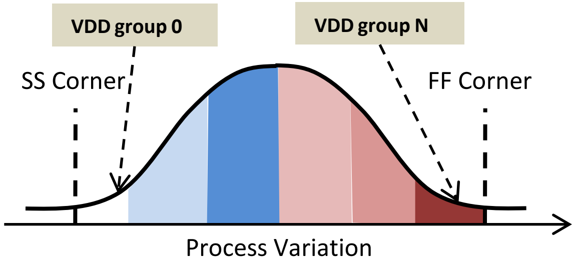
Advanced Design Methodology

Product proven DM through market leading products





Adaptive Supply Voltage



- ▶ Advanced DM complemented by adaptive supply voltage (ASV) and adaptive body bias (ABB)
- ▶ ABB is beneficial to sustain thermal runaway by reducing leakage current and minimizing Freq drop

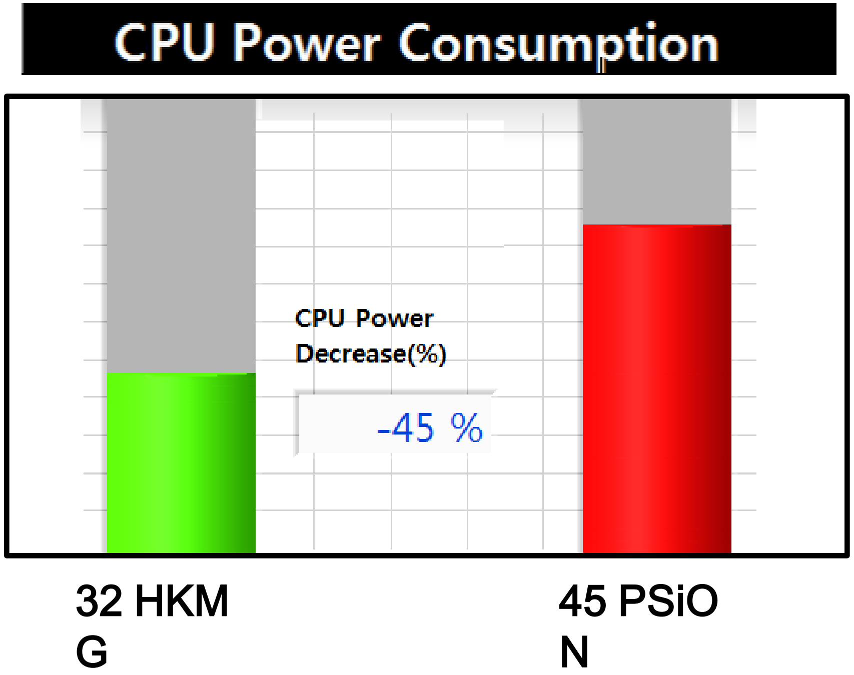
32/28nm
Success Story

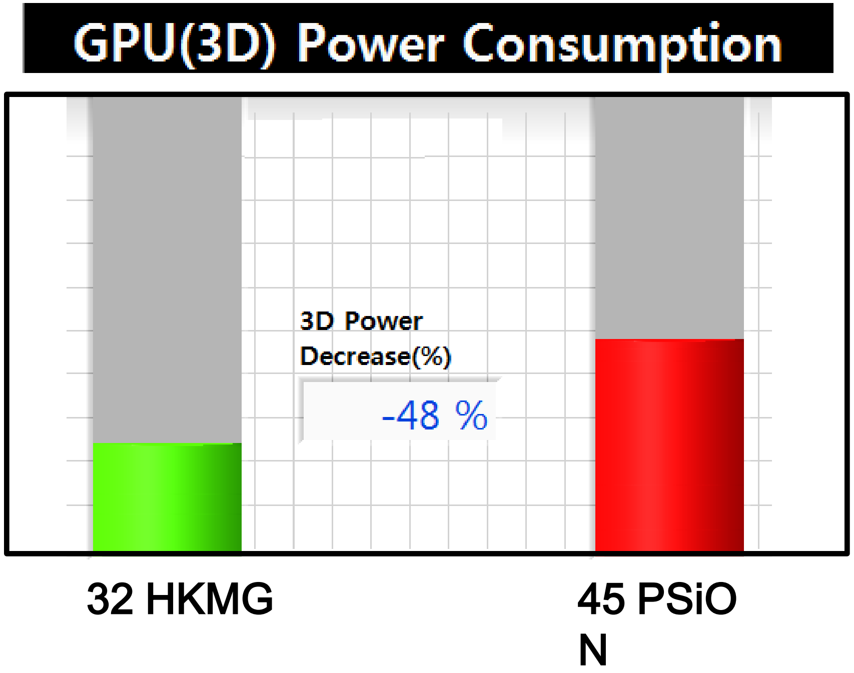
32nm HKMG AP with GHz multi-core CPU

Power comparison to 45nm AP

-On CPU(2D Flash play) : 45%↓

-On GPU(3D Cube rendering) : 48%↓





Conclusion

Product Proven Design and Process Technology **in 32nm/28nm**

- ▶ High-K/Metal Gate
- ▶ PDK / Library / IP / Design Methodology

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Thank You