MELPS 41/42 MICROCOMPUTERS

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SINGLE-CHIP 4-BIT CMOS MICROCOMPUTER

DESCRIPTION

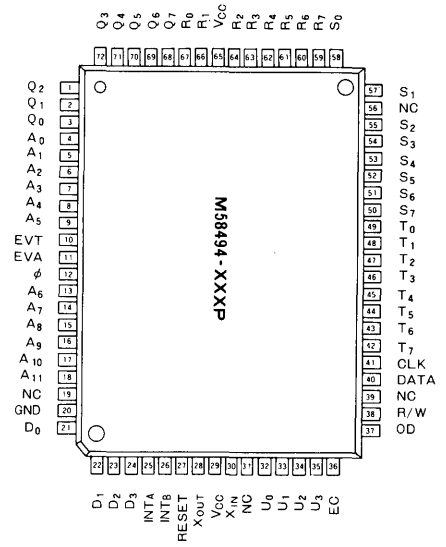
The M58494-XXXP is a single-chip 4-bit microcomputer fabricated using CMOS technology in a 72-pin plastic flat package. It has a 4096-word by 10-bit mask-programmable ROM and a 32-word by 4-bit RAM. RAM capacity can be expanded to as much as 4096 words by 4 bits by directly connecting generally available CMOS RAMs.

The device is designed for application where the low power dissipation of CMOS is essential.

FEATURES

- Basic machine instructions 92
- Basic instruction execution time (at 455kHz clock frequency) 8.8μs
- Large memory capacity:
  - ROM ..... 4096-word x 10-bit
  - Internal RAM ..... 32-word x 4-bit
  - External RAM ..... 4906-word x 4-bit (max)
- Single 5V power supply
- Saving of last data pointer 4-level
- Subroutine nesting 12-level
- Internal timer: Timer 1 ..... 14-bit
  Timer 2 ..... 4-bit
- Internal event-counter 4-bit
- I/O port for external RAMs (all three-state)
  - Address (port A) 12-bit
  - Control signals (R/W, 0D) 2-bit
  - Data I/O (port D) 4-bit
- General-purpose registers 32-bit
- I/O port (port Q) 8-bit
- I/O port (port R) ..... 4-bit x 2
- I/O port (serial data port) 2-bit

PIN CONFIGURATION (TOP VIEW)



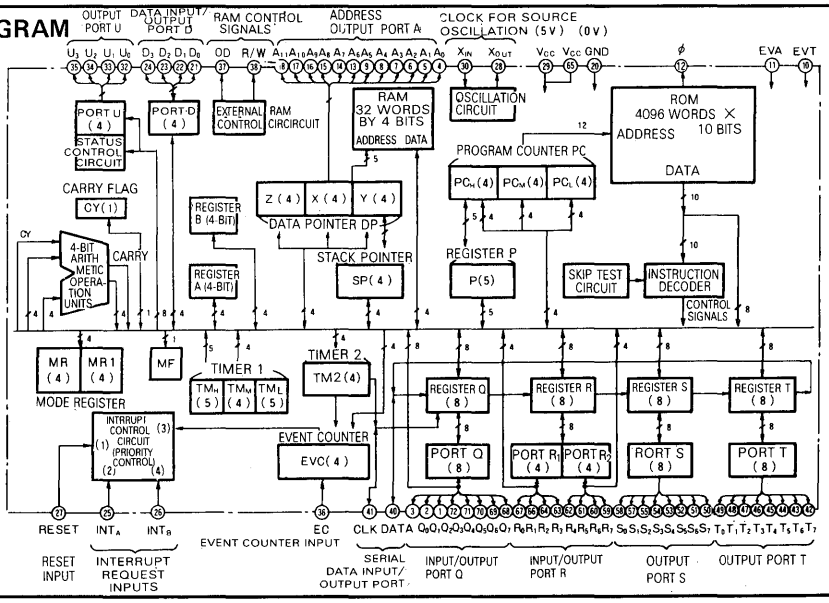
Package Outline 72P2

- Output ports (port S, port T) ..... 8-bit x 2
- Output port (port U, three-state output) 4-bit
- Event-counter input (port EC) 1-bit
- Interrupt function (priority interrupt type) 4-factor, 1-level

APPLICATIONS

- Electronic cash registers, electronic calculators (with printer and/or programmable)
- Office machines, intelligent terminals, data terminals
- Sewing machines, knitting machines, etc.

BLOCK DIAGRAM



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Outline Specifications of M58494-XXXP

Item			Performance
Number of basic instructions			92
Execution time of basic instructions			8.8μs (at V_{CC} = 5V, f = 455kHz)
Clock frequency			100 ~ 455kHz
Memory capacity	ROM		4096 words × 10 bits
	RAM (built-in)		32 words × 4 bits
	RAM (external)		4095 words × 4 bits (max.)
Input/output port for external RAM	Address (port A)		12 bits x 1 (3 states)
	Control signal (port OD and R/W)		2 bits (3 states)
	Data bus (port D)		4 bits x 1 (3 states)
Input/output port	Q	Input	8 bits x 1
		Output	8 bits x 1
	R	Input	4 bits x 2
		Output	8 bits x 1
	S	Output	8 bits x 1
	T	Output	8 bits x 1
	DATA	Serial data	1 bit (input/output port)
	CLK	Synchronizing pulse	1 bit (input/output port)
	U	Output	4 bits x 1 (3-state)
	EC	Input	1 bit
Subroutine nesting			12 levels
Interrupt request			4 factors 1 level
Saving of data pointer			4 levels
Clock generation circuit			Built-in (oscillation reference element is outside)
Ports input/output characteristics	Absolute maximum rating voltage		V_{CC}
	Input/output characterstics		Interchangeable with CMOS logic series
Power supply voltage	V_{CC}		5V (nominal)
	V_{SS}		0 V
Element structure			CMOS
Package			72-pin plastic molded flat package
Power dissipation			5 mW (at V_{CC} = 5V, f = 455kHz)

PIN DESCRIPTIONS

Pin	Name	Input or output	At reset	Function
X_{IN}	Source oscillation clock input	Input	—	Incorporates the clock oscillation circuit, for setting of the oscillation frequency. The oscillation reference device such as a ceramic filter for IF is connected between X_{IN} and X_{OUT}. When an external clock is used, connect the clock oscillation source to the X_{IN} pin and leave the X_{OUT} pin open.
X_{OUT}	Source oscillation clock output	Output	—	
RESET	Reset signal	Input	—	Resets the program counter PC and mode registers, and performs the reset initiation of the related input ports and output ports. For input/output ports, refer to the column for "At reset" of this table.
INT_A	Interrupt request signal A	Input	Disable	Input signals for interrupt request. Request is accepted on the rising edge of the signal. Besides these external input signals, the interrupt requests. T from timer 2/event counter are also received in the relative order RESET > INT_A > INT_T > INT_B. Since the interrupt requests are held at each latch, there will be none undetected.
INT_B	Interrupt request signal B	Input	Disable	
EC	Event counter input	Input	—	The input signal for the event counter, which program $2^0 \sim 2^4$ events of the event mode. This value is set as an initial value and countdown starts from this value to reach F_{16}, which then generates interrupt request signal INT_T.
$A_0 \sim A_{11}$	Address output port A	Output	Floating	The address signal for main memory (RAM) externally connected, in the form of a 3-state output. At MM mode where external memory is used the data of the data pointer DP is read out directly. In SM mode where internal memory (RAM) is used, the data of the data pointer Y immediately before switching to MM mode is transferred to the auxiliary latch (4 bits) prior to read-out. However, the lower 8 bits of the address signal ($A_0 \sim A_7$) are not affected by this mode, since data pointers X and Z are not related to latch operation.
$D_0 \sim D_3$	Data input/output port D	Input/ output	Floating	A 3-state input/output port to execute data transfer in 4-bit units to/from an externally connected main memory (RAM). Switching of input-output is made automatically by instruction.
OD	External RAM read signal	Output	Floating	The output port is 3-state and the read signal generated at the data input cycle is in the externally connected main memory(RAM). During a read cycle, it becomes automatically set to low-level.
R/W	External RAM write signal	Output	Floating	The output port is 3-state and the write signal generated at the data write cycle is in the externally connected main memory (RAM). During a write cycle, it is automatically set to low-level.
$U_0 \sim U_3$	Output port U	Output	Floating	The output port enables 3-state setting per 1-bit unit. The 3-state condition is modified by the data content of register B, and the data of register A is output. The output setting of port U, however, is made either by instruction SU unconditionally or by the instruction TPRA or TPRN, which transfers the data of the general-purpose register to ports Q, R, S and T.
$Q_0 \sim Q_7$	Input/output port Q	Input/ output	Input	The input/output port for 8-bit data transfer to/from register Q. Register Q enables data transfer between register A and register B. By instruction OPI, this port also functions to load the value (8-bit) of the immediate field of the ROM to register Q. Port Q data can be transferred to registers A and B as an input signal of 8 bits.
$R_0 \sim R_7$	Input/output port R	Input/ output	Input	The input/output port for 8-bit data transfer to/from register R. Register R enables data transfer between register A and register B. By instruction OPI, this port also functions to load the value (8-bit) of the data field of the ROM to register R. When port R is used as the input signal of a 4-bit unit, the data, 4 bits each can be transferred to register B.
$S_0 \sim S_7$	Output port S	Output	Low-level	The output port that enables 8-bit data transfer to/from register S. Register S enables data transfer between register A and register B. By instruction OPI, this port also functions to load the value (8-bit) of the data field of the ROM to register S.
$T_0 \sim T_7$	Output port T	Output	Low-level	The output port for 8-bit data transfer to register S. Register T enables data transfer between register A and register B. By instruction OPI, this also functions to load the value (8-bit) of the immediate field of the ROMto register T.
DATA	Serial data port	Input/ output	Floating	The input/output port normally is floating to handle the serial data of the 32-bit general-purpose register. At output mode data of the least significant bit of the general purpose register (the least significant bit of register T) is read out, and at the input mode, the input is to the most significant bit of the general-purpose register (the most significant bit of register O).
CLK	Serial data shift clock signal	Input/ output	Floating	The input/output port is normally floating to generate a shift clock pulse synchronized with the above serial data port. At output mode a shift clock pulse synchronized with the data transmission is generated and at the input mode, a shift pulse synchronized with the rate of data receiving is applied.

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BASIC FUNCTIONAL BLOCKS AND THEIR OPERATIONS

Program Memory ROM

The ROM stores 32-pages by 128 words of program and its addressing is performed by a program counter. The program counter consists of a 7-bit binary sequential counter and a 5-bit page register.

Program Counter PC

The ROM is composed of 32 pages of 128 words, and when program execution completes instruction at address 127, the binary counter is set to 0 and the next page is automatically incremented in the page-designation register.

The 12-bit contents of the program counter PC can be saved for up to 12 levels in the fixed stack area of the external main memory (RAM). In the execution of instructions BM and BMA, control can be returned to a former routine by storing the contents of the program counter before branching, in the execution of instructions RT, RTS, and RTI.

Register P

In the page register, the contents of register P are loaded by instructions BL, BA, BM and BMA. Instruction BMAB branches unconditionally to the address derived by using the contents of register A for the low-order 4-bits of the 12-bit PC, those of register B for the middle 4-bits, and those of the upper 4-bits of the 5-bit register P for the upper 4-bits, and then executes the instruction OPI of the branch, and simultaneously returns automatically.

Stack Pointer SP

A stack of 12 levels is provided for saving of the program counter PC in the fixed address area within the external main memory (RAM), and the contents of the stack pointer are used during addressing. The contents of the stack pointer are incremented by an interruption or in the execution of instructions BM and BMA, and are decremented in the execution of instructions RT, RTS and RTI.

Data Memory RAM

The internal RAM is used to store data in the form of two files each consisting of 16 words by 4 bits. The external RAM can be expanded up to 4096 words by 4 bits. These addresses are designated by a 12-bit data pointer. The contents of the data pointer can be saved for up to 4 levels in the stack region (fixed region in the external RAMs) by execution of a special instruction. The external RAM can be easily expanded without any extra interface circuits by connecting a 12-bit address signal, the 2-bit RAM control signal and the 4-bit data input/output signal. These signals can address external RAMs for up to 4096 x 4-bit words, thus incrementing the basic external minimum RAM organization of 256 x 4-bit words.

Data Pointer DP

This is a register of 12 bits addressing memory, being composed of registers X, Y, and Z, having 4 bits each. Register X address 16 files, each of which comprises 16 words. Register Y address data of 16 files (a file comprises 16 words). Register Z permits address specification such that data memory may be extended up to maximum of 16 sets of 4096 words by 4 bits, where one unit comprises 16 files (256 words by 4 bits).

Since the address of the external main memory (4096 words by 4 bits maximum) and the internal scratch-pad memory (32 words by 4 bits) are designated identically, the external main memory is selected by instruction MM, and the internal scratch-pad memory by instruction SM.

The contents of DP can be saved for up to 4 levels in the fixed stack region of the external main memory. This pointer is saved during the execution of instruction SDP, and is restored by instruction LDP.

When the data pointer stack is not used, the entire stack may be used as a program counter stack.

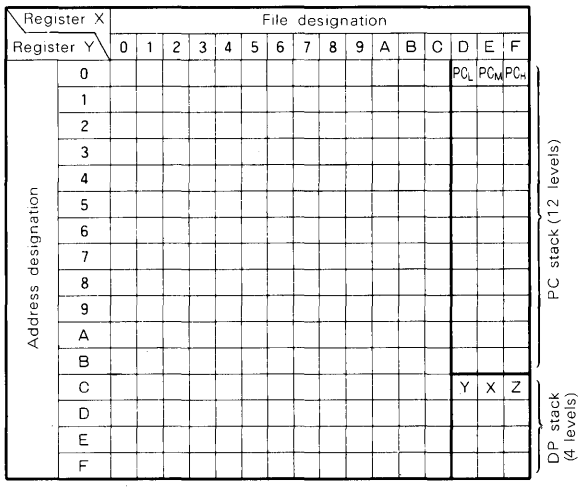


Fig. 1 External basic main memory (Z = 0) and RAM map

Table 1 Address designation of data pointer stack

Value of data field during execution of instructions SDP and LDP		Stack DP (file designated by register Y)
I_1	I_0	
0	0	C
0	1	D
1	0	E
1	1	F

Accumulator (Register A), Carry Flag CY

Register A is an accumulator forming the central unit of a 4-bit-wide microcomputer. Data processing operations such as arithmetic, data transfer, data exchange, data conversion, input/output, etc. are executed principally with this register.

The carry flag CY stores the carry or borrow from the most significant bit of the arithmetic unit in the execution of specific arithmetic instructions, and is available for multipurpose uses as a one-bit flag.

Auxiliary Register (Register B)

Register B is composed of four bits. It is employed for bit operating functions, temporary memory of four-bit data and transfer of eight-bit data when coupled with register A, etc.

Four-Bit Arithmetic Logic Unit (ALU)

This unit carries out four-bit arithmetic and logical functions, and is composed of a four-bit adder and a logic circuit associated with it. It carries out addition, complement conversion, logic arithmetic comparison, arithmetic comparison, bit processing, etc.

General-Purpose Registers Q, R, S, and T

These general-purpose registers comprise a set of four 8-bit shift registers. When using combinations of functions such as serial input, serial output, parallel input and parallel output, by properly selected instructions, they are employed for data transfer between register A and register B, data transfer between output ports or input/output ports, data storage of the data field of the ROM value (8 bits), transmission of internal serial data, receiving of external serial data, etc.

Table 2 Relationship between input/output address N and general-purpose registers

Input/output address	Immediate data N in execution of the instructions BMAB TNAB TPRN and TRPN		General-purpose register to be selected
N	I_1	I_0	
0	0	0	Register Q
1	0	1	Register R
2	1	0	Register S
3	1	1	Register T

Instruction OPI loads one of the four general-purpose registers selected by the input/output address N with the value (8 bits) of the data field. The input/output address N is latched with the contents of the lower 2 bits of the data field in the execution of the instructions BMAB, TNAB, TABN, TPRN and TRPN and determines the register which loads data in the execution of the instruction OPI.

When the general-purpose registers are used as a single 32-bit shift register, four kinds of modes as shown in Table 3 can be set by instruction SMR1.

Mode Register

The mode register is composed of 8 bits, and can select operation modes and functions, etc. of the associated input port or output port by setting or resetting the mode flag corresponding to a bit in register A.

The mode setting by the instruction SMR is shown in Table 4.

The mode setting by instruction SMR1 is shown in Table 5.

Interrupt Function

This microcomputer has a hardware interrupt function for four conditions by one-level. The interrupt requests comprise: the RESET signal; the interrupt request signals INT_A and INT_B as external signals; and the interrupt request signal INT_T by the internal event counter.

The fixed addresses to be jumped to and the priority order of four factors in the interrupt request are defined as follows:

(1) In case of by reset signal RESET page 0, address 0
(2) In case of interrupt signal INT_A page 0, address 2
(3) In case of interrupt signal INT_T page 0, address 8
(4) In case of interrupt signal INT_B page 0, address 4

A RESET signal restores the hardware to the initial state, independent of any current instruction.

In an interrupt enable state, the interrupt is accepted at the rising edge of interrupt request signals INT_A and INT_B. When an interruption is requested in an interrupt disable state, the interrupt is not executed. If the interrupt disable state is removed thereafter and a corresponding interrupt enable instruction is executed, the interrupt routine will be

Table 3 Mode setting by instruction SMR 1; when the general-purpose registers are employed as a 32-bit shift register

Mode flag	SDM	0	0	1	1
	RVM	0	1	0	1
DATA pin		Input	Output	Output	Output
CLK pin		Floating	Input (rising edge trigger)	Output (gernated by timer 2)	Output (generated by shift instruction)
Shift data input	SST, RST	Immediate field data	O input independent of executable instruction	Immediate field data	Immediate field data
	IST	DATA pin output		DATA pin output	DATA pin output
Shift clock pulse		Instructions SST, RST IST	CLK input	Instructions SST, RST, IST	Instructions SST, RST, IST
Transmission receiving		Receiving (only in instruction IST)	Transmission	Transmission	Transmission

executed immediately because the interrupt request has been held in the latch. The current interrupt request, held in a latch during the interrupt disable state, is reset by the interrupt disable instruction.

When two and more interrupt requests of four factors occur simultaneously, the interrupt processing is by order of the highest priority routine. The interrupt request of lower priority order is held in the corresponding latch in an interrupt disable state. When the interrupt disable state is removed by the interrupt enable instruction (after completion of the interrupt process of upper priority order), the interrupt request of next lower priority is initiated.

Table 4 SMR mode setting

Bits of register A	Mode flag (contents of register A are stored)	Status	Function	Mode flag at reset
A_0	IMQ	0	Port Q is used as an 8-bit input port	0
		1	Port Q is used as an 8-bit output port	
A_1	LCD	0	For output port U, only instruction cat set port U.	0
		1	For output port U, instructions TPRN and TPRA for port Q, R, S and T can also set port U.	
A_2	IMR1	0	Port R_1 is used as a 4-bit input port	0
		1	Port R_1 is used as a 4-bit output port	
A_3	IMR2	0	Port R_2 is used as a 4-bit input port	0
		1	Port R_2 is used as a 4-bit output port	

Table 5 SMR 1 mode setting

Bits of register A	Mode flag (contents of register A are stored)	Status	Function	Mode flag at reset
A_0	TMM	0	Event mode, event counter is used with EC input.	0
		1	Timer mode, event counter is used in combination with timer 2.	
A_1	BF	0	All signals (A_{11}~A_0, D_3~D_0, OD and R/W) for external main memory (RAM) are put in floating.	0
		1	All signals (A_{11}~A_0, D_3~D_0, OD and R/W) for external main memory (RAM) are activated.	
A_2	RVM	0	When the general-purpose registers are used as a 32-bit shift register, functions of transmission/receiving, terminals DATA and CLK are employed properly by RVM, SDM flags. For further details, refer to explanation of the general-purpose register.	0
		1		
A_3	SDM	0		0
		1		

Timers and Event Counter

This block is composed of a 14-bit timer 1, a 4-bit timer 2 and a 4-bit event counter.

Timer 1 is a standard timer that continuously counts the frequency X_{IN}, divided by fourteen. The timer performs accurate counting and the period is given by the following formula:

(Fundamental output frequency X_{IN}) x
2^5 (TM_L) x 2^4 (TM_M) x 2^5 (TM_H) = cycle time of timer 1

By the continuous use of instructions TATM and TBTM, the contents of TM_M are stored in register B, the contents of the lower 4 bits of TM_H in register A, and the high-order bit of TM_H in carry flag CY, respectively. The contents of timer 1 can be accessed. Instruction

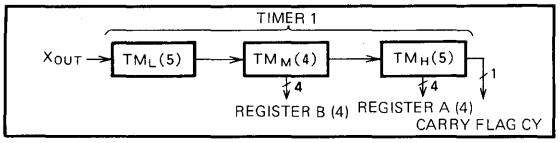
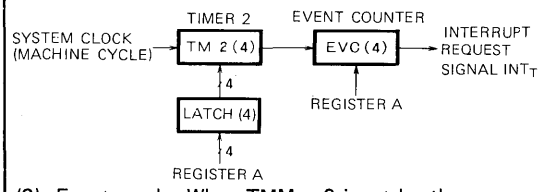


Fig. 2 Outline of timer 1 configuration

RTM clears the contents of timer 1 and resets it to 0.

Timer 2 is composed of a 4-bit counter and a 4-bit latch. The contents of register A are stored as the starting value in the latch and the counter by an STM instruction, whereupon counting down starts in synchronization with each machine cycle. When the contents of the counter become F during countdown, the pre-programmed starting value is restored in the counter from the latch.

(1) Timer mode: When TMM = 1 is set by the instruction SMR1



(2) Event mode: When TMM = 0 is set by the instruction SMR1

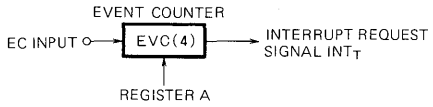


Fig. 3 Outline configuration of timer 2 and event counter

The cycle period of timer 2 is given by the following formula:

Machine cycle x $[1 + (2^0 \sim 2^4)]$

Where the timer mode is set by SMR1 instruction, timer 2 is connected to the event counter. Every time the contents of timer 2 become F the event counter counts down once. For the event counter, the contents of register A can be stored in the counter and used as a starting value by using instruction SEC.

When the event mode is set using instruction SMR1, the event counter is counted down by sensing the rising edge of external event counter input EC.

In both timer mode and event mode, the event counter is counted down from a starting value, and an interrupt request signal is generated when the contents become F.

The time necessary for INT_T generation from the starting value is given by the following formulas:

Timer mode

Machine cycle x $[1 + (2^0 \sim 2^4)] \times (2^0 \sim 2^4)$

Event mode

EC input period x $(2^0 \sim 2^4)$

Reset Function

Applying a low-level input to the RESET input pin for 3 machine cycles or more causes the reset state. Power-on reset is provided by such circuit as shown in Fig. 4.

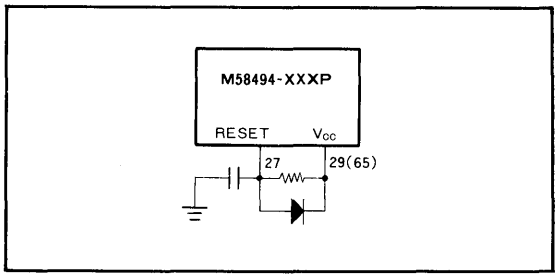


Fig. 4 Power-on reset circuit

Clock Generation Circuit

Clock pulses are easily generated by connecting an external IF ceramic filter between the pins X_{IN} and X_{OUT}. An example of such as circuit is shown in Fig. 5. If the clock signal is to be supplied from an external source, the clock source should be connected to pin X_{IN}, leaving the X_{OUT} pin open. An example of such circuit is shown in Fig. 6.

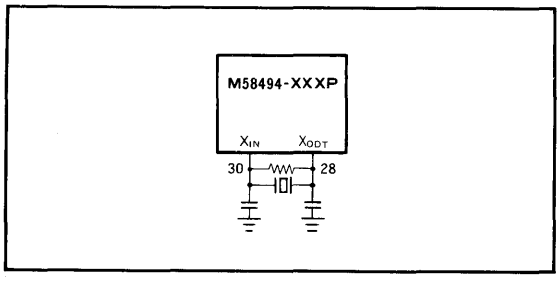


Fig. 5 External oscillation element connections

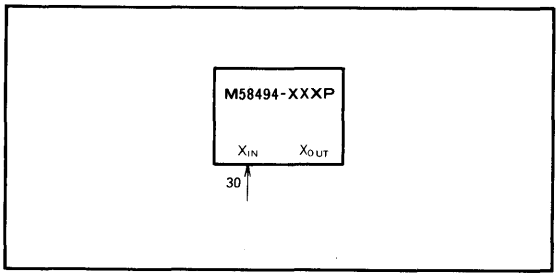


Fig. 6 Exteranl clock input circuit (Note 1)

Note 1. Low and high input levels should be set such that
input level = 0~0.8V
Output level = $V_{CC} \sim (V_{CC} - 0.8)V$
and such that the duty cycle is 40 to 60% with respect to the X_{IN} input.

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MACHINE INSTRUCTIONS

Item: Classification	Symbol	Code: $I_9 I_8 I_7 I_6 I_5 I_4 I_3 I_2 I_1 I_0$	Code: 16 mal notation	No. of words	No. of cycle	Function	Skip conditions	Flag CY
RAM address	**MM**	00 1000 0010	**082**	1	1	(MF)←1, Selects external main memory	—	—
	SM	00 1000 0000	**080**	1	1	(MF)←0, Selects internal scratch-pad memory	—	—
	LY y	01 1000 yyyy	**18y**	1	1	(Y)←y, where y = 0 ~ 15	Consecutively described	—
	LX x	01 1011 xxxx	**1Bx**	1	1	(X)←x, where x = 0 ~ 15	Consecutively described	—
	LZ z	01 1010 zzzz	**1Az**	1	1	(Z)←z, where z = 0 ~ 15	Consecutively described	—
	INY	00 0111 1100	**07C**	1	1	(Y)←(Y)+1	(Y) = 0	—
	DEY	00 0111 1000	**078**	1	1	(Y)←(Y)−1	(Y) = 15	—
	TAY	00 0010 0000	**020**	1	1	(A)←(Y)	—	—
	TAX	00 0010 0010	**022**	1	1	(A)←(X)	—	—
	TAZ	00 0010 0011	**023**	1	1	(A)←(Z)	—	—
	TYA	00 0100 0000	**040**	1	1	(Y)←(A)	—	—
	TXA	00 0100 0010	**042**	1	1	(X)←(A)	—	—
	TZA	00 0100 0011	**043**	1	1	(Z)←(A)	—	—
	SDP j	00 0111 01jj	**074** + j	1	3	(Mj)←(DP), where j = 0 ~ 3	—	—
	LDP j	00 1111 01jj	**0F4** + j	1	3	(DP)←(Mj), where j = 0 ~ 3	—	—
Register-to-register transfer	**TSM**	00 1011 1100	**0BC**	1	1	(SM(DP)) ← (MM(DP))	—	—
	TSMI	00 1111 1100	**0FC**	1	1	(SM(DP)) ← (MM(DP)), (Y)←(Y)+1	(Y) = 0	—
	TMS	00 1011 1110	**0BE**	1	1	(MM(DP)) ← (SM(DP))	—	—
	TMSI	00 1111 1110	**0FE**	1	1	(MM(DP)) ← (SM(DP)), (Y)←(Y)+1	(Y) = 0	—
	TAB	00 1010 0000	**0A0**	1	1	(A)←(B)	—	—
	TBA	00 1100 0000	**0C0**	1	1	(B)←(A)	—	—
	TASP	00 1010 0010	**0A2**	1	1	(A)←(SP)	—	—
	TSPA	00 1100 0010	**0C2**	1	1	(SP)←(A)	—	—
	TACM	00 1000 0100	**084**	1	1	(A)←(N, MF, CY), where $A_{3\sim2}$=N, A_1=MF, A_0=CY	—	—
	TCMA	00 1100 1100	**0CC**	1	1	(N, MF, CY)←(A), where $A_{3\sim2}$=N, A_1=MF, A_0=CY	—	—
Transfer between RAM and accumulator	**TAM j**	00 0010 01jj	**024** + j	1	1	(A)←(M(DP)), (X)←(X)∀j, where, j = 0 ~ 3	—	—
	XAM j	00 0110 01jj	**064** + j	1	1	(A)←→(M(DP)) (X)←(X)∀j, where, j = 0 ~ 3	—	—
	XAMD j	00 0110 10jj	**068** + j	1	1	(A)←→(M(DP)), (Y)←(Y)−1 (X)←(X)∀j, where j = 0 ~ 3	(Y) = 15	—
	XAMI j	00 0110 11jj	**06C** + j	1	1	(A)←→(M(DP)), (Y)←(Y)+1 (X)←(X)∀j, where j = 0 ~ 3	(Y) = 0	—
	XAMD1 j	00 1110 10jj	**0E8** + j	1	1	(A)←→(M(DP)), (Y)←(Y)−1 (X)←(X)∀j, where j = 0 ~ 3	(Y) = 3, 7, 11, 15	—
	XAMI1 j	00 1110 11jj	**0EC** + j	1	1	(A)←→(M(DP)), (Y)←(Y)+1 (X)←(X)∀j, where j = 0 ~ 3	(Y) = 4, 8, 12, 0	—
	TMA	00 0100 0100	**044**	1	1	(M(DP))←(A)		
Arithmetic	**LA n**	01 1001 nnnn	**19n**	1	1	(A)←n, where, n = 0 ~ 15	Consecutively described	—
	AM	00 0110 0000	**060**	1	1	(A)←(A)+(M(DP))	—	—
	AMC	00 0110 0010	**062**	1	1	(A)←(A)+(M(DP))+(CY), (CY)← Carry	—	0/1
	AMCS	00 0110 0011	**063**	1	1	(A)←(A)+(M(DP))+(CY), (CY)← Carry	Carry = 1	0/1
	A n	00 0101 nnnn	**05n**	1	1	(A)←(A)+n, where, n = 0 ~ 15	Carry = 0	—
	SC	00 1000 1010	**08A**	1	1	(CY)←1	—	1
	RC	00 1000 1000	**088**	1	1	(CY)←0	—	0
	SZC	00 1011 1000	**0B8**	1	1		(CY) = 0	—
	CMA	00 1011 1010	**0BA**	1	1	(A)←($\overline{A}$)	—	—

Item / Classification	Symbol	Code $I_9 I_8 I_7 I_6 I_5 I_4 I_3 I_2 I_1 I_0$	16 mal notation	No. of words	No. of cycle	Function	Skip condition	Flag CY
Bit manipulation	SB j	00 1000 11jj	08C + j	1	1	$(B(j)) \leftarrow 1$, where, $j = 0 \sim 3$	—	—
	RB j	00 1010 11jj	0AC + j	1	1	$(B(j)) \leftarrow 0$, where, $j = 0 \sim 3$	—	—
	SZB j	00 0011 10jj	038 + j	1	1		$(B(j)) = 0$ where, $j = 0 \sim 3$	—
	SZM j	00 0000 01jj	004 + j	1	1		$(M_j(DP)) = 0$ where, $j = 0 \sim 3$	—
Compare	SEAM	00 1110 0000	0E0	1	1		$(A) = (M(DP))$	—
	SEY n	00 0001 nnnn	01n	1	1		$(Y) = n$ where, $n = 0 \sim 15$	—
	SEI n	00 1001 nnnn	09n	1	1		$(A) = n$ where, $n = 0 \sim 15$	—
Branch	B xy	01 0xxx yyyy	1xy	1	1	$(PC_L) \leftarrow y$, $(PC_M) \leftarrow x$ where $16x + y = 0 \sim 127$	—	—
	BL xy	11 0xxx yyyy	3xy	1	1	$(PC_L) \leftarrow y$, $(PC_M) \leftarrow (P_0, x)$, $(PC_H) \leftarrow (P_4, P_3, P_2, P_1)$ where $16x + y = 0 \sim 127$	—	—
	BA i	00 1101 0iii	0Di	1	1	$(PC_L) \leftarrow (A_0, i)$ where, $i = 0 \sim 7$; $(PC_M) \leftarrow (P_0, A_3, A_2, A_1)$; $(PC_H) \leftarrow (P_4, P_3, P_2, P_1)$	—	—
	BMAB r	00 1100 10rr	0C8 + r	1	1	$(PC_L) \leftarrow (A)$, $(PC_M) \leftarrow (B)$, $(PC_H) \leftarrow (P_4, P_3, P_2, P_1)$ but returns unconditionally after one machine cycle. Input/output address $r = 0 \sim 3$ designates general-purpose register	—	—
	LP p	01 110p pppp	1CP + p	1	1	$(P) \leftarrow p$ where, $p = 0 \sim 31$	Consecutively described	—
	TPAC	00 1100 0100	0C4	1	1	$(P) \leftarrow (CY, A)$	—	—
	TACP	00 1010 0100	0A4	1	1	$(CY, A) \leftarrow (P)$	—	—
Subroutine call	BM xy	11 1xxx yyyy	38y + x	1	3	$(PC_L) \leftarrow y$, $(PC_M) \leftarrow (P_0, x)$, where $16x + y = 0 \sim 127$, $(PC_H) \leftarrow (P_4, P_3, P_2, P_1)$, $(M(SP)) \leftarrow (PC)$, $(SP) \leftarrow (SP) + 1$	—	—
	BMA i	00 1101 1iii	0D8 + i	1	3	$(PC_L) \leftarrow (A_0, i)$, where, $j = 0 \sim 7$; $(PC_M) \leftarrow (P_0, A_3, A_2, A_1)$; $(PC_H) \leftarrow (P_4, P_3, P_2, P_1)$; $(M(SP)) \leftarrow (PC)$; $(SP) \leftarrow (SP) + 1$	—	—
Return	RT	00 1111 1000	0F8	1	3	$(PC) \leftarrow (M(SP))$, $(SP) \leftarrow (SP) - 1$	—	—
	RTS	00 1111 1010	0FA	1	4	$(PC) \leftarrow (M(SP))$, $(SP) \leftarrow (SP) - 1$, $(PC) \leftarrow (PC) + 1$	Unconditionally	—
	RTI	00 1111 1001	0F9	1	3	$(PC) \leftarrow (M(SP))$, $(SP) \leftarrow (SP) - 1$	—	—

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Item / Classification	Symbol	Code $I_9 I_8$ $I_7 I_6 I_5 I_4$ $I_3 I_2 I_1 I_0$	16 mal notation	No. of works	No. of cycle	Function	Skip conditions	Flag CY
Interrupt flip-flop control	**EIA**	00 0000 1001	009	1	1	Enables interruption of INT_A signal.	—	—
	EIB	00 0000 1010	00A	1	1	Enables interruption of INT_B signal.	—	—
	EIAB	00 0000 1011	00B	1	1	Enables interruption of INT_A and INT_B signals.	—	—
	EIT	00 0000 1000	008	1	1	Enables interruption of INT_T signal.	—	—
	DIA	00 0000 1101	00D	1	1	Disables interruption of INT_A signal.	—	—
	DIB	00 0000 1110	00E	1	1	Disables interruption of INT_B signal.	—	—
	DIAB	00 0000 1111	00F	1	1	Disables interruption of INT_A and INT_B signals.	—	—
	DIT	00 0000 1100	00C	1	1	Disables interruption of INT_T signal.	—	—
Timer	**TBTM**	00 0010 1111	02F	1	1	$(B) \leftarrow (TM_M)$	—	—
	TATM	00 1010 0111	0A7	1	1	$(A) \leftarrow (TM_{H3}, TM_{H2}, TM_{H1}, TM_{H0})$ $(CY) \leftarrow (TM_{H4})$		
	RTM	00 1011 0100	0B4	1	1	$(TM_L) \leftarrow 0$, $(TM_M) \leftarrow 0$, $(TM_H) \leftarrow 0$	—	—
	STM	00 1100 0111	0C7	1	1	$(TM2) \leftarrow (A)$	—	—
	SEC	00 1100 0110	0C6	1	1	$(EVC) \leftarrow (A)$	—	—
Input/output	**ID**	00 0010 1110	02E	1	1	$(B) \leftarrow (D)$, $(OD) \leftarrow$ "L"	—	—
	OD	00 0100 1100	04C	1	1	$(D) \leftarrow (B)$, $(R/W) \leftarrow$ "L"	—	—
	OPI s	10 ssss ssss	2ss	1	1	$(R(r)) \leftarrow s$	—	—
	TNAB r	00 0100 10rr	048 + r	1	1	$(R(r)) \leftarrow (A, B)$ where the general-purpose register is designated with r = 0 ~ 3	—	—
	TABN r	00 0010 10rr	028 + r	1	1	$(A, B) \leftarrow (R(r))$ where the general-purpose register is designated with r = 0 ~ 3	—	—
	IQ	00 1010 1000	0A8	1	1	$(A, B) \leftarrow (P(Q))$	—	—
	IR1	00 0010 1100	02C	1	1	$(B) \leftarrow (P(R_1))$	—	—
	IR2	00 0010 1101	02D	1	1	$(B) \leftarrow (P(R_2))$	—	—
Input/output control	**SMR**	00 0011 0100	034	1	1	$(MR) \leftarrow (A)$	—	—
	SMR1	00 0011 0110	036	1	1	$(MR1) \leftarrow (A)$	—	—
	SST	00 0011 1100	03C	1	1	$(R(Q_0)) \leftarrow 1$, R(All) ← 1-bit shift R (All)	—	—
	RST	00 0011 1101	03D	1	1	$(R(Q_0)) \leftarrow 0$, R(All) ← 1-bit shift R (All)	—	—
	IST	00 0011 1110	03E	1	1	$(R(Q_0)) \leftarrow$ (DATA), R(All) ← 1-bit shift R (All)	—	—
	SU	00 0100 1110	04E	1	1	$(U) \leftarrow (A, B)$	—	—
	CLP	00 0000 0001	001	1	1	$(P(All)) \leftarrow 0$	—	—
	TPRA	00 1011 0000	0B0	1	1	$(P(All)) \leftarrow (R(All))$	—	—
	TPRN r	00 1111 00rr	0Fr	1	1	$(P(r)) \leftarrow (R(r))$	—	—
	TRPN r	00 0111 00rr	07r	1	1	$(R(r)) \leftarrow (P(r))$	—	—
Others	**NOP**	00 0000 0000	000	1	1	No operation	—	—

Symbol	Details	Symbol	Details
A	4-bit register (accumlator)	$P(R_2)$	4-bit port R_2
A_i	Indicates the bits of register A. Where i = 0 ~ 3	P(Q)	8-bit port Q
B	4-bit auxiliary register	R(All)	Indicates all the 8-bit registers. Q, R, S, T (32-bit)
B(j)	The bit of register B addressed when j = 0 ~ 3		
CY	1-bit carry flag	R(r)	The register selected by r (r corresponds with registers Q, R, S, and T where r = 0 ~ 3)
D	4-bit input/output port (3-state)		
DATA	1-bit input/output port for serial data	$R(Q_0)$	1st bit of register Q
DP	12-bit data pointer composed of registers X, Y and Z	R/W	1-bit output port which is used for the write signal of the external main memory
EVC	4-bit event counter		
M(DP)	4-bit data memory addressed by the data pointer DP	SM(DP)	The 4-bit internal scratch-pad memory addressed by the data pointer DP
Mj	12-bit data from the scratch-pad memory addressed by i = 0 ~ 3 (data pointer number in the fixed area)	SP	4-bit stack pointer
		TMI	14-bit counter composed of TM_L, TM_M and TM_H counters
Mj (DP)	4-bit data from external memory addressed by the contents data pointer DP, where j = 0 ~ 3	TML	5-bit counter
		TM_M	4-bit counter
MF	1-bit flat for selection of internal scratch-pad memory (MF ← Q at instruction SM) or external main memory (MF ← 1 at instruction MM)	TM_H	5-bit counter
		TM_{H_i}	Indicates the bit of TM_H counter, where i = 0 ~ 4
		TM2	4-bit counter
MM(DP)	4-bit external main memory data addressed by the data pointer DP	U	4-bit output port (3-state)
		X	4-bit register where X = 0 ~ 15, addressing the field of 16 words by 4 bits per file.
M(SP)	12-bit data from external memory addressed by the stack pointer SP (return address stored in the fixed area)		
MR	4-bit mode flag (IMQ, LCD, IMR1, IMR2)	Y	4-bit register where Y = 0 ~ 15, which addresses the word unit of 16 words by 4 bits.
MR1	4-bit mode flag (TMM, BF, RVM, SDM)		
r	Input/output address to select one of the general-purpose registers Q, R, S and T (r = 0 ~ 3)	Z	4-bit register where Z = 0 ~ 15, which addresses 16 files x 16 words x 4 bits
OD	1-bit output port used for the read signal for external main memory		
		iii	3-bit binary variable
P	5-bit page register	jj	2-bit binary constant
P_i	Indicates the bits of register P, where i = 0 ~ 4	nnnn	4-bit binary constant
PC	12-bit program counter composed of counters PC_L, PC_M and PC_H	ppppp	5-bit binary constant
		rr	2-bit binary constant
PC_L	4-bit counter	ssss ssss	8-bit binary constant
PC_M	4-bit counter	xxxx	4-bit binary variable
PC_H	4-bit counter	yyyy	4-bit binary variable
P(All)	Indicates all the 8-bit ports. Q, R, S, T (32-bit)	zzzz	4-bit binary variable
P(r)	The port selected by r (corresponds with ports Q, R, S, and T at r = 0 ~ 3)		
$P(R_1)$	4-bit port R_1		

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INSTRUCTION CODE LIST

$I_9 \sim I_4$ / 16 mal notation / $I_3 \sim I_0$		00 0000	00 0001	00 0010	00 0011	00 0100	00 0101	00 0110	00 0111	00 1000	00 1001	00 1010	00 1011	00 1100	00 1101	00 1110	00 1111	01 0000 ∫ 01 0111	01 1000	01 1001	01 1010	01 1011	01 1100 ∫ 01 1101	01 1110 ∫ 01 1111	10 0000 ∫ 10 1111	11 0000 ∫ 11 0111	11 1000 ∫ 11 1111
		00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10~17	18	19	1A	1B	1C~1D	1E~1F	20~2F	30~37	38~3F
0000	0	NOP	SEY 0	TAY	—	TYA	A 0	AM	TRPN 0	SM	SEI 0	TAB	TPRA	TBA	BA 0	SEAM	TPRN 0	B	LY 0	LA 0	LZ 0	LX 0	LP	—	OPI	BL	BM
0001	1	CLP	SEY 1	*	—	*	A 1	*	TRPN 1	*	SEI 1	*	*	*	BA 1	*	TPRN 1	B	LY 1	LA 1	LZ 1	LX 1	LP	—	OPI	BL	BM
0010	2	—	SEY 2	TAX	—	TXA	A 2	AMC	TRPN 2	MM	SEI 2	TASP	*	TSPA	BA 2	*	TPRN 2	B	LY 2	LA 2	LZ 2	LX 2	LP	—	OPI	BL	BM
0011	3	—	SEY 3	TAZ	—	TZA	A 3	AMCS	TRPN 3	*	SEI 3	*	*	*	BA 3	*	TPRN 3	B	LY 3	LA 3	LZ 3	LX 3	LP	-	OPI	BL	BM
0100	4	SZM 0	SEY 4	TAM 0	SMR	TMA	A 4	XAM 0	SDP 0	TACM	SEI 4	TACP	RTM	TPAC	BA 4	—	LDP 0	B	LY 4	LA 4	LZ 4	LX 4	LP	—	OPI	BL	BM
0101	5	SZM 1	SEY 5	TAM 1	*	*	A 5	XAM 1	SDP 1	*	SEI 5	*	*	*	BA 5	—	LDP 1	B	LY 5	LA 5	LZ 5	LX 5	LP	—	OPI	BL	BM
0110	6	SZM 2	SEY 6	TAM 2	SMR1	*	A 6	XAM 2	SDP 2	*	SEI 6	—	—	SEC	BA 6	—	LDP 2	B	LY 6	LA 6	LZ 6	LX 6	LP	—	OPI	BL	BM
0111	7	SZM 3	SEY 7	TAM 3	*	*	A 7	XAM 3	SDP 3	*	SEI 7	TATM	—	STM	BA 7	—	LDP 3	B	LY 7	LA 7	LZ 7	LX 7	LP	—	OPI	BL	BM
1000	8	EIT	SEY 8	TABN 0	SZB 0	TNAB 0	A 8	XAMD 0	DEY	RC	SEI 8	IQ	SZC	BMAB 0	BMA 0	XAMD1 0	RT	B	LY 8	LA 8	LZ 8	LX 8	LP	—	OPI	BL	BM
1001	9	EIA	SEY 9	TABN 1	SZB 1	TNAB 1	A 9	XAMD 1	*	*	SEI 9	*	*	BMAB 1	BMA 1	XAMD1 1	RTI	B	LY 9	LA 9	LZ 9	LX 9	LP	—	OPI	BL	BM
1010	A	EIB	SEY 10	TABN 2	SZB 2	TNAB 2	A 10	XAMD 2	*	SC	SEI 10	*	CMA	BMAB 2	BMA 2	XAMD1 2	RTS	B	LY 10	LA 10	LZ 10	LX 10	LP	—	OPI	BL	BM
1011	B	EIAB	SEY 11	TABN 3	SZB 3	TNAB 3	A 11	XAMD 3	*	*	SEI 11	*	*	BMAB 3	BMA 3	XAMD1 3	*	B	LY 11	LA 11	LZ 11	LX 11	LP	—	OPI	BL	BM
1100	C	DIT	SEY 12	IR1	SST	OD	A 12	XAMI 0	INY	SB 0	SEI 12	RB 0	TSM	TCMA	BMA 4	XAMI1 0	TSMI	B	LY 12	LA 12	LZ 12	LX 12	LP	—	OPI	BL	BM
1101	D	DIA	SEY 13	IR2	RST	*	A 13	XAMI 1	*	SB 1	SEI 13	RB 1	*	*	BMA 5	XAMI1 1	*	B	LY 13	LA 13	LZ 13	LX 13	LP	—	OPI	BL	BM
1110	E	DIB	SEY 14	ID	IST	SU	A 14	XAMI 2	*	SB 2	SEI 14	RB 2	TMS	*	BMA 6	XAMI1 2	TMSI	B	LY 14	LA 14	LZ 14	LX 14	LP	—	OPI	BL	BM
1111	F	DIAB	SEY 15	TBTM	*	*	A 15	XAMI 3	*	SB 3	SEI 15	RB 3	*	*	BMA 7	XAMI1 3	*	B	LY 15	LA 15	LZ 15	LX 15	LP	—	OPI	BL	BM

Note: $I_3 \sim I_0$ indicate the low-order 4 bits of the machine code and $I_9 \sim I_4$ show the high-order 6 bits Hexadecimal expressions of the codes are also given. All instructions are one word.

* — : Do not use these codes.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−0.3~6.0	V
V_I	Input voltage		−0.3~V_{CC}+0.3	V
V_O	Output voltage		0~V_{CC}	V
Pd	Power dissipation	Ta=25℃	300	mW
Topr	Operating free-air temperature range		0~50	℃
Tstg	Storage temperature range		−40~125	℃

RECOMMENDED OPERATING CONDITIONS (T_a = 0~50°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	V_{CC}−0.8		V_{CC}	V
V_{IL}	Low-level input voltage	0		0.8	V
$f(\phi)_1$	Internal clock oscillation frequency (Delay time is not taken into account by external RAM)	100		455	kHz
$f(\phi)_2$	Internal clock oscillation frequency (Standard external RAM is connected)	100		350	kHz
$D(\phi)$	Clock duty cycle	40	50	60	%

ELECTRICAL CHARACTERISTICS (T_a = 0~50°C, V_{CC} = 5V ±10%, V_{SS} = 0V, f(φ) = 100~455kHz)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{OH}	High-level output current	V_{OH}=(V_{CC}−0.8)V	−0.36			mA
I_{OL}	Low-level output current	V_{OL}=0.8V			0.36	mA
I_{CC}	Supply current from V_{CC}	f=455kHz, V_{CC}=5V Ta=25℃ Clock input applied from the external		0.4	1	mA

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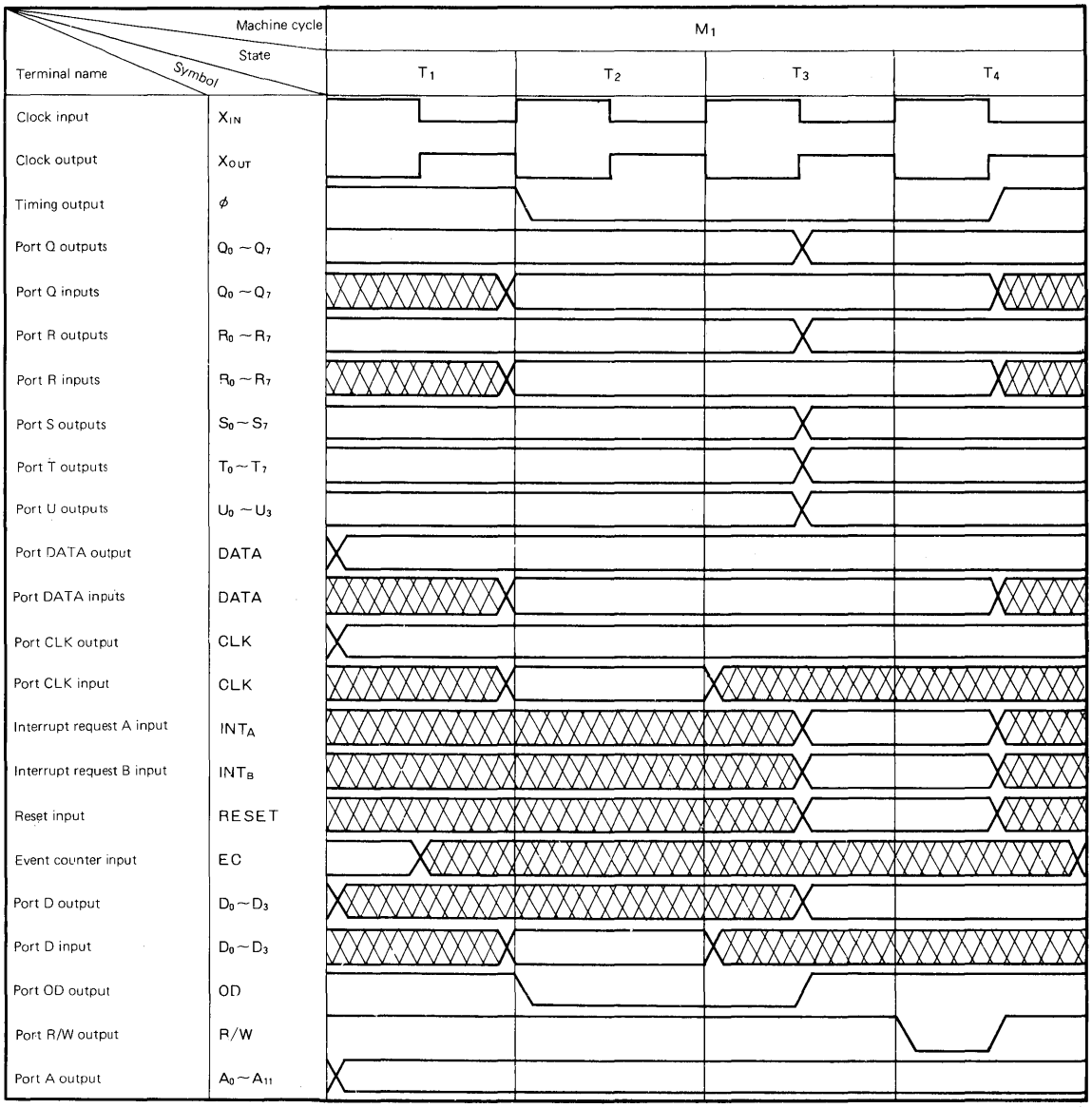
BASIC TIMING DIAGRAM



Note: ▨ The crosshatched area indicates invalid input.

M58496-XXXP

SINGLE-CHIP 4-BIT CMOS MICROCOMPUTER

DESCRIPTION

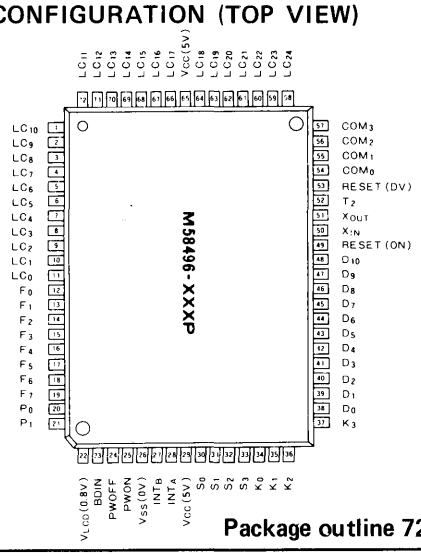
The M58496-XXXP is a single-chip 4-bit microcomputer fabricated using CMOS technology. Its features are liquid crystal display direct drive circuit, current saving circuit for back-up of a 22-stage frequency divider and RAM.

This device is designed for applications in which clock and liquid crystal display functions are included and where the low-power dissipation achieved by CMOS is especially important.

FEATURES

- Single 5V power supply
- Basic machine instructions 77
- Basic instruction execution time
  (at 4.2MHz liquid crystal frequency) 7.7μs
- Memory capacity: ROM . . . . . 2048 words x 10 bits
  Internal RAM . . 128 words x 4 bits
  External RAM . . 256 words x 4 bits
- Internal crystal oscillation circuit
- Internal 22-stage frequency divider
- Low voltage detector circuit
- Internal current saving circuit while idling
- Subroutine nesting . . . . . 3 levels
  Internal timer: Prescaler . . . 7 bits Timer . . . 4 bits
- Output ports for liquid crystal display
  segment signal (port LC) . . . . . 25 bits
  common signal (port COM) . . . . . 4 bits
- I/O Ports (ports K and S) . . . . . 4 bits x 2
- Output port (port D) . . . . . 1 bit x 11

PIN CONFIGURATION (TOP VIEW)



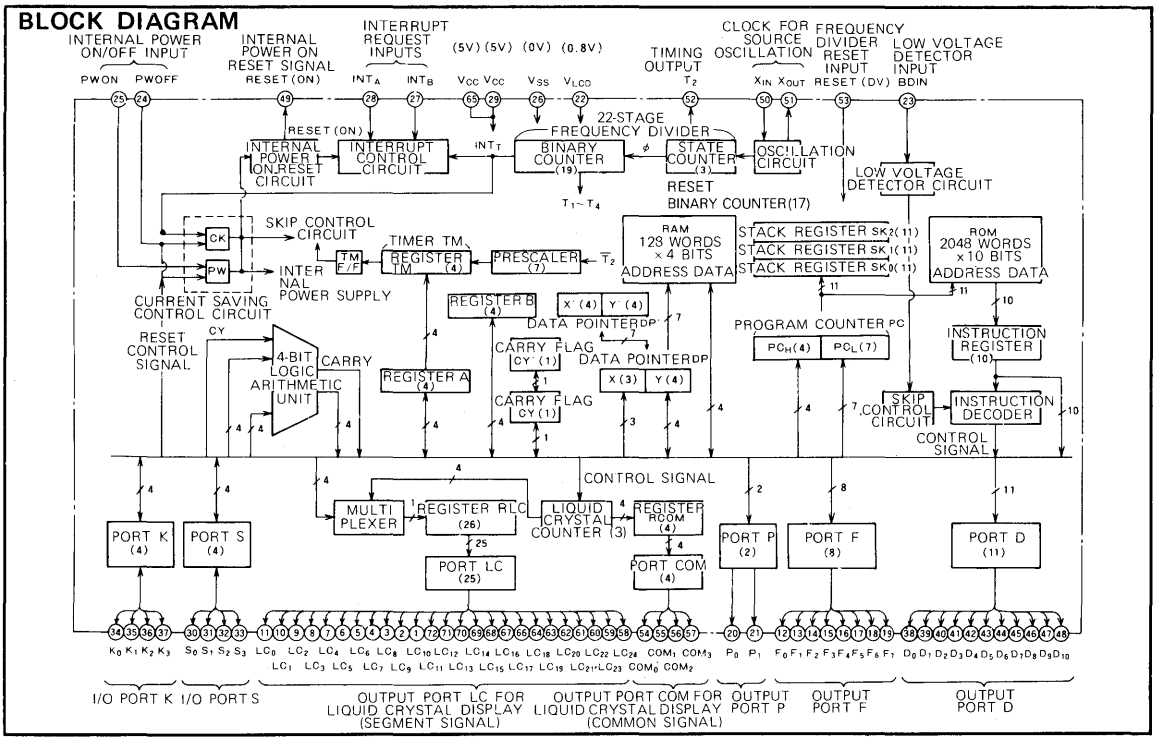
Package outline 72P2

- Output port (port F) . . . . . 1 bit x 8
- Output port (port P) . . . . . 1 bit x 2
- Interrupt function . . . . . 4 factors, 1 level

APPLICATIONS

- Electronic cash registers and calculators with printer
- Office machines, intelligent terminals and data terminals
- Electronic Games
- Electronic coin and changer machines
- Sewing machines

BLOCK DIAGRAM



SINGLE-CHIP 4-BIT CMOS MICROCOMPUTER

FUNCTION

The M58496-XXXP consists of mask ROM and RAM, a 4-bit arithmetic logic unit, crystal oscillation circuit, 22-stage frequency divider, power saving circuit, low voltage detector circuit, 4-bit timer, interrupt circuit and a liquid crystal display direct drive circuit. The RAM capacity can easily be expanded by the external connection of 256-word by 4-bit CMOS RAM.

The ROM storage is organized as 16 pages of 128 words which is used mainly for programs. Addressing the ROM is done through the program counter. The address register is structured as a 7-bit address register and a 4-bit page register. The address register is counted up as nonbranching instructions are executed. When a nonbranching instruction at address 127 on a page is executed an overflow of the address register is produced. This carry (overflow) is disregarded so the page register is not counted up and the next instruction to be executed will come from address 0 on the same page.

When an interrupt request is accepted control is transferred to fixed addresses as follows: in case of an internal power on reset signal (RESET(ON)) the program is set to page 0 address 0, for the INT_A signal it is set to page 0 address 2, for the INT_B signal it is set to page 0 address 4 and for the output signal INT_T(second signal) of the 22-stage frequency divider it is set to page 0 address 8.

The internal RAM which is configured as 8 files of 16 words is used for data storage and each word can be addressed. The internal RAM is addressed by a 7-bit data pointer. The internal RAM can be augmented by external RAM consisting of up to 16 files of 16 words. The external RAM is addressed by the 8-bit combined register Y (4 bits) and register B (4 bits).

RAM addressing, register-to-register transfers, RAM-to-accumulator transfers, arithmetic operations, input/output operations and timer operation are performed mainly through register A (accumulator).

The current saving circuit used in conjunction with the 22-stage frequency divider and RAM can be controlled by the PWOFF input and instruction.

The low voltage detector circuit is also active while the power source is a battery. Low voltage is sensed by the program and an indication can be output.

The output ports for direct drive of the liquid crystal display are port LC (25 terminals) and port COM (4 terminals). The liquid crystal display can be driven by 1/4 duty, 1/3 bias or 1/3 duty, 1/3 bias.

Output port D consists of 11 individually latched bits that can be used to output not only 1-bit data but can also output data such as the contents of register Y of the data pointer and 8-bit addresses for external RAM.

Output port F consists of 8 individually latched bits that can be used to output data. It can be set or reset by instructions.

Output port P consists of 2 terminals through which a synchronous signal of 1 machine cycle width can be output by instruction.

The combined 7-bit output of ports F and P can be used to directly fetch the contents of ROM addressed by the data field of an instruction.

The I/O ports K and S consist of 4 terminals through which data can be transferred to and from register A.

PERFORMANCE SPECIFICATIONS

Item			Performance
Number of basic instructions			77
Execution time of basic instructions			7.7μs (V_{CC}=5V, f=4.1943MHz)
Clock frequency			250~525kHz
Memory Capacity	ROM		2048 words x 10 bits
	Internal RAM		128 words x 4 bits
	External RAM		256 words x 4 bits
I/O Port	LC	Liquid crystal display output	25 x 1 bit
	COM		4 bits
	K	Input	4 bits
		Output	4 bits (Note 1)
	S	Input	4 bits
		Output	4 bits (Note 1)
	D	Output	11x 1 bit (open drain)
	F	Output	8 x 1 bit (Note 1)
	P	Output	2 x 1 bit (Note 1)
Frequency divider			22-stage built in
Current saving circuit			Built in
Low voltage detector			Built in
Subroutine nesting			3 levels (including 1 level of interrupt)
Interrupt request			4 factors, 1 level
Clock generation circuit			Built in (4.1943 MHz crystal oscillator external) (Note 2)
Input/output port	Output voltage		6V (max)
	Output current		-0.4 mA (min.)
Power supply voltage	V_{CC}		5V (nom)
	V_{SS}		0V
Liquid crystal display driving supply voltage			0.8V (nom)
Element structure			CMOS
Package			72-pin plastic molded flat package
Power dissipation (open output terminals)	In operation		5mW (V_{CC}=5V, 525 kHz)
	In idle		1.5mW (V_{CC}=5V, 525 kHz)

Note 1: Ports K, S, F, and P are connected to high-impedance pull-down resistors. When high-driving current is required, external resistors are required.

2: External oscillator can be selected by mask option.
(1) 4.1943 MHz crystal oscillator
(2) 455 kHz ceramic oscillator

PIN DESCRIPTION

Pin	Name	Input or output	At reset (internal power-on)	Function
X_{IN}	Source oscillation clock input	Input	—	Incorporates the clock oscillation circuit, for setting the frequency. An oscillation reference device such as a crystal oscillator is connected between X_{IN} and X_{OUT}. When an external clock is used, connect the clock oscillation source to the X_{IN} pin and leave the X_{OUT} pin open.
X_{OUT}	Source oscillation clock output	Output	—	
PWON	Internal power on input	Input	—	Incorporates the power saving circuit. Its control inputs are PWON and PWOFF. The 22-stage frequency divider and RAM are put in the idle state by a PWOFF input.
PWOFF	Internal power off input	Input	Low level	
RESET (DV)	Frequency divider reset input	Input	—	Incorporates the 22-stage frequency divider as the crystal oscillation reference device. This is a reset input for up to lower 17 steps of the divider.
BDIN	Low voltage detector input	Input	—	The low voltage detector circuit is built in. A resistor should be connected to the BDIN pin for voltage sensing.
INT_A	Interrupt request A signal	Input	Interrupt disable	This input signal is for an interrupt request. The request is accepted on the rising edge of the signal. Besides these external input signals, an interrupt request INT_T from the 22-stage frequency divider output signal is sensed as an interrupt.
INT_B	Interrupt request B signal	Input	Interrupt disable	
$LC_0 \sim LC_{24}$	Liquid crystal display segment output	Output	—	Incorporates the liquid crystal display direct drive circuit. It is suitable for liquid crystal display at 1/4 duty and 1/3 bias. The output ports for direct drive of the liquid crystal display are port LC ($LC_0 \sim LC_{24}$) and port COM ($COM_0 \sim COM_3$).
$COM_0 \sim COM_3$	Liquid crystal display common output	Output	—	
V_{LCD}	Power supply for liquid crystal display	—	—	This is the power supply terminal for a liquid crystal display. It includes the bias resistor for the segment and common signals.
$D_0 \sim D_{10}$	Output port D	Output	Floating	This output port consists of 11 bits. Each output is individually latched and can be selected to be set or reset by the contents of register Y. Also 8 bits of the port can be used to fetch 8-bit addresses for external RAM.
$F_0 \sim F_7$	Output port F	Output	Low level	The output port consists of 8 bits. Each output is individually latched and can be set or reset by instructions.
P_0, P_1	Output port P	Output	Low level	This output port consists of 2 bits from which 1 synchronous signal of 1 machine cycle width can be output per instruction. The immediate 7-bit field of an instruction can be output through this port in combination with 5 bits of port F.
$K_0 \sim K_3$	Input/output port K	Input/output	Low level	Ports K and S are 4-bit latched input/output ports through which data can be transferred to and from register A. When output is low-level the output will be high-impedance so it can be used as an input port.
$S_0 \sim S_3$	Input/output S	Input/output	Low level	
T_2	Timing output	Output	—	The timing output is used for testing the device.
RESET (ON)	Internal power-on reset signal	Output	Low level	When the internal power supply is switched on, a built in automatic reset circuit generates a high-level reset signal that resets the I/O ports.

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DESCRIPTION OF OPERATION

Program Counter PC

The program counter is an 11-bit address register. The high-order 4 bits designate the page number and as a group are called PC_H. The low-order 7 bits designate the address on the page and as a group are called PC_L. The PC designates the address of the 2048 words by 10-bit mask-programmable ROM. The ROM is organized into 16 pages of 128 words. As instructions are fetched from ROM, PC_L is incremented so that unless there is a branch executed instructions are fetched and executed in sequence. Care must be taken when the last instruction on a page (address 127) is executed because when PC_L is incremented it becomes zero with a carry, but the carry is disregarded so the next instruction to be fetched will be the start of the same page. Therefore to move to the next page PC_H must modified by using branch instructions such as BL, BML, BLA and BMLA.

Pages 14 and 15 are special pages designed to accommodate subroutines. Subroutines starting on page 14 can be called by 1-word instructions BM or BMA. These instructions automatically load PC_H to designate page 14 and in addition the return address and control status are saved so they can be restored when the subroutine transfers control back to the main program. If the instructions BM or BMA are executed on page 14, they execute a branch within page 14 without saving any information. If the instructions B or BA are executed on page 14, they execute a branch to page 15.

Stack Registers SK_0, SK_1, SK_2

The 3-level stack register consists of 11-bit registers for storing the contents of the program counter when control is transferred from the main program to a subroutine or interrupt. When control is transferred back to the main program, the PC can be restored. There are 3 levels, but when 1 level is saved for interrupts it leaves 2 levels for subroutine nesting.

Data Pointers DP, DP'

The data pointer is a 7-bit register used to designate the address of RAM or the bit position of output port D. The data pointer is composed of the 3-bit register X and the 4-bit register Y. Internal RAM is organized as 8 files of 16 words. Register X designates the file and register Y designates the word position of a file or the bit position of output port D.

The data pointer DP' is selected by software during interrupt processing to leave the contents of DP unchanged (saves the DP).

External RAM is organized as 16 files of 16 words that can be added to the system to expand memory. Register Y designates the word position of a file while register B designates the file.

Register A (accumulator) and Carry Flags CY, CY'

Register A is the 4-bit accumulator forming the heart of the 4-bit microcomputer. Data processing operations such as arithmetic, transfer, exchange, conversion, and input/output are executed principally through this register.

The carry flags CY are to store the carry or borrow from the most significant bit of the arithmetic unit resulting from executing the various instructions. It can be tested and used for various purposes. In principle it acts as a 1-bit flag.

The carry flag CY' is selected by software to leave the contents of CY unchanged (saves the CY).

Register B (Auxiliary Register)

Register B is a 4-bit register used for temporary storage of 4-bit data. It also is used to designate the file number of external RAM.

Arithmetic Logic Unit (ALU)

The arithmetic logic unit performs 4-bit arithmetic and logical operations. The heart of the ALU is a 4-bit adder and the logic circuit associated with it. It performs operations such as additions, complement conversions, logic arithmetic comparisons and bit processing.

Frequency Divider and Timer

The frequency divider divides the basic oscillation frequency into 22 stages. It is connected to the basic oscillation device through X_{IN} and X_{OUT}. The frequency divider generates the interrupt request signal INT_T to the interrupt control circuit. The frequency divider sets flag CK for controlling the power saving circuit.

Basic oscillation for the timer is the timing signal T_2. The timer is composed of a 7-bit prescaler and a 4-bit counter. Timer flag TMF/F is set when a timer overflows, and is sensed by the TTM instruction. The 4-bit timer counter is set by the STM instruction. Prescaler and timer flag are reset at the same time.

Power Saving Circuit

The power saving circuit is controlled by the CK flag and PW. Its output is input to the internal power supply reset circuit and generates an interrupt request signal RESET (ON). Control is transferred unconditionally to address 0 on page 0 and resets the I/O ports. The interrupt request

signal RESET (ON) generates on the rising edge of internal power supply on reset output. Internal power supply is switched off by the external terminal and stop instruction, but power is maintained to the following circuits:

1. Internal data memory (RAM)
2. Clock oscillation circuit
3. 22-stage frequency divider
4. Low voltage detector circuit
5. Power saving circuit

Low Voltage Detector Circuit

The low voltage detector circuit connects the resistor for sensing voltage to the BDIN terminal. A falling voltage level is sensed by the program and can be displayed by using apt output port.

Interrupt Functions

The M58496-XXXP has internal circuits to process interrupt requests from 4 single level sources. The 4 interrupt request sources are external interrupt signals INT_A and INT_B, internal power supply reset output RESET (ON), output INT_T from the 22-stage frequency divider. Interrupt requests INT_A, INT_B and INT_T are enabled by the instructions EIA, EIB and EIT respectively and disabled by the instruction DIA, DIB and DIT respectively. Interrupt requests from the internal power supply through reset output RESET (ON) cannot be disabled and will cause an interrupt whenever received.

During the interrupt enable state an interrupt request by INT_A or INT_B is accepted on the rising edge of the signal. When an interrupt request is received during the interrupt disable state it is latched, but is not executed. When the disable is removed thereafter by executing the corresponding interrupt enable instruction, the interrupt request will be accepted immediately and control transferred to the interrupt routine because the request was latched. A current interrupt request, held by latching during interrupt disable state is reset when the corresponding interrupt disable instruction is executed.

One level of the 3-level stack register is required when interrupt programs are used. This leaves 2 levels available for subroutine processing. After an interrupt is processed control is returned to the main program by executing a return instruction such as RTI. Care must be taken after starting an interrupt program to save the contents the data pointer DP, register A, carry flag and any other registers used, so the contents can be restored before returning to the main program. The contents must be saved and restored by the interrupt program.

When an interrupt request is accepted the program counter, interrupt enable flag and skip flag are affected as follows:

(1) Program counter
The contents (the current program address) are stored in the stack register. Control is transferred to address 0 on page 0 by a RESET (ON) interrupt, to address 2 on page 0 by an INT_A interrupt, to address 4 on page by an INT_B interrupt or to address 8 on page 0 by an INT_T interrupt by setting the control counter to 00, 02, 04 or 08 respectively. When control is transferred to address 0 page 0, the instruction is invalid and is not executed, so the first instruction is executed from address 1 on page 0.

(2) Interrupt enable flags
When an interrupt request is accepted additional interrupts are disabled until the accepted interrupt is processed. Except that a RESET (ON) interrupt may be accepted at any time.

(3) Skip flags
The skip flags are used to indicate an instruction skip and the NOP state for instructions LXY and LA are saved. A special stack is provided for saving these flags.

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General-Purpose I/O ports K, S, F, P and D

These 4-bit or 1-bit general-purpose registers are used for such things as data transfer between register A, instruction transfers, 1-bit transfers as selected by register Y, storing 7-bit immediate field data of instructions fetched from ROM, and data transfers between external RAM. Each output has a latch and its output circuit contains an open drain resistor or a pulldown resistor (high-impedance).

I/O ports K, S

Ports K and S are 4-bit latched I/O ports, that can transfer data to and from register A. Output latches are reset by the DIKS instruction when the port is being used as an input port.

Output port F

Port F is an 8-bit latched output port, that has independent latches for each bit. The individual bits can be set by the SF instruction and reset by the RF instruction.

Output port P

Port P is a 2-bit latched output port, that is usually in low-level, but can output the machine cycle high-level synchronous signal by SP_0 or SP_1 instructions. The 7 bits (F_4~F_0, P_1, P_0) can be used for direct fetching of the immediate field of the OTRO instruction.

Output port D

Port D is an 11-bit latched output port, that has independent latches for each bit. The contents for register Y indicate the individual bit to be set by the SD instruction or to be reset by the RD instruction. The 8-bit address of external memory (RAM) is output through this port.

Liquid Crystal Display Drive Circuit

The liquid crystal display direct drive circuit is composed of the following units. A block diagram of the units is shown in Fig. 1.

1 Control counter for the liquid crystal display
This is an octal counter composed of 3 bits and is counted down by the ELC instruction. The contents of the counter select 1 bit of register A and transfer data in order to the segment register RLC by the TLC instruction and determines the frame frequency for the liquid crystal display by transferring the contents of the counter to common register RCOM.

2 Register A
This 4-bit register is the accumulator. Its function is to control data processing, arithmetic operations control functions and input/output of the microcomputer.

3 Segment register RLC
The 26-bit segment register stores selected 1-bit data from register A by execution of the TLC instruction. It shifts 1 bit in order and stores the segment signals for the liquid crystal display device.

4 Common register RCOM
The 4-bit common register stores the common signal for the liquid crystal display. The input for the common register is the converted contents of the control counter for the liquid crystal display.

5 Port LC
The 26-bit latched port LC stores data in parallel by the ELC or DLC instruction from the segment register RLC. A bias resistor provides for the output at 2 levels and the 25 low-order bits are output as standard type. The high-order bit is not output to an external terminal.

6 Port COM
Port COM has 4 bits of latched storage. The data is transferred in parallel by the ELC or DLC instruction through the common register (RCOM). The outputs of this port have 3 biased levels by means of bias resistors.

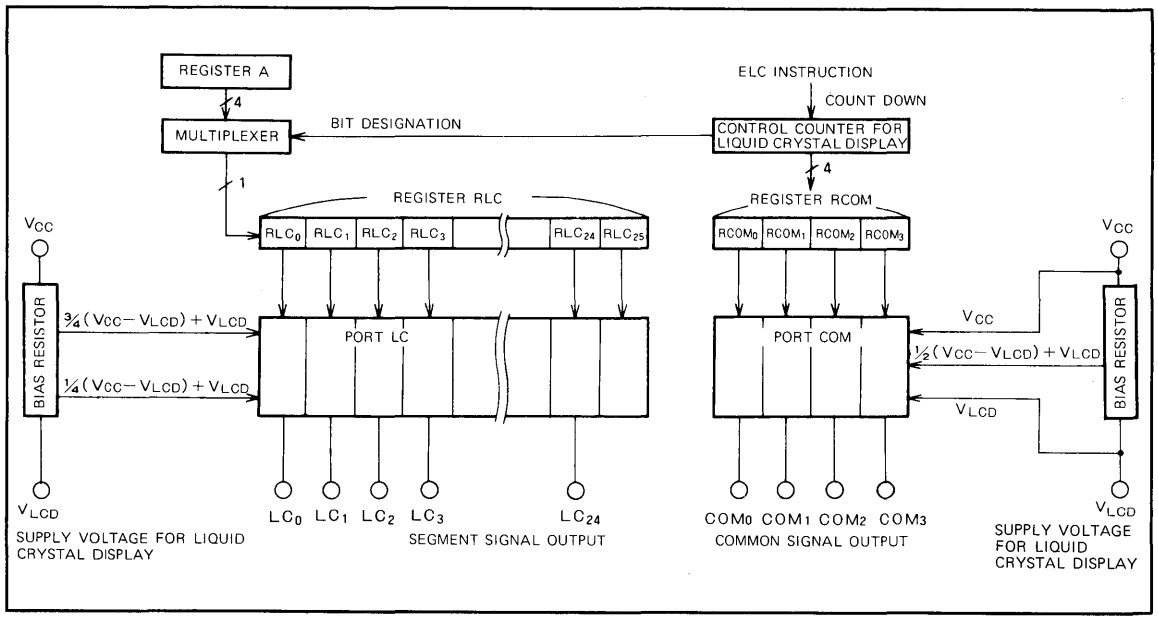

Fig. 1 Liquid crystal display drive circuit block diagram

RESET FUNCTION

As shown in Fig. 2, when the PWOFF input of the M58496-XXXP is driven low for at least 10ms, the input/output ports are reset and the interrupt disabled state is entered. (Refer to the descriptions of the power-on reset states in the Pin Description.) Next, if the PWON input is driven high, or an interrupt is generated by the internal power-on reset RESET (ON) caused by a frequency divider output INT_T, the program counter is set to address 0 page 0 as a starting location.

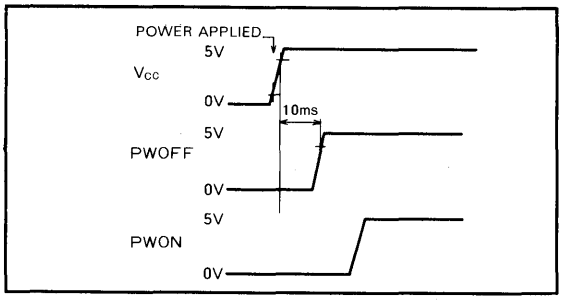

Fig. 2 Power-on reset circuit

CLOCK GENERATOR CIRCUIT

A built-in clock generator circuit has been provided and a quartz crystal or ceramic element (mask option) can be externally connected. In addition, an external clock source may be connected to pin X_{IN}, leaving pin X_{OUT} open. Circuit examples are shown in Fig. 3 and Fig. 4.

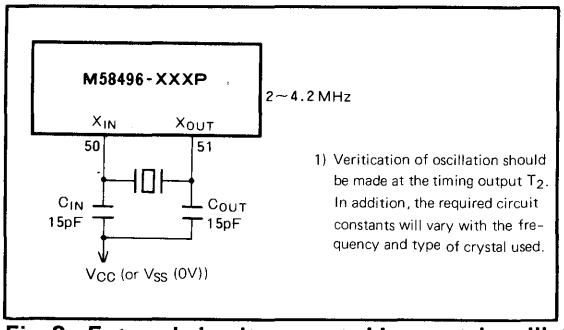

Fig. 3 External circuit connected by crystal oscillator

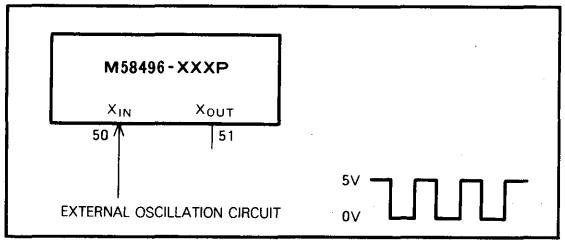

Fig. 4 External clock input circuit

Documentation Required Upon Ordering

The following information should be provided when ordering a custom mask.

(1) M58496-XXXP mask confirmation sheet
(2) ROM data ..... 3 EPROM sets
(3) Oscillation frequency selection
..... On confirmation sheets
(4) Frequency divider output selection (1Hz/2Hz)
..... On confirmation sheets

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INSTRUCTION CODE LIST (Note 1)

$D_9 \sim D_4$ (Hexadecimal notation) / $D_3 \sim D_0$		00 0000	00 0001	00 0010	00 0011	00 0100	00 0101	00 0110	00 0111	00 1000	00 1001	00 1010	00 1011	00 1100	00 1101	00 1110 ~ 00 1111	01 0000 ~ 01 0111	01 1000 ~ 01 1111	10 0000 ~ 10 0111	10 1000 ~ 10 1111	11 0000 ~ 11 0111	11 1000 ~ 11 1111
		0 0	0 1	0 2	0 3	0 4	0 5	0 6	0 7	0 8	0 9	0 A	0 B	0 C	0 D	0E ~ 0F	10 ~ 17	18 ~ 1F	20 ~ 27	28 ~ 2F	30 ~ 37	38 ~ 3F
0000	0	NOP	TLC	INY	SZB 0	SEY 0	SEI 0	SF 0	BL BLA BML BMLA	–	RAR	TAM 0	XAMD 0	A 0	LA 0	–	OTRO	LXY	BM	BMA	B	BA
0001	1	SCOM	DIKS	DEY	SZB 1	SEY 1	SEI 1	SF 1	BL BLA BML BMLA	–	–	TAM 1	XAMD 1	A 1	LA 1	–	OTRO	LXY	BM	BMA	B	BA
0010	2	EIA	SFK	XDP	SZB 2	SEY 2	SEI 2	SF 2	BL BLA BML BMLA	*	IK	TAM 2	XAMD 2	A 2	LA 2	–	OTRO	LXY	BM	BMA	B	BA
0011	3	DIA	SFS	TYA	SZB 3	SEY 3	SEI 3	SF 3	BL BLA BML BMLA	SEAM	IS	TAM 3	XAMD 3	A 3	LA 3	–	OTRO	LXY	BM	BMA	B	BA
0100	4	EIB	*	SC	RT	SEY 4	SEI 4	SF 4	BL BLA BML BMLA	*	TBA	TAM 4	XAMD 4	A 4	LA 4	–	OTRO	LXY	BM	BMA	B	BA
0101	5	DIB	DLC	RC	RTS	SEY 5	SEI 5	SF 5	BL BLA BML BMLA	TAY	–	TAM 5	XAMD 5	A 5	LA 5	–	OTRO	LXY	BM	BMA	B	BA
0110	6	DETS	*	XC	RTI	SEY 6	SEI 6	SF 6	BL BLA BML BMLA	AND	XAB	TAM 6	XAMD 6	A 6	LA 6	–	OTRO	LXY	BM	BMA	B	BA
0111	7	DETR	ELC	*	*	SEY 7	SEI 7	SF 7	BL BLA BML BMLA	EXL	TAB	TAM 7	XAMD 7	A 7	LA 7	–	OTRO	LXY	BM	BMA	B	BA
1000	8	EIT	SP0	*	*	SEY 8	SEI 8	RF 0	BL BLA BML BMLA	*	SB 0	XAM 0	XAMI 0	A 8	LA 8	–	OTRO	LXY	BM	BMA	B	BA
1001	9	DIT	*	SD	*	SEY 9	SEI 9	RF 1	BL BLA BML BMLA	CMA	SB 1	XAM 1	XAMI 1	A 9	LA 9	–	OTRO	LXY	BM	BMA	B	BA
1010	A	STM	SP1	*	*	SEY 10	SEI 10	RF 2	BL BLA BML BMLA	AM	SB 2	XAM 2	XAMI 2	A 10	LA 10	–	OTRO	LXY	BM	BMA	B	BA
1011	B	POF2	*	*	*	SEY 11	SEI 11	RF 3	BL BLA BML BMLA	*	SB 3	XAM 3	XAMI 3	A 11	LA 11	–	OTRO	LXY	BM	BMA	B	BA
1100	C	POF1	OTAD	*	*	SEY 12	SEI 12	RF 4	BL BLA BML BMLA	*	RB 0	XAM 4	XAMI 4	A 12	LA 12	–	OTRO	LXY	BM	BMA	B	BA
1101	D	SDET	*	RD	*	SEY 13	SEI 13	RF 5	BL BLA BML BMLA	*	RB 1	XAM 5	XAMI 5	A 13	LA 13	–	OTRO	LXY	BM	BMA	B	BA
1110	E	TTM	ADRT	*	*	SEY 14	SEI 14	RF 6	BL BLA BML BMLA	AMC	RB 2	XAM 6	XAMI 6	A 14	LA 14	–	OTRO	LXY	BM	BMA	B	BA
1111	F	TCK	TPW	*	SZC	SEY 15	SEI 15	RF 7	BL BLA BML BMLA	AMCS	RB 3	XAM 7	XAMI 7	A 15	LA 15	–	OTRO	LXY	BM	BMA	B	BA

Note 1: This list shows the machine codes and corresponding machine instructions $D_3 \sim D_0$ indicate the low-order 4 bits of the machine code and $D_9 \sim D_4$ indicate the high-order 6 bits. Hexadecimal numbers are also shown that represent the codes. An instruction may consist of one or two words, but only the first word is listed. Code combination indicated with asterisk (*) and bar (–) must not be used.

Two-word instructions

	Second word
BL	11 0xxx yyyy
BLA	11 1xxx XXXX
BML	10 0xxx yyyy
BMLA	10 1xxx XXXX

MACHINE INSTRUCTIONS (Note 1)

Item / Classification	Mnemonic	Instruction code D_9D_8	$D_7D_6D_5D_4$	$D_3D_2D_1D_0$	Hexa-decimal	No. of words	No. of cycles	Functions	Skip conditions	Flag CY
RAM address	**LXY x,y**	0 1	1 x x x	y y y y	18y + x	1	1	(X)←x, where, x=0~7 (Y)←y, where, y=0~15	Consecutively described	×
	INY	0 0	0 0 1 0	0 0 0 0	020	1	1	(Y)←(Y)+1	—	×
	DEY	0 0	0 0 1 0	0 0 0 1	021	1	1	(Y)←(Y)−1	—	×
Register to register transfer	**TAB**	0 0	1 0 0 1	0 1 1 1	097	1	1	(A)←(B)	—	×
	TBA	0 0	1 0 0 1	0 1 0 0	094	1	1	(B)←(A)	—	×
	XAB	0 0	1 0 0 1	0 1 1 0	096	1	1	(A)↔(B)	—	×
	TAY	0 0	1 0 0 0	0 1 0 1	085	1	1	(A)←(Y)	—	×
	TYA	0 0	0 0 1 0	0 0 1 1	023	1	1	(Y)←(A)	—	×
	XDP	0 0	0 0 1 0	0 0 1 0	022	1	1	(DP)↔(DP′)	—	×
RAM to accumulator transfer	**TAM j**	0 0	1 0 1 0	0 j j j	0Aj	1	1	(A)←(M(DP)) (X)←(X)∀j, where, j=0~7	—	×
	XAM j	0 0	1 0 1 0	1 j j j	0A8 + j	1	1	(A)↔(M(DP)) (X)←(X)∀j, where, j=0~7	—	×
	XAMD j	0 0	1 0 1 1	0 j j j	0Bj	1	1	(A)↔(M(DP)), (Y)←(Y)−1 (X)←(X)∀j, where, j=0~7	(Y)=15	×
	XAMI j	0 0	1 0 1 1	1 j j j	0B8 + j	1	1	(A)↔(M(DP)), (Y)←(Y)+1 (X)←(X)∀j, where, j=0~7	(Y)=0	×
Arithmetic	**LA n**	0 0	1 1 0 1	n n n n	0Dn	1	1	(A)←n, where, n=0~15	Consecutively described	×
	AM	0 0	1 0 0 0	1 0 1 0	08A	1	1	(A)←(A)+(M(DP))	—	×
	AMC	0 0	1 0 0 0	1 1 1 0	08E	1	1	(A)←(A)+(M(DP))+(CY) (CY)←Carry	—	0/1
	AMCS	0 0	1 0 0 0	1 1 1 1	08F	1	1	(A)←(A)+(M(DP))+(CY) (CY)←Carry	(CY)=0	0/1
	A n	0 0	1 1 0 0	n n n n	0Cn	1	1	(A)←(A)+n, where, n=0~15	Carry = 0	×
	SC	0 0	0 0 1 0	0 1 0 0	024	1	1	(CY)←1	—	1
	RC	0 0	0 0 1 0	0 1 0 1	025	1	1	(CY)←0	—	0
	XC	0 0	0 0 1 0	0 1 1 0	026	1	1	(CY)↔(CY′)	—	(CY′)
	SZC	0 0	0 0 1 1	1 1 1 1	03F	1	1	Skip if (CY)=0	(CY)=0	×
	AND	0 0	1 0 0 0	0 1 1 0	086	1	1	(A)←(A)∧(M(DP))	—	×
	EXL	0 0	1 0 0 0	0 1 1 1	087	1	1	(A)←(A)∀(M(DP))	—	×
	CMA	0 0	1 0 0 0	1 0 0 1	089	1	1	(A)←($\overline{A}$)	—	×
	RAR	0 0	1 0 0 1	0 0 0 0	090	1	1	(An−1)←(An) (CY)←(A0), (A3)←(CY)	—	(A0)
Bit manipulation	**SB i**	0 0	1 0 0 1	1 0 i i	098 + i	1	1	(Mi(DP))←1, where, i=0~3	—	×
	RB i	0 0	1 0 0 1	1 1 i i	09C + i	1	1	(Mi(DP))←0, where, i=0~3	—	×
	SZB i	0 0	0 0 1 1	0 0 i i	03i	1	1	Skip if (Mi(DP))=0, where, i=0~3	(Mi(DP))=0 where, i=0~3	×
Compare	**SEAM**	0 0	1 0 0 0	0 0 1 1	083	1	1	Skip if (M(DP))=(A)	(M(DP))=(A)	×
	SEY y	0 0	0 1 0 0	y y y y	04y	1	1	Skip if (Y)=y, where, y=0~15	(Y)=y, where, y=0~15	×
	SEI n	0 0	0 1 0 1	n n n n	05n	1	1	Skip if (A)=n, where, n=0~15	(A)=n, where, n=0~15	×
	SCOM	0 0	0 0 0 0	0 0 0 1	001	1	1	Skip if (SCA=0) and (SCB=0)	SCA=0 and SCB=0	×

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Item / Classification	Mnemonic	Instruction code D_9D_8	$D_7D_6D_5D_4$	$D_3D_2D_1D_0$	Hexa-decimal	No. of words	No. of cycles	Functions	Skip conditions	Flag CY
Branch	**B xy**	1 1	0 x x x	y y y y	**3xy**	1	1	$(PC_L) \leftarrow 16x + y$	—	×
	(Note 2)							$(PC_H) \leftarrow 15$, $(PC_L) \leftarrow 16x + y$		
	BL pxy	0 0	0 1 1 1	p p p p	**07p**	2	2	$(PC_H) \leftarrow p$	—	×
		1 1	0 x x x	y y y y	**3xy**			$(PC_L) \leftarrow 16x + y$		
	BA xX	1 1	1 x x x	X X X X	**38X + x**	1	1	$(PC_L) \leftarrow 16x + (A)$	—	×
	(Note 2)							$(PC_H) \leftarrow 15$, $(PC_L) \leftarrow 16x + (A)$		
	BLA pxX	0 0	0 1 1 1	p p p p	**07p**	2	2	$(PC_H) \leftarrow p$	—	×
		1 1	1 x x x	X X X X	**38X + x**			$(PC_L) \leftarrow 16x + (A)$		
Subroutine call	**BM xy**	1 0	0 x x x	y y y y	**2xy**	1	1	$(SK2) \leftarrow (SK1) \leftarrow (SK0) \leftarrow (PC)$ $(PC_H) \leftarrow 14$, $(PC_L) \leftarrow 16x + y$	—	×
	(Note 2)							$(PC_H) \leftarrow 14$, $(PC_L) \leftarrow 16x + y$		
	BML pxy	0 0	0 1 1 1	p p p p	**07p**	2	2	$(SK2) \leftarrow (SK1) \leftarrow (SK0) \leftarrow (PC)$	—	×
		1 0	0 x x x	y y y y	**2xy**			$(PC_H) \leftarrow p$, $(PC_L) \leftarrow 16x + y$		
	BMA xX	1 0	1 x x x	X X X X	**28X + x**	1	1	$(SK2) \leftarrow (SK1) \leftarrow (SK0) \leftarrow (PC)$ $(PC_H) \leftarrow 14$, $(PC_L) \leftarrow 16x + (A)$	—	×
	(Note 2)							$(PC_H) \leftarrow 14$, $(PC_L) \leftarrow 16x + (A)$		
	BMLA pxX	0 0	0 1 1 1	p p p p	**07p**	2	2	$(SK2) \leftarrow (SK1) \leftarrow (SK0) \leftarrow (PC)$	—	×
		1 0	1 x x x	X X X X	**28X + x**			$(PC_H) \leftarrow p$, $(PC_L) \leftarrow 16x + (A)$		
Return	**RTI**	0 0	0 0 1 1	0 1 1 0	**036**	1	1	$(PC) \leftarrow (SK0) \leftarrow (SK1) \leftarrow (SK2)$ Restore interrupt skip flags	—	×
	RT	0 0	0 0 1 1	0 1 0 0	**034**	1	1	$(PC) \leftarrow (SK0) \leftarrow (SK1) \leftarrow (SK2)$	—	×
	RTS	0 0	0 0 1 1	0 1 0 1	**035**	1	1	$(PC) \leftarrow (SK0) \leftarrow (SK1) \leftarrow (SK2)$	Unconditional	×
Input/output	**DIKS**	0 0	0 0 0 1	0 0 0 1	**011**	1	1	$(K) \leftarrow 0$, $(S) \leftarrow 0$	—	×
	IK	0 0	1 0 0 1	0 0 1 0	**092**	1	1	$(A) \leftarrow (K)$	—	×
	IS	0 0	1 0 0 1	0 0 1 1	**093**	1	1	$(A) \leftarrow (S)$	—	×
	SFK	0 0	0 0 0 1	0 0 1 0	**012**	1	1	$(K) \leftarrow (A)$	—	×
	SFS	0 0	0 0 0 1	0 0 1 1	**013**	1	1	$(S) \leftarrow (A)$	—	×
	SD	0 0	0 0 1 0	1 0 0 1	**029**	1	1	$(D(Y)) \leftarrow 1$, where, $0 \leqq (Y) \leqq 10$	—	×
	RD	0 0	0 0 1 0	1 1 0 1	**02D**	1	1	$(D(Y)) \leftarrow 0$, where, $0 \leqq (Y) \leqq 10$	—	×
	ADRT	0 0	0 0 0 1	1 1 1 0	**01E**	1	1	$(D) \leftarrow 0$	—	×
	OTAD	0 0	0 0 0 1	1 1 0 0	**01C**	1	1	$(D_7 \sim D_4) \leftarrow (B)$ $(D_3 \sim D_0) \leftarrow (Y)$	—	×
	SF m	0 0	0 1 1 0	0 m m m	**06m**	1	1	$(Fm) \leftarrow 1$, where, $m = 0 \sim 7$	—	×
	RF m	0 0	0 1 1 0	1 m m m	**068 + m**	1	1	$(Fm) \leftarrow 0$, where, $m = 0 \sim 7$	—	×
	OTRO mn	0 1	0 m m m	n n n n	**1mn**	1	1	$(F_0 \sim F_3) \leftarrow n$, where, $n = 0 \sim 15$ $(F_4, P_0, P_1) \leftarrow m$, where, $m = 0 \sim 7$	—	×
	SP0	0 0	0 0 0 1	1 0 0 0	**018**	1	1	$(P_0) \leftarrow 1$, where output 1 machine cycle	—	×
	SP1	0 0	0 0 0 1	1 0 1 0	**01A**	1	1	$(P_1) \leftarrow 1$, where output 1 machine cycle	—	×
	TLC	0 0	0 0 0 1	0 0 0 0	**010**	1	1	$(R(LC_0)) \leftarrow (Ai)$, where, $i = 0 \sim 3$ $(R(LC_{n+1})) \leftarrow (R(LC\ n))$	—	×
	ELC	0 0	0 0 0 1	0 1 1 1	**017**	1	1	$(P(LCn)) \leftarrow (R(LCn))$ $(P(COMn)) \leftarrow (R(COMn))$	—	×
	DLC	0 0	0 0 0 1	0 1 0 1	**015**	1	1	$(P(LCn)) \leftarrow (R(LCn))$ $(P(COM)) \leftarrow \frac{1}{2}(V_{CC} - V_{LCD}) + V_{LCD}$	—	×

Item / Classification	Mnemonic	Instruction code D_9D_8	$D_7D_6D_5D_4$	$D_3D_2D_1D_0$	Hexa-decimal	No. of words	No. of cycles	Functions	Skip conditions	Flag CY
Interrupt	**EIA**	0 0	0 0 0 0	0 0 1 0	**002**	1	1	Enables interruption of INT_A signal.	—	×
	DIA	0 0	0 0 0 0	0 0 1 1	**003**	1	1	Disables interruption of INT_A signal.	—	×
	EIB	0 0	0 0 0 0	0 1 0 0	**004**	1	1	Enables interruption of INT_B signal.	—	×
	DIB	0 0	0 0 0 0	0 1 0 1	**005**	1	1	Disables interruption of INT_B signal.	—	×
	EIT	0 0	0 0 0 0	1 0 0 0	**008**	1	1	Enables interruption of INT_T signal.	—	×
	DIT	0 0	0 0 0 0	1 0 0 1	**009**	1	1	Disables interruption of INT_T signal.	—	×
Timer	**STM**	0 0	0 0 0 0	1 0 1 0	**00A**	1	1	(TM)←(A), (TM F/F)←0 7-bit prescaler presetting	—	×
	TTM	0 0	0 0 0 0	1 1 1 0	**00E**	1	1	Skip if (TM F/F)=1	(TM F/F)=1	×
Power supply control	**TCK**	0 0	0 0 0 0	1 1 1 1	**00F**	1	1	Skip if (CK F/F)=1	(CK F/F)=1	×
	POF1	0 0	0 0 0 0	1 1 0 0	**00C**	1	1	(CK F/F)←0	—	×
	POF2	0 0	0 0 0 0	1 0 1 1	**00B**	1	1	(PW F/F)←0	—	×
	TPW	0 0	0 0 0 1	1 1 1 1	**01F**	1	1	Skip if (PW F/F)=1	(PW F/F)=1	×
	DETS	0 0	0 0 0 0	0 1 1 0	**006**	1	1	(DET F/F)←1	—	×
	DETR	0 0	0 0 0 0	0 1 1 1	**007**	1	1	(DET F/F)←0	—	×
	SDET	0 0	0 0 0 0	1 1 0 1	**00D**	1	1	Skip if (BD_{OUT})=1	(BD_{OUT})=1	×
Misc.	**NOP**	0 0	0 0 0 0	0 0 0 0	**000**	1	1	No operation	—	×

Note 1 : When the M58496-XXXP generates a skip it is not necessary to increment the program counter so no additional cycles are required for execution.

2 : Instructions B, BA, BM or BMA execute the second function of the functions column when executed, provided that none of instructions RT, RTS, BL, BML, BLA or BMLA was executed after execution of instruction BM or BMA.

Symbol	Meaning	Symbol	Meaning
A	4-bit register (accumulator)	P(COMn)	Common output port for liquid crystal display
Ai	Indicates the bits of register A. Where i=1~3	P(LCn)	Segment output port for liquid crystal display
B	4-bit auxiliary register	PW F/F	1-bit power supply control flag display
BD_{OUT}	Battery detector signal	R(COMn)	Common register for liquid crystal display (4 bits)
CK F/F	1-bit 1-second flag	R(LCn)	Segment register for liquid crystal display (25 bits)
CY	1-bit carry flag	S	4-bit I/O port
CY'	1-bit carry flag	SCA	Output of bit A of control counter for liquid crystal display
D	11-bit output port	SCB	Output of bit B of control counter for liquid crystal display
Di	Indicates the bits of port D. Where i=0~3	SK0	11-bit stack register
D(Y)	The bit of port D addressed by Y	SK1	11-bit stack register
DP	7-bit data pointer composed of register Y, X	SK2	11-bit stack register
		TM	4-bit timer/counter
Y, Y'	4-bit register	TM F/F	1-bit timer/counter flag
X, X'	3-bit register	xx	2-bit binary variable
DP'	7-bit data pointer	yyyy	4-bit binary variable
DET F/F	1-bit battery detector flag	mmm	3-bit binary variable
F	8-bit output port	nnnn	4-bit binary variable
Fi	Indicates the bits of port F. Where i=0~7	ii	2-bit binary variable
K	4-bit I/O port	jjj	3-bit binary variable
M(DP)	4-bit data of memory addressed by data pointer DP	XXXX	4-bit unknown binary variable (the value does not affect execution)
		←	Indicates direction of data flow
Mi(DP)	A bit of data of memory addressed by data pointer DP where i=0~3	( )	Indicates contents of register memory, etc.
		∀	Exclusive OR
PC	11-bit program acounter composed of PC_L, PC_H	∧	AND
		—	Negation
PC_L	Low-order 7 bits of the program counter	X	Indicates flag is unaffected by instruction execution
PC_H	High-order 4 bits of the program counter	xy	Label used to indicate the address xxx yyyy
P_0	1-bit output port	C	Hexadecimal number C + binary number-X
P_1	1-bit output port	+ x	

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−0.3~6.0	V
V_I	Input voltage		−0.3~V_{CC}+0.3	V
V_O	Output voltage		0 ~V_{CC}	V
P_d	Power dissipation	T_a=25°C	300	mW
T_{opr}	Operating free-air temperature range		0 ~50	°C
T_{stg}	Storage temperature range		−40~125	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0~50°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{LCD}	Liquid crystal supply voltage		0.8		V
V_{IH}	High-level input voltage	V_{CC}−0.8		V_{CC}	V
V_{IL}	Low-level input voltage	0		0.8	V
f_{XIN}	Oscillator frequency	2		4.2	MHz
f_ϕ	Internal clock oscillator frequency	250		525	kHz

ELECTRICAL CHARACTERISTICS (Ta=0~50°C, V_{CC}=5V±10%, V_{SS}=0V, f_{XIN}=2~4.2MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{OH}	High-level output current, port D	V_{OH}=(V_{CC}−0.5)V	−0.4	−0.8		mA
I_{OH}	High-level output current, ports F, P, K, and S	V_{OH}=(V_{CC}−0.5)V	−0.4	−0.6		mA
I_{OL}	Low-level output current, ports F, P, K, and S	V_{OL}=0.5V		2	20	μA
V_{OH}	High-level output voltage, port LC	V_{CC}=5V, V_{LCD}=0.8V, Ta=25°C	3.75	3.95		V
V_{OH}	High-level output voltage, port COM	V_{CC}=5V, V_{LCD}=0.8V, Ta=25°C	4.8	5		V
V_{OX}	Medium-level output voltage, port COM (Note 1)	V_{CC}=5V, V_{LCD}=0.8V, Ta=25°C	2.7	2.9	3.1	V
V_{OL}	Low-level output voltage, port LC	V_{CC}=5V, V_{LCD}=0.8V, Ta=25°C		1.85	2.05	V
V_{OL}	Low-level output voltage, port COM	V_{CC}=5V, V_{LCD}=0.8V, Ta=25°C		0.8	1	V
I_{CC}	Supply current, full operating condition	V_{CC}=5V, Ta=25°C, Output pins open		0.7	1	mA
I_{CC}	Supply current, partial operating condition	V_{CC}=5V, Ta=25°C, Output pins open		200	300	μA
I_{LCD}	Liquid crystal supply current, full operating condition	V_{CC}−V_{LCD}=4.2V, Ta=25°C, Output pins open		60	120	μA
C_i	Input capacitance	V_{CC}=V_I=V_O=V_{SS}, f=1MHz, 25mVrms		7	10	pF
$C_{i(XIN)}$	Oscillator input capacitance	V_{CC}=X_{OUT}=V_{SS}, f=1MHz, 25mVrms		7	10	pF
V_{BD}	Battery voltage detection voltage range (Note 2)	10kΩ≤R_{BD}≤200kΩ, Ta=25°C	4.5		5.5	V

Note 1. V_{OX} is the medium level of the 3-level output of port COM.
2. The detection resistance R_{BD} is connected between the V_{SS} and pin BDIN
3. Currents are taken to be positive when flowing into the IC with minimum and maximum values taken as absolute values.

TIMING REQUIREMENTS (Ta=0~50°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(K-X_{IN})}$	Data setup time before clock input, port K inputs	f_ϕ=525kHz (Note 1)	0			μs
$t_{su(S-X_{IN})}$	Data setup time before clock input, port S inputs		0			μs
$t_{su(INT_A-X_{IN})}$	Data setup time before clock input, INT_A input		0			μs
$t_{su(INT_B-X_{IN})}$	Data setup time before clock input, INT_B input		0			μs
$t_{h(K-X_{IN})}$	Data hold time after clock input, port K inputs		0.4			μs
$t_{h(S-X_{IN})}$	Data hold time after clock input, port S inputs		0.4			μs
$t_{h(INT_A-X_{IN})}$	Data hold time after clock input, INT_A input		0.4			μs
$t_{h(INT_B-X_{IN})}$	Data hold time after clock input, INT_B input		0.4			μs

Note 1. $f\phi$=1/8 f_{XIN} which corresponds to the internal clock frequency.

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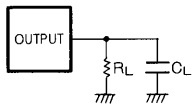
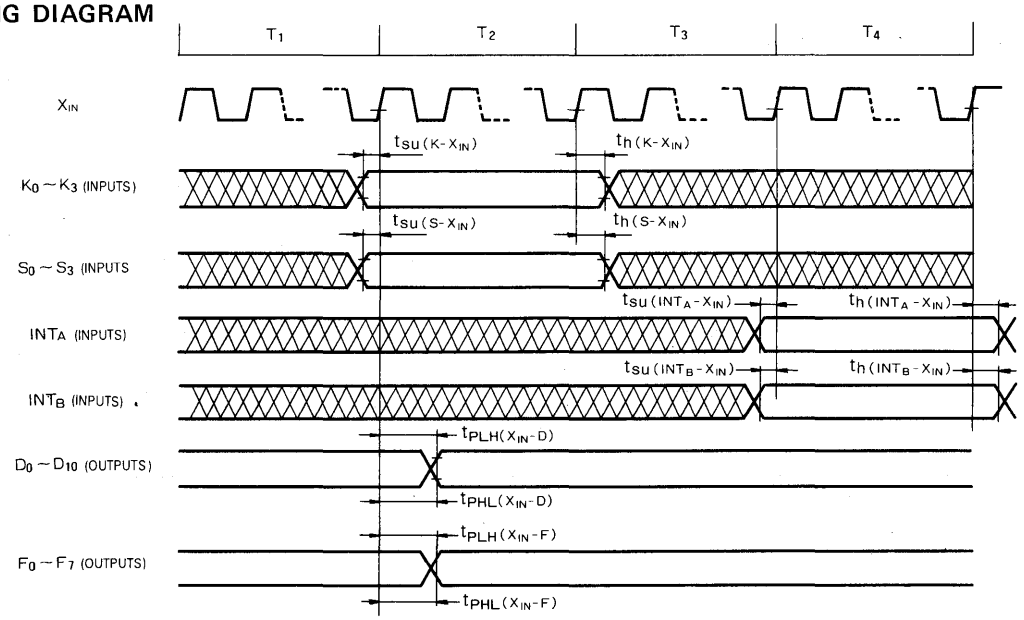
SWITCHING CHARACTERISTICS (Ta=0~50°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{PLH(X_{IN}-D)}$	Low-to-high-level propagation time from clock input to port data output, port D	f_ϕ=525kHz, R_L=20kΩ, C_L=100pF (Note 2)		0.7	1.5	μs
$t_{PLH(X_{IN}-F)}$	Low-to-high-level propagation time from clock input to port data output, port F, P, K, and S			0.7	1.5	μs
$t_{PHL(X_{IN}-D)}$	High-to-low-level propagation time from clock input to port data output, port D			2.2	3.0	μs
$t_{PHL(X_{IN}-F)}$	High-to-low-level propagation time from clock input to port data output, port F, P, K, and S			2.2	3.0	μs

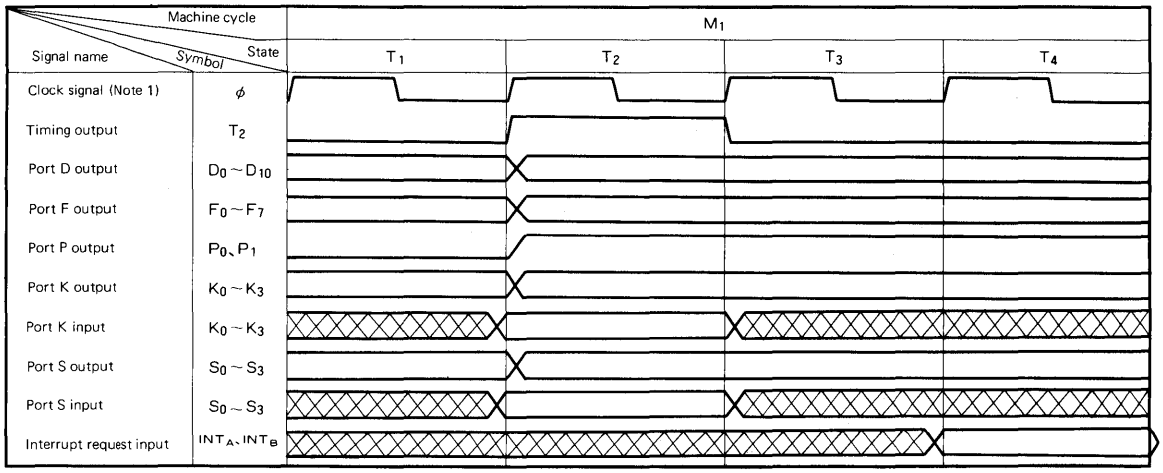
Note 2. Measurement circuit



TIMING DIAGRAM

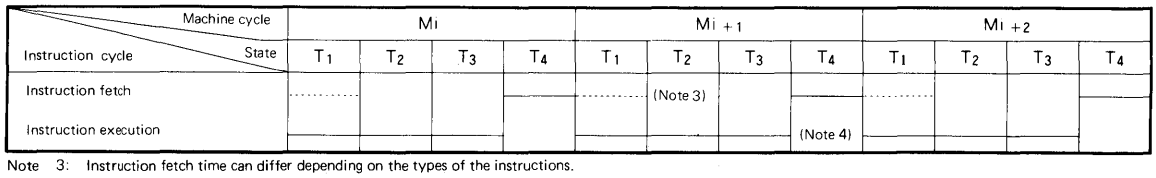


BASIC TIMING CHART (Note 2)



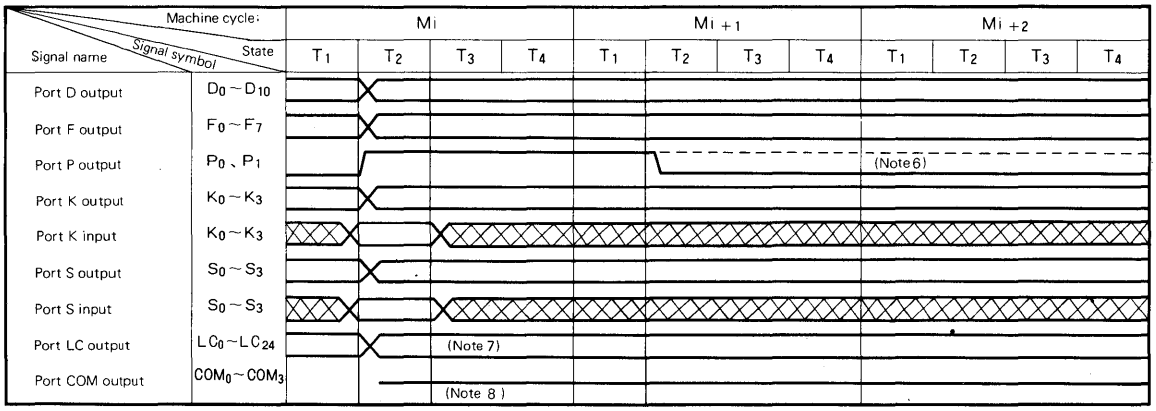
Note 1: Internal clock signal which is 1/8 of basic oscillation frequency.
2: ⊠ indicates an invalid signal input.

INSTRUCTION FETCH TIMING



Note 3: Instruction fetch time can differ depending on the types of the instructions.
4: The instruction which was fetched in the preceding cycle is executed.
5: The execution of the instruction and addressing of ROM and RAM are performed simultaneously.

I/O INSTRUCTION EXECUTION TIMING



Note 6: When an OTRO instruction is executed, the output is latched.
7: Output voltage of port LC depends upon power supply V_{LCD} for the liquid crystal display.
8: Output voltage of port COM has 3 levels depending on the power supply V_{LCD} for the liquid crystal display.

BRANCH AND SUBROUTINE CALL INSTRUCTION EXECUTION TIMING (Note 1)

Operation \ Machine cycle / State	M_i				M_{i+1}				M_{i+2}			
	T_1	T_2	T_3	T_4	T_1	T_2	T_3	T_4	T_1	T_2	T_3	T_4
Instruction B_{xy} (to be operated as the branch instruction, when the instruction BM or BMA was not executed before).												
Program counter		$(PC_L) \leftarrow xy$	$(PC_L) \leftarrow (PC_L)+1$				$(PC_L) \leftarrow (PC_L)+1$					
ROM address		(ROM address) $\leftarrow$ (PC)				(ROM address) $\leftarrow$ (PC)						
Execution of program	Execution of the branch instruction				Execution of the instruction stored in the branched address							
Instruction B_{xy} (to be operated as the branch instruction to page 15, when the instruction BM or BMA was executed before).												
Program counter		$(PC_H) \leftarrow 15$ $(PC_L) \leftarrow xy$	$(PC_L) \leftarrow (PC_L)+1$				$(PC_L) \leftarrow (PC_L)+1$					
ROM address		(ROM address) $\leftarrow$ (PC)				(ROM address) $\leftarrow$ (PC)						
Execution of program	Execution of the branch instruction				Execution of the instruction stored in the branched address on page 15							
Instruction BM_{xy} (subroutine call instruction).												
Program counter		$(PC_H) \leftarrow 14$ $(PC_L) \leftarrow xy$	$(PC_L) \leftarrow (PC_L)+1$				$(PC_L) \leftarrow (PC_L)+1$					
ROM address		(ROM address) $\leftarrow$ (PC)				(ROM address) $\leftarrow$ (PC)						
Stack register	$(SK_2) \leftarrow (SK_1) \leftarrow (SK_0) \leftarrow (PC)$											
Execution of program	Execution of the subroutine call instruction				Execution of the instruction stored in the subroutine called address							
Instruction BL p,xy (branch instruction).												
Program counter	(Temporary register) $\leftarrow P$	$(PC_L) \leftarrow (PC_L)+1$			$(PC_H) \leftarrow$ (Temporary register) $(PC_L) \leftarrow xy$		$(PC_L) \leftarrow (PC_L)+1$			$(PC_L) \leftarrow (PC_L)+1$		
ROM address		(ROM address) $\leftarrow$ (PC)				(ROM address) $\leftarrow$ (PC)				(ROM address) $\leftarrow$ (PC)		
Execution of program	Page number is stored temporarily				Execution of branch instruction				Execution of the instruction stored in the branched address			
Instruction BML p, xy (subroutine call instruction).												
Program counter	(Temporary register) $\leftarrow P$	$(PC_L) \leftarrow (PC_L)+1$			$(PC_H) \leftarrow$ (Temporary register) $(PC_L) \leftarrow xy$		$(PC_L) \leftarrow (PC_L)+1$			$(PC_L) \leftarrow (PC_L)+1$		
ROM address		(ROM address) $\leftarrow$ (PC)				(ROM address) $\leftarrow$ (PC)				(ROM address) $\leftarrow$ (PC)		
Stack register					$(SK_2) \leftarrow (SK_1) \leftarrow (SK_0) \leftarrow (PC)$							
Execution of program	Page number is stored temporarily				Execution of the subroutine call instruction				Execution of the instruction stored in the subroutine called address			

Note 1: The instructions BA, BMA, BLA and BMLA have the same execution timing as B, BM, BL and BML respectively as shown. The only difference is that $(PC_L) \leftarrow xy$ is replaced by $(PC_L) \leftarrow x(A)$.

INTERRUPT EXECUTION TIMING (Note 2)

Operation \ Machine cycle / State		M_{i-1}	M_i				M_{i+1}				M_{i+2}			
		T_4	T_1	T_2	T_3	T_4	T_1	T_2	T_3	T_4	T_1	T_2	T_3	T_4
Interrupt request input	INT_A (Note 3)													
Program counter	(PC)				$(PC_L) \leftarrow (PC_L)+1$				$(PC_L) \leftarrow (PC_L)$		$(PC_H) \leftarrow 0$ $(PC_L) \leftarrow 2$		$(PC_L) \leftarrow (PC_L)+1$	
ROM address				(ROM address) $\leftarrow$ (PC)				(ROM address) $\leftarrow$ (PC)				(ROM address) $\leftarrow$ (PC)		
Stack register											$(SK_2) \leftarrow (SK_1) \leftarrow (SK_0) \leftarrow (PC)$			
Execution of program											no execution (skip)			

Note 2: When the instruction executed in the machine cycle M_{i+1} is a BL, BML, BLA or BMLA, the value of address 2 of page 0 is stored in the program counter during M_{i+3}.
3: The interrupt request input INT_B has the same execution timing as INT_A. If the input is low level in the machine cycle M_{i-1} and high level in the machine cycle M_i, the interrupt is executed during the interrupt enable state.

M58497-XXXP

SINGLE-CHIP 4-BIT CMOS MICROCOMPUTER

DESCRIPTION

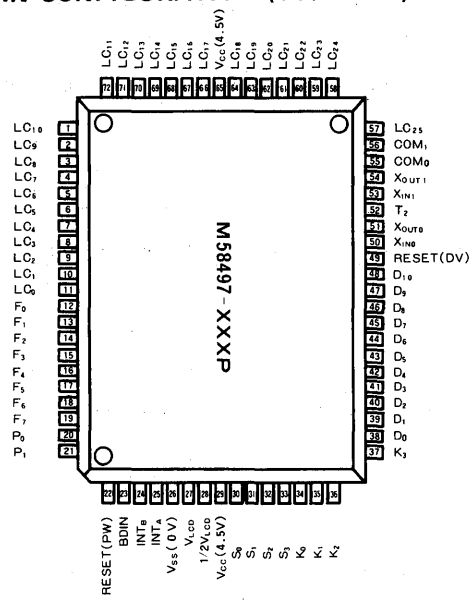
The M58497-XXXP is a single-chip 4-bit microcomputer fabricated using CMOS technology. Its features are liquid crystal display direct drive circuit, current saving circuit for back-up of a 15-stage frequency divider and RAM.

The device is designed for applications in which clock and liquid crystal display functions are included and where the low-power dissipation achieved by CMOS is especially important.

FEATURES

- Basic machine instructions 77
- Instruction execution time (at an oscillation frequency of 455kHz) 17.6μs
- Memory capacity: ROM: ..... 2048 words x 10 bits
  Internal RAM: .. 128 words x 4 bits
  External RAM: .. 256 words x 4 bits
- Single 4.5V power supply
- Internal oscillator circuit
- Internal 15-stage frequency divider
- Internal current saving cirucit
- Internal low-voltage detector circuit
- Subroutine nesting ..... 3 levels
- Internal timer: Prescaler: ..... 6 bits
  Timer: ..... 4 bits
- Output ports for liquid crystal display
  Segment signals (port LC) 26 bits
  Common signals (port COM) 2 bits

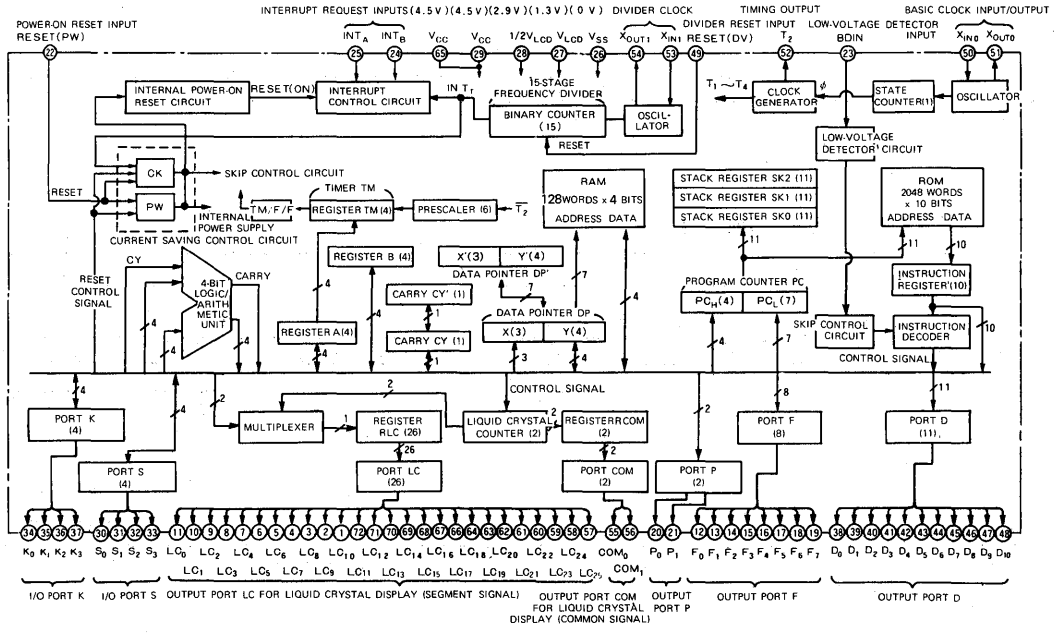
PIN CONFIGURATION (TOP VIEW)



Package Outline 72P2

- I/O ports (ports K and S) ..... 2 x 4 bits
- Output port (port D) ..... 11 x 1 bit
- Output port (port F) ..... 8 x 1 bit
- Output port (port P) ..... 2 x 1 bit
- Interrupt function ..... 4 factors, 1 level

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

SINGLE-CHIP 4-BIT CMOS MICROCOMPUTER

APPLICATIONS

- Electronic tuners for radios and TVs
- Medical equipment
- Measurement instruments
- Vending machines

FUNCTION

The M58497-XXXP consists of a 2,048 word x 10-bit mask ROM, 128 word x 4-bit RAM, 4-bit arithmetic logic unit, oscillator circuit, 15-stage frequency divider, power saving backup circuit for the RAM memory, low-voltage detector circuit, 4-bit timer, interrupt circuit, and liquid crystal display direct drive circuit. By connecting external 256-word x 4-bit CMOS RAMs to this 4-bit microcomputer, RAM capacity can be easily expanded.

The ROM is capable of storing 16 pages of 128 words of program, addresses being specified by the program counter. The program counter consists of a 7-bit address designating counter and a 4-bit page designating counter. Wrap-around to address zero is automatic after exceeding the address 127. The return address from subroutines and interrupts is stored in a stack register of 11 bits x 3 levels.

When an interrupt request has occurred, control is transferred to a fixed address as follows. If the case of internal power-on reset (RESET(ON)), the program is set to page 0, address 0, for the INT_A signal it is set to page 0, address 2, for the INT_B signal it is set to page 0, address 4, and for the output signal INT_T (1 second signal) of the 15-stage frequency divider, it is set to page 0, address 8.

The internal RAM is configured as 8 files of 16 words, addressed by the 7-bit data pointer. A 16 file x 16 digit external expansion memory can be addressed using 8 bits of address composed of the 4-bit register Y and 4-bit register B.

RAM addressing, register-to-register transfers, RAM-accumulator transfers, arithmetic operations, input/output operations, and timer operations are performed chiefly through the 4-bit register A (accumulator).

The current saving circuit used in conjunction with the 15-stage frequency divider and RAM can be controlled by the RESET (PW) input and program instructions.

The low-voltage detector circuit is operative when using a battery power source, and can be program controlled to provide an appropriate output upon sensing a low voltage level.

Direct drive of a liquid crystal display is possible using the 26 LC pins and 2 COM pins. 1/2 duty cycle and 1/2 bias or static drive is possible.

The output port D consists of 11 individually latched bits, and in addition to the ability to output a single bit, the position of which is determined by the contents of the data point register Y, 8 bits of the port D can be used as the external RAM address signal output.

Output port F consists of 8 individually latched bits that can be used to output data. It can be set or reset using program instructions.

5

PERFORMANCE SPECIFICATIONS

Parameter			Performance
Number of basic instructions			77
Execution time of basic instructions (one-word instruction)			17.6μs (V_{CC}=4.5V, f=455kHz)
Clock frequency			120~260kHz
Memory capacity	ROM		2,048 words x 10 bits
	Internal RAM		128 words x 4 bits
	External RAM		256 words x 4 bits
I/O ports	LC	Liquid crystal display output	26 bits
	COM	Liquid crystal display output	2 bits
	K	Input	4 bits
		Output	4 bits
	S	Input	4 bits
		Output	4 bits
	D	Output	11 x 1 bit
	F	Output	8 x 1 bit
	P	Output	2 x 1 bit
Frequency divider			15-stage built-in divider
Current saving circuit			Built-in
Low-voltage detector circuit			Built-in
Subroutine nesting			3 levels (including 1 level of interrupt)
Interrupt requests			4 factors, 1 level
Clock generator circuit			Built-in (for use with 455kHz ceramic filter externally connected)
Input/output ports	Output voltage		6V (max)
	Output current (I_{OL})		1.8mA (min)
Supply voltages	V_{CC}		4.5V (nom)
	V_{SS}		0V
Liquid crystal display driving voltage V_{LCD}			1.3V (nom)
Element structure			CMOS
Package			72-pin plastic molded flat package
Power dissipation (open output terminals)	In full operation		2mW (nom) (V_{CC}=4.5V, f=455kHz)
	Divider and RAM in the idle state		90μW (nom) (V_{CC}=4.5V, f=455kHz)

Output port P consists of 2 pins through which a synchronous signal of one machine cycle width can be output by program instructions.

Seven bits of output port F and P can be used to directly fetch the immediate field of the ROM.

The I/O ports K and S consist of 4 bits through which data can be transferred to and from register A.

PIN DESCRIPTIONS

Pin	Name	Input or output	State at reset (internal power-on)	Function
X_{IN0}	Clock oscillator input	Input	—	These are the clock input and output pins. A ceramic element or other frequency-determing element is connected between pins X_{IN0} and X_{OUT0}. When an external clock is used, connect the clock source to the X_{IN0} pin and leave the X_{OUT0} pin open.
X_{OUT0}	Clock oscillator output	Output	—	
X_{IN1}	Divider clock input	Input	—	These are the divider clock input and output pins. The quartz crystal that determines the reference oscillation frequency is connected between pins X_{IN1} and X_{OUT1}.
X_{OUT1}	Divider clock output	Output	—	
$RESET_{(DV)}$	Divider reset input	Input	—	This is the divider reset input for the 15-stage divider circuit used to divide the 32k Hz crystal reference signal.
BDIN	Low-voltage detector input	Input	—	A built-in low-voltage detector circuit has been provided. A resistor should be connected to the BDIN pin for voltage sensing.
INT_A	Interrupt request A signal	Input	Interrupt disable	These input signals are for an interrupt request. The request is accepted on the rising edge of the signal. In addition to these external input signals, an interrupt request INT_T from the 15-stage frequency divider output signal is also treated as an interrupt.
INT_B	Interrupt request B signal	Input	Interrupt disable	
$LC_0 \sim LC_{25}$	Liquid crystal display segment outputs	Output	—	These liquid crystal display outputs are suitable for driving a liquid crystal display at 1/2 duty cycle and 1/2 bias. The output ports for direct drive of such liquid crystal displays are port LC ($LC_0 \sim LC_{25}$) for the segments and port COM ($COM_0 \sim COM_1$) for the common outputs.
$COM_0 \sim COM_1$	Liquid crystal display common outputs	Output	—	
V_{LCD}, $\frac{1}{2}V_{LCD}$	Power supply for liquid crystal display	—	—	These are the liquid crystal display power supply pins for segment signals and common signals.
$D_0 \sim D_{10}$	Output port D	Output	High level	This output port consists of 11 bits, each of which is individually latched and can be selected to be set or reset according to the contents of register Y. In addition, 8 bits of this port can be used to fetch an 8-bit address for external RAM.
$F_0 \sim F_7$	Output port F	Output	High level	This output port consists of 8 bits, each of which is individually latched and can be set or reset using machine instructions.
P_0, P_1	Output port P	Output	High level	This output port consists of 2 bits from which one synchronous signal of one machine cycle width can be output per instruction. The 7-bit immediate field of an instruction can be output through this port in combination with 5 bits of port F.
$K_0 \sim K_3$	Input/output port K	Input/output	High level	Ports K and S are 4-bit latched input/output ports through which data can be transferred to and from register A (accumulator). When the output is programmed high, the high-impedance state is enabled allowing use of the pins as input pins.
$S_0 \sim S_3$	Input/output port S	Input/output	High level	
T_2	Timing output	Output	—	This timing output is used for testing the device.
$RESET_{(PW)}$	Power-on reset input	Input	Low level	When the internal power supply is switched on, a built-in automatic reset circuit generates a high level reset signal that resets the I/O ports and starts the system.

DESCRIPTION OF BASIC FUNCTIONAL BLOCKS

Program Counter PC

The program counter is an 11-bit address register. The 4 high-order bits are used to designate the page number and are as a group called PC_H. The 7 low-order bits are used to designate the address on the page and as a group are called PC_L. The PC designates the address of the 2048 words by 10-bit mask-programmable ROM. The ROM is organized into 16 pages of 128 words. As instructions are fetched from ROM, PC_L is incremented, so that, unless there is a branch, executed instructions are fetched and executed in sequence. Care must be taken when the last instruction on a page (address 127) is executed, because when PC_L is incremented it becomes zero with a carry, but the carry is disregarded so that the next instruction to be fetched will be the instruction at the first address of the same page. Therefore, to move to the next page, PC_H must be modified by using branch instructions such as BL, BML, BLA, and BMLA.

Pages 14 and 15 are special pages set aside to accommodate subroutines. Page 14 can be used to store subroutines, which are callable from pages other than page 14 by using the instructions BM and BMA which can be used as single-instructions to call page 14 subroutines.

When BM or BMA instructions are executed within page 14, they are equivalent to the branch instructions B and BA. When B or BA instructions are executed within page 14, a branch to the specified address on page 15 is executed.

Stack Registers SK_0, SK_1, SK_2

The 3-level stack register consists of 11-bit registers for storing the contents of the program counter when control is transferred from the main program to a subroutine or interrupt. Subroutines can use 3 levels, so that when 1 level is used for an interrupt routine 2 levels are reserved for subroutine nesting.

Data Pointers DP, DP'

The data pointer is used to designate the address of RAM or the bit position of output port D and consists of the 3-bit register X and the 4-bit register Y. The internal RAM is organized as 8 files of 16 words. Register X designates the file and register Y designates the word position of a file or the bit position of the output port D.

The data pointer DP' is selected by software during interrupt processing, leaving the contents of DP saved (unchanged).

The external RAM memory is organized as 16 files of 16 words that can be added to the system to expand memory capacity. Register Y is used to designate the word position of a file while register B designates the file itself.

Register A (Accumulator) and Carry Flags, CY, CY'

Register A is the 4-bit accumulator which forms the heart of the 4-bit microcomputer. Data processing operations such as arithmetic, transfer, exchange, conversion, and input/output operations are executed basically through this register.

The carry flag CY are used to store the carry or borrow from the most significant bit of the arithmetic unit resulting from the execution of various instructions. It can be tested and used for a variety of purposes. In principle, it acts as a 1-bit flag.

The carry flag CY' is used during interrupt processing to save the contents of the carry flag CY.

Register B (Auxiliary Register)

This register consists of a 4-bit register used for temporary storage as well as designate the file number of external RAM.

4-Bit Arithmetic Logic Unit

This unit is used to perform 4-bit arithmetic and logical operations and consists of a 4-bit adder and the associated logic circuitry. It is used to perform operations such as additions, complementing, logical and arithmetic comparisons, and bit manipulation.

Frequency Divider and Timer

A 15-stage frequency divider is used to divide the basic oscillator frequency. It is connected to the oscillator source device through pins X_{IN1} and X_{OUT1}. The frequency divider generates the interrupt request signal INT_T which is input to the interrupt control circuit. It also sets the CK flag for controlling the power saving circuit.

The basic oscillator circuit for the timer is the timing signal T_2. The timer consists of a 6-bit prescaler and a 4-bit counter. The timer flags TMF/F are set when a timer overflow occurs and sensed by the TTM instruction. The 4-bit timer counter is set by the STM instruction. Prescaler and timer flags are reset at the same time.

Power Saving Circuit

The power saving circuit is controlled by the CK flag and PW. Its output is sent to the built-in power supply reset circuit and causes the generation of an interrupt request signal RESET(ON). Control is unconditionally transferred to address 0 on page 0 and results in the resetting of I/O ports. The interrupt request signal RESET(ON) is generated on the rising edge of the built-in power supply reset output. The built-in power supply may be switched off by means of either an external signal or stop instruction, but power is maintained to the following circuits:

1. Internal data memory (RAM)

2. Divider Clock oscillator circuit
3. 15-stage frequency divider
4. Low-voltage detector circuit
5. Power saving circuit

Low-Voltage Detector Circuit

The low-voltage detector circuit is effective when using the M58497-XXXP with a battery power supply. The resistor which is used to determine the low sensing voltage is connected to the BDIN pin. A voltage falling below this level is sensed by the program and can be displayed by using an output port.

Interrupt Functions

Four factors in one level of hardware interrupt functions have been provided. The four interrupt request sources consist of the external interrupt requests INT_A and INT_B, the internal power-on reset output RESET(ON), and the 15-stage frequency divider output INT_T. Interrupt is enabled by the instructions EIA, EIB, and EIT, and disabled by the DIA, DIB, and DIT instructions respectively. Interrupt requests generated by the internal power supply by means of the reset output RESET(ON) cannot be disabled and will cause an unconditional hardware initialization whenever received.

In the interrupt enable state, interrupt requests INT_A and INT_B are accepted on the rising edge of these signals. When an interrupt request is received when interrupt is disabled, interrupt processing does not occur but the interrupt request is stored in a latch so that when the interrupt disable condition is cancelled the appropriate interrupt enabling instruction can be used to execute the interrupt routine immediately.

One level of the 3-level stack register is required when using an interrupt program. This leaves the remaining two levels available for subroutine processing. After an interrupt is processed, control is returned to the main program by means of an instruction such as RTI. Care must be taken, however, after starting an interrupt program to save the content of data pointer DP, register A, carry flag CY, and any other registers used by the interrupt program so that the contents may be restored before returning to the main program.

When an interrupt has been accepted, the microcomputer internal states are as follows.

(1) Program counter
The main program current address is stored in the stack register. Control is transferred to address 0 page 0 by a RESET(ON) interrupt, to address 2 page 0 by an INT_A interrupt to address 4 page 0 by an INT_B interrupt, and to address 8 page 0 by an INT_T interrupt. Note, however, that for the RESET(ON) signal the instruction on address 0 page 0 is invalid.

(2) Interrupt Enable Flags
If any of the four available interrupt factors are executed, all the interrupt enable flags are reset and the interrupt disable state is entered.

(3) Skip flags
Skip flags have been provided to indicate skip conditions for skip or continuous skip instructions. These are provided for all stacks, the stack flags being saved and the skip condition for an interrupt being held in memory.

General-Purpose I/O Ports K, S, F, P and D

These 4-bit and 1-bit general-purpose registers are used for such operations as data transfers to and from register A, instruction transfers, 1-bit transfers as selected by register Y, storage of the 7-bit immediate filed of instructions fetched from ROM, and data transfers between external RAM. Each output circuit is a latched CMOS circuit.

Input/output ports K and S are 4-bit ports, capable of data transfer with register A. When used as input ports, the DIKS instruction is used to reset the output latches.

The output port F consists of an 8-bit port with each bit independently latched. Each bit is settable and resettable by means of the SF and RF instructions respectively.

Output port P is a 2-bit port which is normally at the high level. The instructions SP_0 and SP_1 can be used to generate a low-level synchronous signal for one machine cycle.

Seven bits of the output ports F and P can be used to directly fetch the ROM immediate field value (7 bits) by means of the OTRO instruction.

The output port D consists of 11 bits independently latched. The contents of register Y indicate the individual bit to be set by the SD instruction or to be reset by the RD instruction. The 8-bit address of external memory (RAM) is output by means of this port.

Liquid Crystal Display Drive Circuit

The liquid Crystal display direct drive circuit consists of the following units. A block diagram of these units is shown in Fig. 1.

(1) Liquid crystal display control counter
This 2-bit quaternary counter counts down under control of the ELC instruction. The contents of this counter select 1 bit of register A and transfer data sequentially to the segment register RLC by a TLC instruction while determining the frame frequency by means of transferring the contents of the counter to the common register RCOM.

(2) Register A
This 4-bit register serves as an accumulator. Its func-

tions include microcomputer processing, control, and central processing for input and output.

(3) Segment Register RLC
This 26-bit serial register is used to store selected single data bit from register A by means of the TLC instruction. It shifts single bit in order and temporarily stores the segment signals for the liquid crystal display.

(4) Common Register RCOM
This 2-bit register is used to convert the contents of the liquid crystal display control counter to the common signals required for the display.

(5) Port LC
This 26-bit latched port is used to store data in parallel by means of the ELC or DLC instructions from the segment register RLC. It provides two levels of bias, the liquid crystal drive voltage V_{LCD} and the supply voltage V_{CC}.

(6) Port COM
Port COM consists of 2 latched bits used for parallel storage of data transferred from the common register RCOM by the ELC and DLC instructions. It provides 3 levels of bias including liquid crystal drive voltage (V_{LCD}, 1/2 V_{LCD}) and the supply voltage V_{CC}.

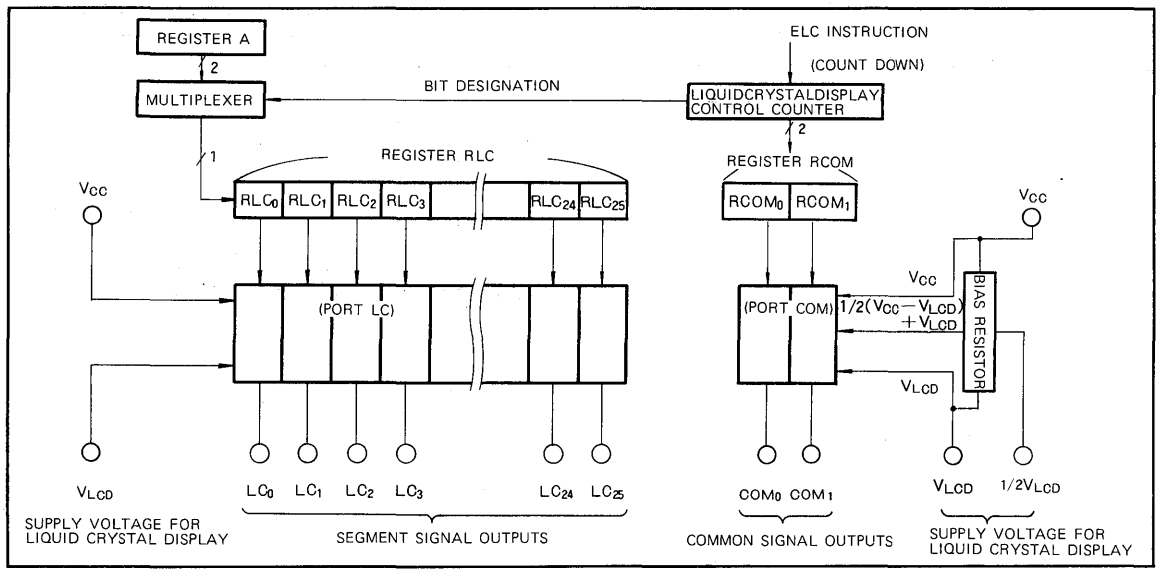


Fig. 1 Liquid crystal display drive circuit block diagram

Reset Function

As shown in Fig. 2, when a low level of at least 10ms is applied to the M58497-XXXP RESET(PW) input pin, all input/output ports are reset and interrupt is disabled. (Refer to the section on Power-on Reset States in the pin descriptions.) Next, when the RESET(PW) input is set to high, the internal power-on reset output RESET(ON) causes the generation of an interrupt and the program coutner is set to address 0 on page 0 as the starting address.

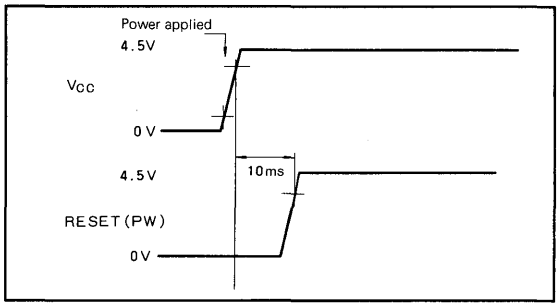


Fig. 2 Power-on reset circuit

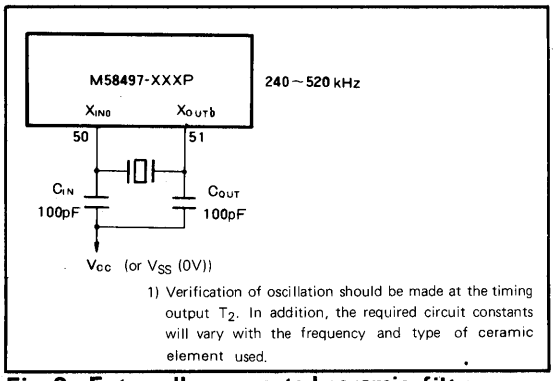
Clock Generator Circuit

A built-in clock generator circuit has been provided for use with a ceramic element connected between the clock input and output pins. In addition, an external clock source may be input at pin X_{IN0}, leaving X_{OUT0} open. Circuit examples are shown in Fig. 3 and Fig. 4.

Documentation Required Upon Ordering

The following information should be provided when ordering a custom mask.

(1) M58497-XXXP mask confirmation sheet
(2) ROM data ..... 3 EPROM sets
(3) Oscillation frequency selection
On confirmation sheets
(4) Frequency divider output selection (1Hz/2Hz)
On confirmation sheets



1) Verification of oscillation should be made at the timing output T_2. In addition, the required circuit constants will vary with the frequency and type of ceramic element used.

Fig. 3 Externally connected ceramic filter

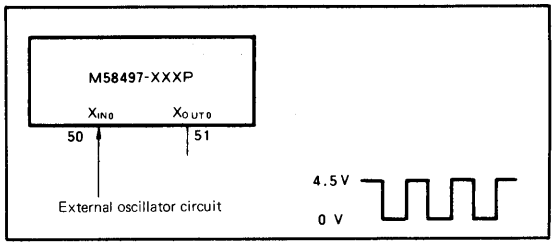


Fig. 4 External clock input circuit

INSTRUCTION CODE LIST (Note 1)

$D_9 \sim D_4$ / Hexadecimal notation / $D_3 \sim D_0$		00 0000	00 0001	00 0010	00 0011	00 0100	00 0101	00 0110	00 0111	00 1000	00 1001	00 1010	00 1011	00 1100	00 1101	00 1110 ↕ 00 1111	01 0000 ↕ 01 0111	01 1000 ↕ 01 1111	10 0000 ↕ 10 0111	10 1000 ↕ 10 1111	11 0000 ↕ 11 0111	11 1000 ↕ 11 1111
		00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E~0F	10~17	18~1F	20~27	28~2F	30~37	38~3F
0000	0	NOP	TLC	INY	SZB 0	SEY 0	SEI 0	SF 0	BL BLA BML BMLA	—	RAR	TAM 0	XAMD 0	A 0	LA 0	—	OTRO	LXY	BM	BMA	B	BA
0001	1	SCOM	DIKS	DEY	SZB 1	SEY 1	SEI 1	SF 1	BL BLA BML BMLA	—	—	TAM 1	XAMD 1	A 1	LA 1	—	OTRO	LXY	BM	BMA	B	BA
0010	2	EIA	SFK	XDP	SZB 2	SEY 2	SEI 2	SF 2	BL BLA BML BMLA	*	IK	TAM 2	XAMD 2	A 2	LA 2	—	OTRO	LXY	BM	BMA	B	BA
0011	3	DIA	SFS	TYA	SZB 3	SEY 3	SEI 3	SF 3	BL BLA BML BMLA	SEAM	IS	TAM 3	XAMD 3	A 3	LA 3	—	OTRO	LXY	BM	BMA	B	BA
0100	4	EIB	*	SC	RT	SEY 4	SEI 4	SF 4	BL BLA BML BMLA	*	TBA	TAM 4	XAMD 4	A 4	LA 4	—	OTRO	LXY	BM	BMA	B	BA
0101	5	DIB	DLC	RC	RTS	SEY 5	SEI 5	SF 5	BL BLA BML BMLA	TAY	—	TAM 5	XAMD 5	A 5	LA 5	—	OTRO	LXY	BM	BMA	B	BA
0110	6	DETS	*	XC	RTI	SEY 6	SEI 6	SF 6	BL BLA BML BMLA	AND	XAB	TAM 6	XAMD 6	A 6	LA 6	—	OTRO	LXY	BM	BMA	B	BA
0111	7	DETR	ELC	*	*	SEY 7	SEI 7	SF 7	BL BLA BML BMLA	EXL	TAB	TAM 7	XAMD 7	A 7	LA 7	—	OTRO	LXY	BM	BMA	B	BA
1000	8	EIT	SP0	*	*	SEY 8	SEI 8	RF 0	BL BLA BML BMLA	*	SB 0	XAM 0	XAMI 0	A 8	LA 8	—	OTRO	LXY	BM	BMA	B	BA
1001	9	DIT	*	SD	*	SEY 9	SEI 9	RF 1	BL BLA BML BMLA	CMA	SB 1	XAM 1	XAMI 1	A 9	LA 9	—	OTRO	LXY	BM	BMA	B	BA
1010	A	STM	SP1	*	*	SEY 10	SEI 10	RF 2	BL BLA BML BMLA	AM	SB 2	XAM 2	XAMI 2	A 10	LA 10	—	OTRO	LXY	BM	BMA	B	BA
1011	B	POF2	*	*	*	SEY 11	SEI 11	RF 3	BL BLA BML BMLA	*	SB 3	XAM 3	XAMI 3	A 11	LA 11	—	OTRO	LXY	BM	BMA	B	BA
1100	C	POF1	OTAD	*	*	SEY 12	SEI 12	RF 4	BL BLA BML BMLA	*	RB 0	XAM 4	XAMI 4	A 12	LA 12	—	OTRO	LXY	BM	BMA	B	BA
1101	D	SDET	*	RD	*	SEY 13	SEI 13	RF 5	BL BLA BML BMLA	*	RB 1	XAM 5	XAMI 5	A 13	LA 13	—	OTRO	LXY	BM	BMA	B	BA
1110	E	TTM	ADRT	*	*	SEY 14	SEI 14	RF 6	BL BLA BML BMLA	AMC	RB 2	XAM 6	XAMI 6	A 14	LA 14	—	OTRO	LXY	BM	BMA	B	BA
1111	F	TCK	TPW	*	SZC	SEY 15	SEI 15	RF 7	BL BLA BML BMLA	AMCS	RB 3	XAM 7	XAMI 7	A 15	LA 15	—	OTRO	LXY	BM	BMA	B	BA

Note 1: This list shows the machine codes and corresponding machine instructions. $D_3 \sim D_0$ indicate the low-order 4 bits of the machine code and $D_9 \sim D_4$ indicate the high-order 6 bits. Hexadecimal numbers are also shown that represent the codes. An instruction may consist of one or two words, but only the first word is listed. Code combinations indicated with asterisk (*) and bar (—) must not be used.

Two-word instructions

	Second word
BL	11 0xxxx yyyy
BLA	11 1xxxx XXXX
BML	10 0xxxx yyyy
BMLA	10 1xxxx XXXX

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MACHINE INSTRUCTIONS (Note 1)

Classification \ Item	Mnemonic	Instruction code D_9D_8	$D_7D_6D_5D_4$	$D_3D_2D_1D_0$	Hexa-decimal	No. of words	No. of cycles	Functions	Skip conditions	Flag CY
RAM address	**LXY x,y**	0 1	1 x x x	y y y y	18 y + x	1	1	(X)←x, where, x=0~7 (Y)←y, where, y=0~15	Consecutively described	×
	INY	0 0	0 0 1 0	0 0 0 0	020	1	1	(Y)←(Y)+1	—	×
	DEY	0 0	0 0 1 0	0 0 0 1	021	1	1	(Y)←(Y)−1	—	×
Register to register transfer	**TAB**	0 0	1 0 0 1	0 1 1 1	097	1	1	(A)←(B)	—	×
	TBA	0 0	1 0 0 1	0 1 0 0	094	1	1	(B)←(A)	—	×
	XAB	0 0	1 0 0 1	0 1 1 0	096	1	1	(A)↔(B)	—	×
	TAY	0 0	1 0 0 0	0 1 0 1	085	1	1	(A)←(Y)	—	×
	TYA	0 0	0 0 1 0	0 0 1 1	023	1	1	(Y)←(A)	—	×
	XDP	0 0	0 0 1 0	0 0 1 0	022	1	1	(DP)↔(DP')	—	×
RAM to accumulator transfer	**TAM j**	0 0	1 0 1 0	0 j j j	0Aj	1	1	(A)←(M(DP)) (X)←(X)∀j, where, j=0~7	—	×
	XAM j	0 0	1 0 1 0	1 j j j	0A8 + j	1	1	(A)↔(M(DP)) (X)←(X)∀j, where, j=0~7	—	×
	XAMD j	0 0	1 0 1 1	0 j j j	0Bj	1	1	(A)↔(M(DP)), (Y)←(Y)−1 (X)←(X)∀j, where, j=0~7	(Y)=15	×
	XAMI j	0 0	1 0 1 1	1 j j j	0B8 + j	1	1	(A)↔(M(DP)), (Y)←(Y)+1 (X)←(X)∀j, where, j=0~7	(Y)=0	×
Arithmetic	**LA n**	0 0	1 1 0 1	n n n n	0Dn	1	1	(A)←n, where, n=0~15	Consecutively described	×
	AM	0 0	1 0 0 0	1 0 1 0	08A	1	1	(A)←(A)+(M(DP))	—	×
	AMC	0 0	1 0 0 0	1 1 1 0	08E	1	1	(A)←(A)+(M(DP))+(CY) (CY)← Carry	—	0/1
	AMCS	0 0	1 0 0 0	1 1 1 1	08F	1	1	(A)←(A)+(M(DP))+(CY) (CY)← Carry	(CY)=0	0/1
	A n	0 0	1 1 0 0	n n n n	0Cn	1	1	(A)←(A)+n, where, n=0~15	Carry=0	×
	SC	0 0	0 0 1 0	0 1 0 0	024	1	1	(CY)←1	—	1
	RC	0 0	0 0 1 0	0 1 0 1	025	1	1	(CY)←0	—	0
	XC	0 0	0 0 1 0	0 1 1 0	026	1	1	(CY)↔(CY')	—	(CY')
	SZC	0 0	0 0 1 1	1 1 1 1	03F	1	1	Skip if (CY)=0	(CY)=0	×
	AND	0 0	1 0 0 0	0 1 1 0	086	1	1	(A)←(A)∧(M(DP))	—	×
	EXL	0 0	1 0 0 0	0 1 1 1	087	1	1	(A)←(A)∀(M(DP))	—	×
	CMA	0 0	1 0 0 0	1 0 0 1	089	1	1	(A)←$\overline{(A)}$	—	×
	RAR	0 0	1 0 0 1	0 0 0 0	090	1	1	(A_{n-1})←(An) (CY)←(A_0), (A_3)←(CY)	—	(A_0)
Bit manipulation	**SB i**	0 0	1 0 0 1	1 0 i i	098 + i	1	1	(Mi(DP))←1, where, i=0~3	—	×
	RB i	0 0	1 0 0 1	1 1 i i	09C + i	1	1	(Mi(DP))←0, where, i=0~3	—	×
	SZB i	0 0	0 0 1 1	0 0 i i	03i	1	1	Skip if (Mi(DP))=0, where, i=0~3	(Mi(DP))=0 where, i=0~3	×
Compare	**SEAM**	0 0	1 0 0 0	0 0 1 1	083	1	1	Skip if (M(DP))=(A)	(M(DP))=(A)	×
	SEY y	0 0	0 1 0 0	y y y y	04y	1	1	Skip if (Y)=y, where, y=0~15	(Y)=y, where, y=0~15	×
	SEI n	0 0	0 1 0 1	n n n n	05n	1	1	Skip if (A)=n, where, n=0~15	(A)=n, where, n=0~15	×
	SCOM	0 0	0 0 0 0	0 0 0 1	001	1	1	Skip if (SCA=0)	SCA=0	×

Item / Classification	Mnemonic	Instruction code $D_9 D_8$	$D_7 D_6 D_5 D_4$	$D_3 D_2 D_1 D_0$	Hexa-decimal	No. of words	No. of cycles	Functions	Skip conditions	Flag CY
Branch	**B xy** (Note 2)	1 1	0 x x x	y y y y	3xy	1	1	$(PC_L) \leftarrow 16x+y$ $(PC_H) \leftarrow 15$, $(PC_L) \leftarrow 16x+y$	—	×
	BL pxy	0 0 1 1	0 1 1 1 0 x x x	p p p p y y y y	07p 3xy	2	2	$(PC_H) \leftarrow p$ $(PC_L) \leftarrow 16x+y$	—	×
	BA xX (Note 2)	1 1	1 x x x	X X X X	38X + x	1	1	$(PC_L) \leftarrow 16x+(A)$ $(PC_H) \leftarrow 15$, $(PC_L) \leftarrow 16x+(A)$	—	×
	BLA pxX	0 0 1 1	0 1 1 1 1 x x x	P P P P X X X X	07p 38X + x	2	2	$(PC_H) \leftarrow p$ $(PC_L) \leftarrow 16x+(A)$	—	×
Subroutine call	**BM xy** (Note 2)	1 0	0 x x x	y y y y	2xy	1	1	$(SK2) \leftarrow (SK1) \leftarrow (SK_0) \leftarrow (PC)$ $(PC_H) \leftarrow 14$, $(PC_L) \leftarrow 16x+y$ $(PC_H) \leftarrow 14$, $(PC_L) \leftarrow 16x+y$	—	×
	BML pxy	0 0 1 0	0 1 1 1 0 x x x	p p p p y y y y	07p 2xy	2	2	$(SK2) \leftarrow (SK1) \leftarrow (SK_0) \leftarrow (PC)$ $(PC_H) \leftarrow p$, $(PC_L) \leftarrow 16x+y$	—	×
	BMA xX (Note 2)	1 0	1 x x x	X X X X	28X + x	1	1	$(SK2) \leftarrow (SK1) \leftarrow (SK_0) \leftarrow (PC)$ $(PC_H) \leftarrow 14$, $(PC_L) \leftarrow 16x+(A)$ $(PC_H) \leftarrow 14$, $(PC_L) \leftarrow 16x+(A)$	—	×
	BMLA pxX	0 0 1 0	0 1 1 1 1 x x x	p p p p X X X X	07p 28X + x	2	2	$(SK2) \leftarrow (SK1) \leftarrow (SK_0) \leftarrow (PC)$ $(PC_H) \leftarrow p$, $(PC_L) \leftarrow 16x+(A)$	—	×
Return	**RTI**	0 0	0 0 1 1	0 1 1 0	036	1	1	$(PC) \leftarrow (SK_0) \leftarrow (SK1) \leftarrow (SK2)$ Restore interrupt skip flags	—	×
	RT	0 0	0 0 1 1	0 1 0 0	034	1	1	$(PC) \leftarrow (SK_0) \leftarrow (SK1) \leftarrow (SK2)$	—	×
	RTS	0 0	0 0 1 1	0 1 0 1	035	1	1	$(PC) \leftarrow (SK_0) \leftarrow (SK1) \leftarrow (SK2)$	Unconditional	×
Input/output	**DIKS**	0 0	0 0 0 1	0 0 0 1	011	1	1	$(K) \leftarrow 1$, $(S) \leftarrow 1$,	—	×
	IK	0 0	1 0 0 1	0 0 1 0	092	1	1	$(A) \leftarrow (K)$	—	×
	IS	0 0	1 0 0 1	0 0 1 1	093	1	1	$(A) \leftarrow (S)$	—	×
	SFK	0 0	0 0 0 1	0 0 1 0	012	1	1	$(K) \leftarrow (A)$	—	×
	SFS	0 0	0 0 0 1	0 0 1 1	013	1	1	$(S) \leftarrow (A)$	—	×
	SD	0 0	0 0 1 0	1 0 0 1	029	1	1	$(D(Y)) \leftarrow 1$, where, $0 \leqq (Y) \leqq 10$	—	×
	RD	0 0	0 0 1 0	1 1 0 1	02D	1	1	$(D(Y)) \leftarrow 0$, where, $0 \leqq (Y) \leqq 10$	—	×
	ADRT	0 0	0 0 0 1	1 1 1 0	01E	1	1	$(D) \leftarrow 1$	—	×
	OTAD	0 0	0 0 0 1	1 1 0 0	01C	1	1	$(D_7 \sim D_4) \leftarrow (B)$ $(D_3 \sim D_0) \leftarrow (Y)$	—	×
	SF m	0 0	0 1 1 0	0 m m m	06m	1	1	$(Fm) \leftarrow 1$, where, $m=0 \sim 7$	—	×
	RF m	0 0	0 1 1 0	1 m m m	068 + m	1	1	$(Fm) \leftarrow 0$, where, $m=0 \sim 7$	—	×
	OTRO mn	0 1	0 m m m	n n n n	1mn	1	1	$(F_0 \sim F_3) \leftarrow n$, where, $n=0 \sim 15$ $(F_4, P_0, P_1) \leftarrow m$, where, $m=0 \sim 7$	—	×
	SP0	0 0	0 0 0 1	1 0 0 0	018	1	1	$(P_0) \leftarrow 0$, output for 1 machine cycle only	—	×
	SP1	0 0	0 0 0 1	1 0 1 0	01A	1	1	$(P_1) \leftarrow 0$, output for 1 machine cycle only	—	×
	TLC	0 0	0 0 0 1	0 0 0 0	010	1	1	$(R(LC_0)) \leftarrow (Ai)$, where, $i=0 \sim 1$ $(R(LCn+1)) \leftarrow (R(LCn))$	—	× ×
	ELC	0 0	0 0 0 1	0 1 1 1	017	1	1	$(P(LCn)) \leftarrow (R(LCn))$ $(P(COMn)) \leftarrow (R(COMn))$	—	×
	DLC	0 0	0 0 0 1	0 1 0 1	015	1	1	$(P(LCn)) \leftarrow (R(LCn))$ $(P(COM)) \leftarrow \frac{1}{2}(V_{CC}-V_{LCD})+V_{LCD}$	—	×

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Classification \ Item	Mnemonic	Instruction code D_9D_8	$D_7D_6D_5D_4$	$D_3D_2D_1D_0$	Hexadecimal	No. of words	No. of cycles	Functions	Skip conditions	Flag CY
Interrupt	**EIA**	0 0	0 0 0 0	0 0 1 0	**002**	1	1	Enables interruption of INT_A signal.	—	×
	DIA	0 0	0 0 0 0	0 0 1 1	**003**	1	1	Disables interruption of INT_A signal.	—	×
	EIB	0 0	0 0 0 0	0 1 0 0	**004**	1	1	Enables interruption of INT_B signal.	—	×
	DIB	0 0	0 0 0 0	0 1 0 1	**005**	1	1	Disables interruption of INT_B signal.	—	×
	EIT	0 0	0 0 0 0	1 0 0 0	**008**	1	1	Enables interruption of INT_T signal.	—	×
	DIT	0 0	0 0 0 0	1 0 0 1	**009**	1	1	Disables interruption of INT_T signal.	—	×
Timer	**STM**	0 0	0 0 0 0	1 0 1 0	**00A**	1	1	(TM)←(A), (TM F/F)←0 6-bit prescaler presetting	—	×
	TTM	0 0	0 0 0 0	1 1 1 0	**00E**	1	1	Skip if (TM F/F)=1	(TM F/F)=1	×
Power supply control	**TCK**	0 0	0 0 0 0	1 1 1 1	**00F**	1	1	Skip if (CK F/F)=1	(CK F/F)=1	×
	POF1	0 0	0 0 0 0	1 1 0 0	**00C**	1	1	(CK F/F)←0, with no CK flag input	—	×
	POF2	0 0	0 0 0 0	1 0 1 1	**00B**	1	1	(PW F/F)←0, with no PW flag input	—	×
	TPW	0 0	0 0 0 1	1 1 1 1	**01F**	1	1	Skip if (PW F/F)=1	(PW F/F)=1	×
	DETS	0 0	0 0 0 0	0 1 1 0	**006**	1	1	(DET F/F)←1	—	×
	DETR	0 0	0 0 0 0	0 1 1 1	**007**	1	1	(DET F/F)←0	—	×
	SDET	0 0	0 0 0 0	1 1 0 1	**00D**	1	1	Skip if (BD_{OUT})=1, (Skip if normal supply voltage apply)	(BD_{OUT})=1	×
Misc.	**NOP**	0 0	0 0 0 0	0 0 0 0	**000**	1	1	No operation	—	×

Note 1. When a skip has been generated, the next instruction only is invalid and the program counter is not incremented by 2. Therefore, the number of cycles does not change even if a skip is not generated.

2. Instructions Bxy, BAxX, BMxy and BMAxX execute the second function of the functions column when executed, provided that none of the instructions RT, RTS, BL, BML, BLA, or BMLA was executed after the execution of a BM or BMA instruction.

Symbol	Meaning	Symbol	Meaning
A	4-bit register (accumulator)	P(COMn)	Common output port for liquid crystal display
Ai	Indicates the bits of register A. Where i=0~1	P(LCn)	Segment output port for liquid crystal display
B	4-bit auxiliary register	PW F/F	1-bit power supply control flag display
BD_{OUT}	Battery detector signal	R(COMn)	Common register for liquid crystal display (4 bits)
CK F/F	1-bit 1-second flag	R(LCn)	Segment register for liquid crystal display (25 bits)
CY	1-bit carry flag	S	4-bit I/O port
CY'	1-bit carry stack flag	SCA	Output of bit A of control counter for liquid crystal display
D	11-bit output port	SK0	11-bit stack register
Di	Indicates the bits of port D. Where i=0~3	SK1	11-bit stack register
D(Y)	The bit of port D addressed by Y	SK2	11-bit stack register
DP	7-bit data pointer composed of register Y, X	TM	4-bit timer/counter
Y	4-bit register	TM F/F	1-bit timer/counter flag
X	3-bit register	xx	2-bit binary variable
DP'	7-bit data pointer	yyyy	4-bit binary variable
DET F/F	1-bit battery detector flag	mmm	3-bit binary variable
F	8-bit output port	nnnn	4-bit binary variable
Fi	Indicates the bits of port F. Where i=0~7	ii	2-bit binary variable
K	4-bit I/O port	jjj	3-bit binary variable
M(DP)	4-bit data of memory addressed by data pointer DP	XXXX	4-bit unknown binary variable (the value doesn't affect execution)
Mi(DP)	A bit of data of memory addressed by data pointer DP where i=0~3	←	Indicates direction of data flow
PC	11-bit program acounter composed of PC_L, PC_H	( )	Indicates contents of register memory, etc.
PC_L	Low-order 7 bits of the program counter	∀	Exclusive OR
PC_H	High-order 4 bits of the program counter	∧	AND
P_0	4-bit output port	—	Negation
P_1	4-bit output port	X	Indicates flag is unaffected by instruction execution
		xy	Label used to indicate the address
		C	Hexadecimal number C + binary number-X
		+	
		x	

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−0.3～6.0	V
V_I	Input voltage		−0.3～V_{CC}+0.3	V
V_O	Output voltage		0～V_{CC}	V
P_d	Power dissipation	Ta=25℃	300	mW
T_{opr}	Operating free-air temperature range		−20～70	℃
T_{stg}	Storage temperature range		−40～125	℃

RECOMMENDED OPERATING CONDITIONS (Ta=−20～70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	3	4.5	5.5	V
V_{SS}	Supply voltage		0		V
V_{LCD}	Liquid crystal supply voltage		1.3		V
V_{IH}	High-level input voltage	0.7V_{CC}		V_{CC}	V
V_{IL}	Low-level input voltage	0		0.3V_{CC}	V
f_{XIN}	Oscillator frequency	240	455	520	kHz
$f\phi$	Internal clock oscillator frequency	120		260	kHz

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ELECTRICAL CHARACTERISTICS (Ta=−20～70°C, V_{CC}=4.5V, V_{SS}=0V, f_{XIN}=455kHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{OH}	High-level output voltage, ports D, K, and S	I_{OH} = −10μA	4			V
V_{OH}	High-level output voltage, ports F, and P	I_{OH} = −200μA	2.4			V
V_{OL}	Low-level output voltage, ports D, K, and S	I_{OL} =1.8mA			0.5	V
V_{OL}	Low-level output voltage, ports F, and P	I_{OL} =1.8mA			0.5	V
V_{OH}	High-level output voltage, port LC	V_{LCD}=1.3V, Ta=25℃	4.3	4.5		V
V_{OH}	High-level output voltage, port COM	V_{LCD}=1.3V, Ta=25℃	4.3	4.5		V
V_{OX}	Medium output voltage, port COM (Note 1)	V_{LCD}=1.3V, Ta=25℃	2.7	2.9	3.1	V
V_{OL}	Low-level output voltage, port LC	V_{LCD}=1.3V, Ta=25℃		1.3	1.5	V
V_{OL}	Low-level output voltage, port COM	V_{LCD}=1.3V, Ta=25℃		1.3	1.5	V
I_{CC}	Supply current for full operation	Ta=25℃, Output pins open		0.4		mA
I_{CC}	Supply current for partial operation	Ta=25℃, Output pins open		20		μA
C_i	Input capacitance	V_{CC}=V_I=V_O=V_{SS}, f=1MHz, 25mVrms		7	10	pF
$C_{i(XIN)}$	Oscillator input capacitance	V_{CC}=X_{OUT}=V_{SS}, f=1MHz, 25mVrms		7	10	pF
V_{BD}	Battery voltage detection voltage range (Note 2)	10kΩ≤R_{BD}≤200kΩ, Ta=25℃	4		5.5	V

Note 1. V_{OX} is the medium level of the 3-level output of port COM.
2. The detection resistance R_{BD} is connected between the V_{SS} and BDIN pin.
3. Currents are taken to be positive when flowing into the IC with minimum and maximum values taken as absolute values.

TIMING REQUIREMENTS (T_a = −20~70°C, V_{CC} = 3~5.5V, V_{SS} = 0V, unless otherwise noted)

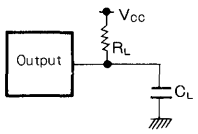
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(K\text{-}X_{IN})}$	Data setup time before clock input, port K inputs	f_ϕ = 230kHz (Note 1)	0			μs
$t_{su(S\text{-}X_{IN})}$	Data setup time before clock input, port S inputs		0			μs
$t_{su(INT_A\text{-}X_{IN})}$	Data setup time before clock input, INT_A input		0			μs
$t_{su(INT_B\text{-}X_{IN})}$	Data setup time before clock input, INT_B input		0			μs
$t_{h(K\text{-}X_{IN})}$	Data hold time after clock input, port K inputs		0.4			μs
$t_{h(S\text{-}X_{IN})}$	Data hold time after clock input, port S inputs		0.4			μs
$t_{h(INT_A\text{-}X_{IN})}$	Data hold time after clock input, INT_A input		0.4			μs
$t_{h(INT_B\text{-}X_{IN})}$	Data hold time after clock input, INT_B input		0.4			μs

Note 1. $f\phi = 1/2.f_{XIN}$ which corresponds to the internal clock frequency.

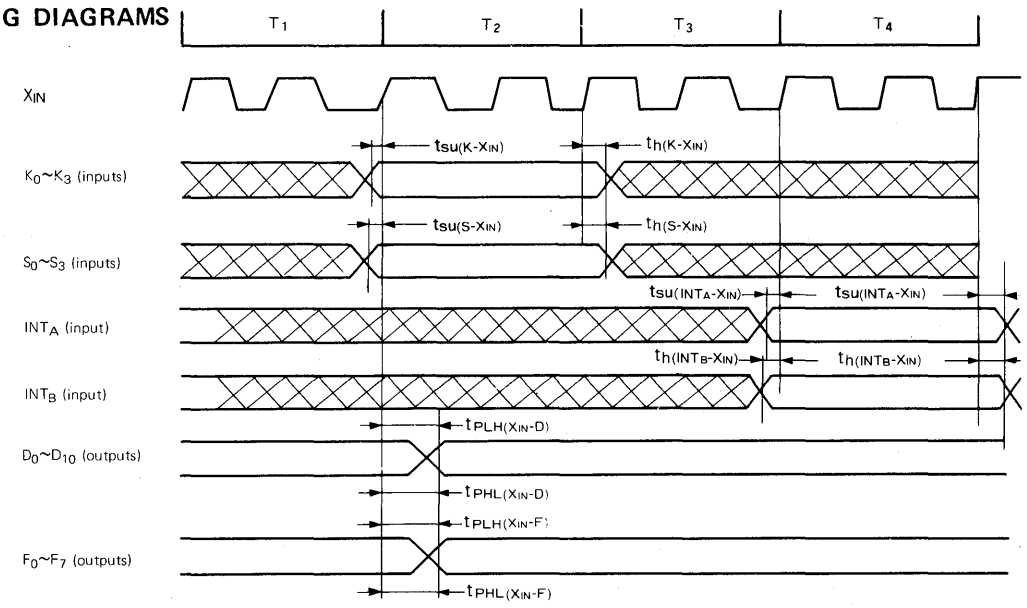
SWITCHING CHARACTERISTICS (T_a = −20~70°C, V_{CC} = 3~5.5V, V_{SS} = 0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{PLH(X_{IN}\text{-}D)}$	Low-to-high-level propagation time from clock input to port data output, port D	f_ϕ = 230kHz, R_L = 20kΩ, C_L = 100pF (Note 2)		2.2	3	μs
$t_{PLH(X_{IN}\text{-}F)}$	Low-to-high level propagation time from clock input to port data output, ports F, P, K, and S			2.2	3	μs
$t_{PHL(X_{IN}\text{-}D)}$	High-to-low-level propagation time from clock input to port data output, port D			0.7	1.5	μs
$t_{PHL(X_{IN}\text{-}F)}$	High-to-low-level propagation time from clock input to port data output, ports F, P, K, and S			0.7	1.5	μs

Note 2. Measurement circuit



TIMING DIAGRAMS



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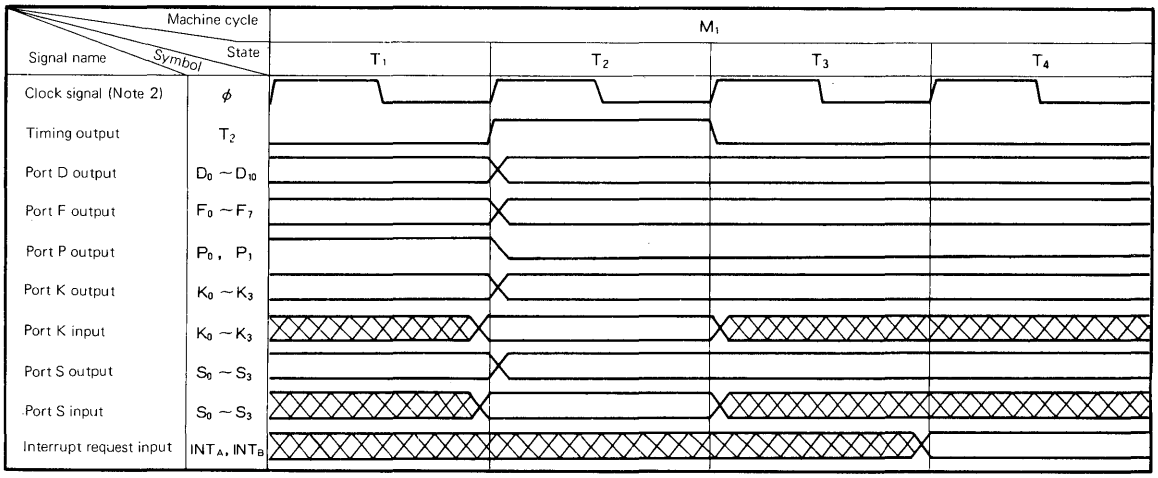
BASIC TIMING CHART (Note 1)



Note 1. ⊠ Indicates an invalid signal input.

2. Internal clock signal which is 1/2 of basic oscillation frequency.

INSTRUCTION FETCH TIMING

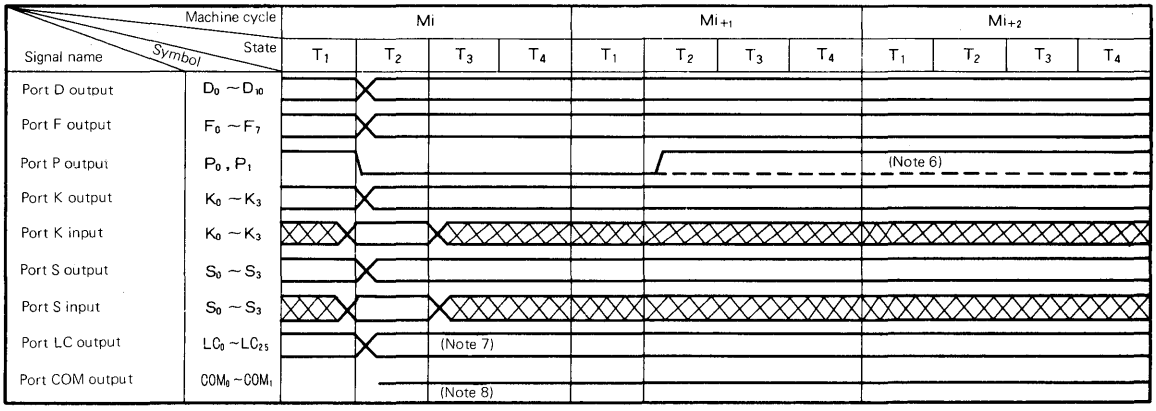
Machine cycle / State / Instruction cycle	Mi				Mi+1				Mi+2			
	T1	T2	T3	T4	T1	T2	T3	T4	T1	T2	T3	T4
Instruction fetch	.....				.....	(Note 3)			.....			
Instruction execution								(Note 4)				

Note 3. Instruction fetch time can differ depending on the types of the instructions.

4. The instruction which was fetched in the preceding cycle is executed.

5. The execution of the instruction and addressing of ROM and RAM are performed simultaneously.

I/O INSTRUCTION EXECUTION TIMING



Note 6. When an OTRO instruction is executed, the output is latched.

7. Output voltage of port LC depends upon power supply V_{LCD} for the liquid crystal display.

8. Output voltage of port COM has 3 levels depending on the power supply V_{LCD} for the liquid crystal display.

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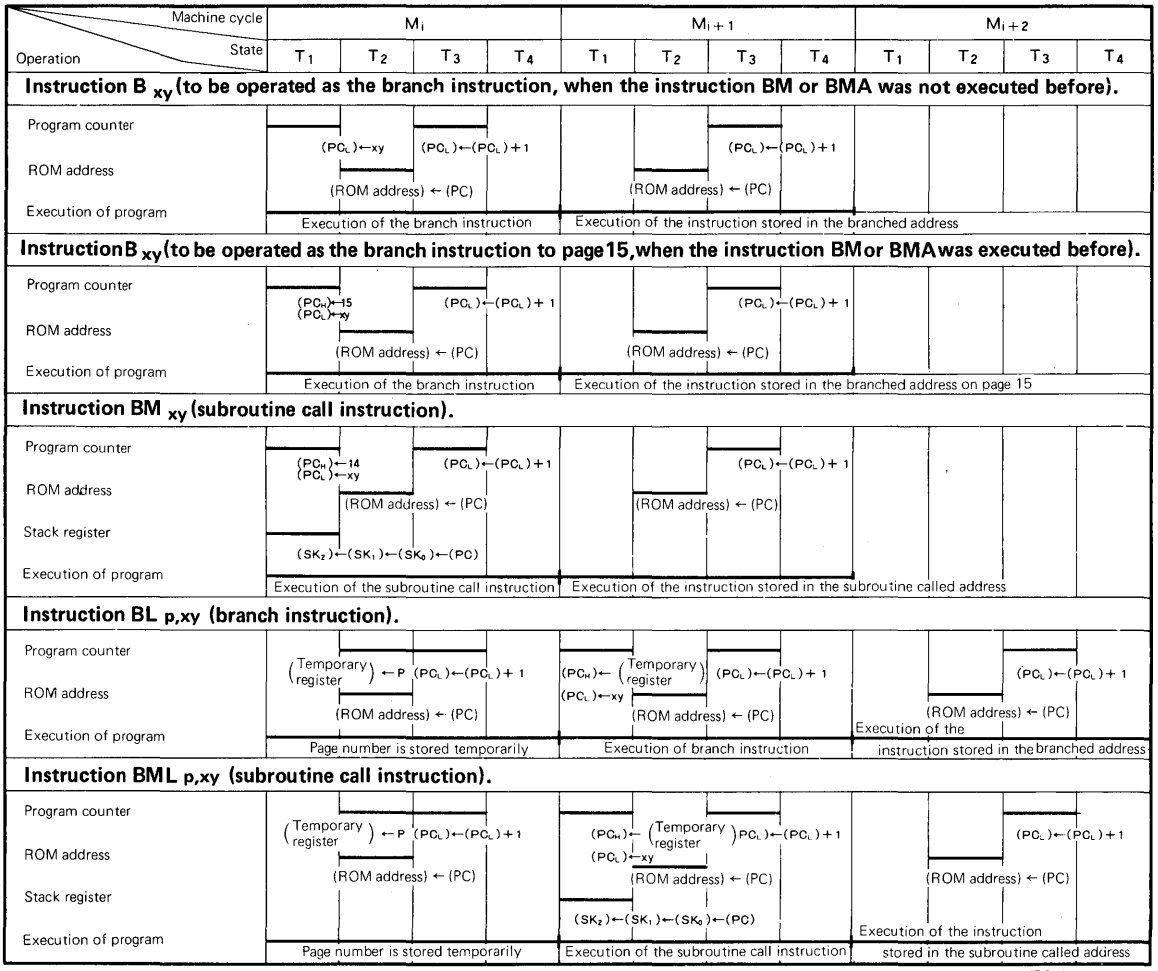
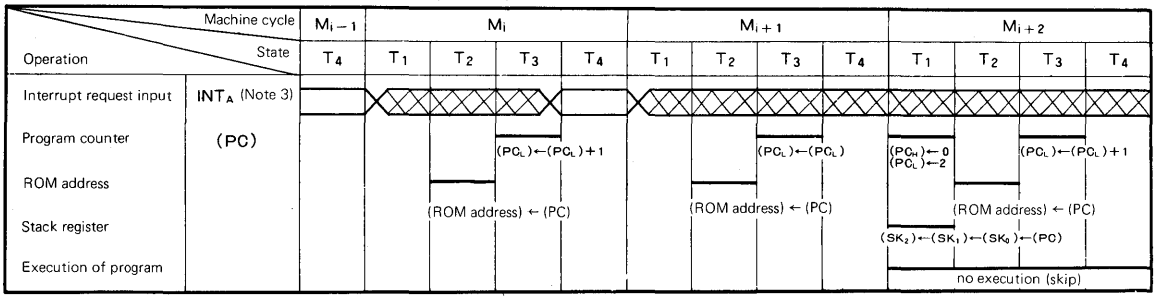
BRANCH AND SUBROUTINE CALL INSTRUCTION EXECUTION TIMING (Note 1)



Note 1. The instructions BA, BMA, BLA and BMAL have the same execution timing as B, BM, BL and BML respectively as shown. The only difference is that $(PC_L) \leftarrow xy$ is replaced by $(PC_L) \leftarrow x(A)$.

INTERRUPT EXECUTION TIMING (Note 2)



Note 2 When the instruction executed in the machine cycle M_{i+1} is a BL, BML, BLA or BMLA, the value of address 2 of page 0 is stored in the program counter during M_{i+3}.

3 The interrupt request input INT_B has the same execution timing as INT_A. If the input is low level in the machine cycle M_{i-1} and high level in the machine cycle M_i, the interrupt is executed during the interrupt enable state.