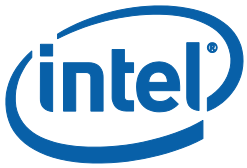


2nd Generation Intel® Core™ Processor Family Mobile with ECC

Datasheet Addendum

May 2012

Revision 002

Document Number: 324855-002

Contents

Figures

Tables

Revision History

Document Number	Revision Number	Description	Revision Date
324855	002	• Added notes for Memory and PCIe bus features of the Celeron 807UE (10 Watt) SKU • Added Section 1.7 *DC Specifications* to include DC electrical specs for the Celeron 807UE (10 Watt) SKU	April 2012
324855	001	Initial release	January 2011

§

1 Specification Addenda

1.1 Related Documents

Refer to the documents in the tables below for additional information.

Table 1. Processor Documents

Document	Document No./Location
Huron River Platform Power Delivery Design Guide	edc.intel.com
2nd Generation Intel® Core™ Processor Family Mobile Datasheet Volume 1 Supporting Intel® Core™ i7 Mobile Extreme Edition Processor Series and Intel® Core™ i5 and i7 Mobile Processor Series	www.intel.com
2nd Generation Intel® Core™ Processor Family Mobile Datasheet Volume 2 Supporting Intel® Core™ i7 Mobile Extreme Edition Processor Series and Intel® Core™ i5 and i7 Mobile Processor Series	www.intel.com
Intel® Core™ i7-600, i5-500 and i3-300 Mobile Processor Series Datasheet Addendum	416056
[Huron River] Platform – Design Guide	436735 edc.intel.com
Huron River Platform for Embedded Computing - Platform Design Guide (PDG) Addendum	439096 edc.intel.com
PCIe Bifurcation in Sandy Bridge Application Note Rev 0.7*	440737 edc.intel.com
Intel® MVP-7.0 Mobile Processor and Mobile Chipset Voltage Regulation Specification	TBD
RS - Platform Environment Control Interface (PECI) Specification	25891

Table 2. PCH Documents

Document	Document No./Location
Intel® 6 Series Chipset and Intel® C200 Series Chipset Datasheet	324645 www.intel.com

Table 3. Public Specifications

Document	Document No./Location
Advanced Configuration and Power Interface Specification 3.0	http://www.acpi.info/
PCI Local Bus Specification 3.0	http://www.pcisig.com/specifications
PCI Express Base Specification 2.0	http://www.pcisig.com
DDR3 SDRAM Specification	http://www.jedec.org
DisplayPort Specification	http://www.vesa.org
Intel® 64 and IA-32 Architectures Software Developer's Manuals	http://www.intel.com/products/processor/manuals/index.htm
Volume 1: Basic Architecture	253665
Volume 2A: Instruction Set Reference, A-M	253666
Volume 2B: Instruction Set Reference, N-Z	253667
Volume 3A: System Programming Guide	253668
Volume 3B: System Programming Guide	253669

1.2 Terminology

Term	Description
BGA	Ball Grid Array
DDR3	Third generation Double Data Rate SDRAM memory technology
DP	DisplayPort*
DMA	Direct Memory Access
DMI	Direct Media Interface
DTS	Digital Thermal Sensor
ECC	Error Correction Code
eDP*	Embedded DisplayPort*
GPU	Graphics Processing Unit

Term	Description
HDMI	High Definition Multimedia Interface
Intel® FDI	Intel® Flexible Display Interface
Intel® HT Technology	Intel® Hyper-Threading Technology
LLC	Last Level Cache. The LLC is the shared cache amongst all processor execution cores.
LVDS	Low Voltage Differential Signaling. A high speed, low power data transmission standard used for display connections to LCD panels.
PCH	Platform Controller Hub. The new 2009 chipset with centralized platform capabilities including the main I/O interfaces along with display connectivity, audio features, power management, manageability, security and storage features. The PCH may also be referred to using the code name Ibex Peak.
PECI	Platform Environment Control Interface
PEG	PCI Express* Graphics. External Graphics using PCI Express Architecture. A high-speed serial interface whose configuration is software compatible with the existing PCI specifications.
Processor	The 64-bit, single-core or multi-core component (package).
Processor Core	The term "processor core" refers to Si die itself which can contain multiple execution cores. Each execution core has an instruction cache, data cache, and 256-KB L2 cache. All execution cores share the L3 cache.
SMT	Simultaneous Multi-Threading.
Storage Conditions	A non-operational state. The processor may be installed in a platform, in a tray, or loose. Processors may be sealed in packaging or exposed to free air. Under these conditions, processor landings should not be connected to any supply voltages, have any I/Os biased or receive any clocks. Upon exposure to "free air" (i.e., unsealed packaging or a device removed from packaging material) the processor must be handled in accordance with moisture sensitivity labeling (MSL) as indicated on the packaging material.
TAC	Thermal Averaging Constant
TDP	Thermal Design Power
VCC	Processor core power supply
VSS	Processor ground
VAXG	Graphics core power supply
VTT	L3 shared cache, memory controller, and processor I/O power rail.
VDDQ	DDR3 power rail

Term	Description
VLD	Variable Length Decoding
x1	Refers to a Link or Port with one Physical Lane.
x4	Refers to a Link or Port with four Physical Lanes.
x8	Refers to a Link or Port with eight Physical Lanes
x16	Refers to a Link or Port with sixteen Physical Lanes

1.3 Introduction

This Datasheet Addendum contains information on the ***Embedded Mobile SKUs of the 2nd Generation Intel® Core™ processors.*** **These are referred throughout this document as the "Sandy Bridge–Mbl +ECC processor".** Non-Embedded SKUs are referred to as the "Sandy Bridge-Mbl processor".

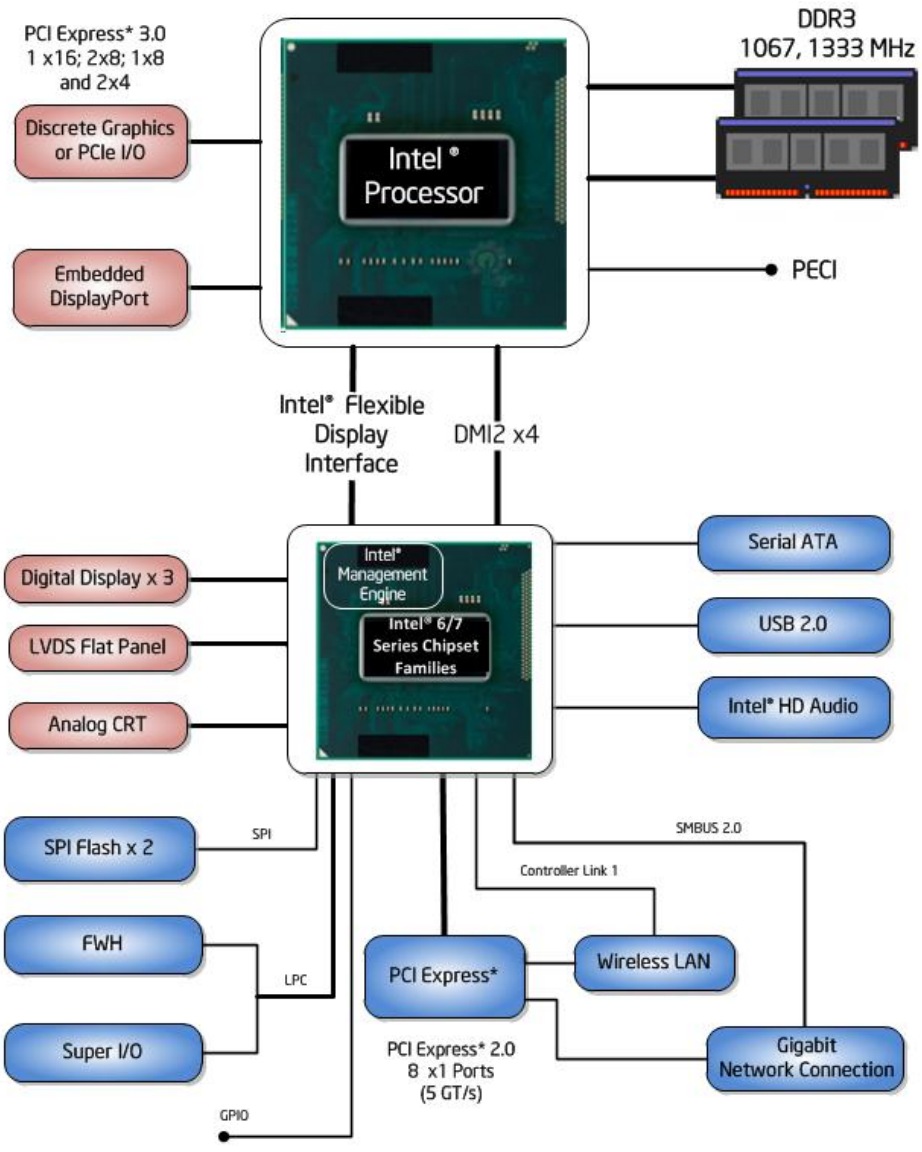
This Datasheet Addendum is a supplement to the ***2nd Generation Intel® Core™ Processors Family Mobile Datasheet***. It contains the additional DC and AC electrical specifications, signal integrity, differential signaling specifications, pinout and signal definitions, interface functional descriptions, additional feature information and configuration registers pertinent to the implementation and operation of the Sandy Bridge-Mbl + ECC Processor and its respective platform*.

Note: This document contains information on interfaces which differ from the Sandy Bridge-Mbl Processor are listed and included in the addendum for the Sandy Bridge-Mbl+ECC Processor.

The Sandy Bridge-Mbl +ECC Processor is the next generation of 64-bit, multi-core mobile processor built on 32- nanometer process technology. Throughout this document, Sandy Bridge series processors may be referred to as simply the processor. Based on the low-power/high-performance Sandy Bridge micro-architecture, the processor is designed for a two-chip platform as opposed to the traditional three-chip platforms (processor, GMCH, and ICH). The two-chip platform consists of a processor and the Platform Controller Hub (PCH) and enables higher performance, lower cost, easier validation, and improved x-y footprint. The PCH may also be referred to as Mobile Intel® 6 Series Chipset (formerly Cougar Point-M). The Sandy Bridge-Mbl + ECC processors referred in this document are designed for the Embedded Huron River+ECC platform (2nd Generation Intel® Core™ processor family and Intel® 6 Series chipset platform) and is offered in a BGA1023 package.

Note: Figure 1 shows the architecture of the Embedded Huron River + ECC platform with the Sandy Bridge-Mbl+ECC processor.

Figure 1. Huron River Platform with Sandy Bridge-Mbl + ECC Processor



1.4 Interfaces

1.4.1 System Memory Support

The following section talks about the features available on the Sandy Bridge-Mbl processor with the special features available only on the Sandy Bridge-Mbl + ECC processor highlighted in bold.

- One or two channels of DDR3 memory with a maximum of one DIMM per channel
- Single- and dual-channel memory organization modes
- Data burst length of eight for all memory organization modes
- 64-bit wide channels
- DDR3 I/O Voltage of 1.5 V.
- The memory controller on Sandy Bridge+ ECC BGA SKU Shares baseline feature set with the Sandy Bridge BGA CPU SKU
- **Adds support for un-buffered ECC DDR3 memory at 1066 and 1333 MT/s**
- **ECC support requires the addition of 20 extra signals (10 per channel):**
  - **Channel A, ECC Check Bits**
  - **Channel B, ECC Check Bits**
  - **Channel A, ECC Strobes**
  - **Channel B, ECC Strobes**
- **Supports ECC and non-ECC, unbuffered DDR3 DIMMs**
- Mixing of ECC and Non-ECC DIMMS is not supported
- Single Channel Mode
  - Either Channel A or Channel B may be populated
  - irrespective of Intel® AMT activity
  - One DIMM Per Channel Supported
- Dual Channel Mode
  - Both Channel A and Channel B are populated
  - One DIMM per channel supported
  - Dual Channel Symmetric (Interleaved)
  - Provides maximum performance. Amount of memory per channel must be the same
  - Dual-Channel Asymmetric
  - Trades performance for flexibility. Amount of memory per channel does not need to be the same
  - Intel® Flex Memory Technology
  - Combines advantages of Dual-Channel Symmetric and Asymmetric modes. Amount of memory per channel does not need to be the same
- DDR3 1066 MT/s (PC3-8500) or 1333 MT/s (PC3-10600) support
  - 512Mb, 1Gb, 2Gb or 4Gb technologies for x8 and x16 devices
  - 17.1 GB/S in dual-channel mode assuming DDR3 1066 MT/s
  - 21.3 GB/S in dual-channel mode assuming DDR3 1333MT/s

- Maximum memory capacity of 16 GB (using x8 devices, in a 2Rank, dual-channel SO-DIMM memory configuration)
- SODIMM module types Raw Card A, B, C, D and F supported.

- Intel® Fast Memory Access (Intel® FMA)
  - Just-in-Time Command Scheduling
  - Command Overlap
  - Out-of-Order Scheduling

Note: The single core Celeron sku Intel® Celeron® Processor 807UE supports only a single memory channel.

1.4.2 PCI Express*

Only the unique features of the Sandy Bridge-Mbl+ECC are listed here. For the rest of the specifications please refer to the *2nd Generation Intel® Core™ Processor Family Mobile Datasheet*.

- The processor PCI Express* port(s) are fully-compliant to the PCI Express Base Specification, Revision 2.0.
- The processor supports:
  - One 16-lane PCI Express port for graphics or I/O.
  - Two 8-lane PCI Express ports for graphics or I/O.
  - One 8-Lane, Two 4- Lane PCI Express Ports for Graphics or I/O
  - Four 4 -Lane PCI Express Ports for I/O - Available only on select processors skus.

Note: Connection of PCI Express lanes and the bifurcation information is provided in the *PCIe** Bifurcation in *Sandy Bridge Application Note*.

Note: The single core Celeron SKU Intel® Celeron® Processor 807UE does not support PCI Express in any configuration. All of the processor's PCI Express lanes are disabled for both graphics and I/O.

1.5 Signal Information

The signals listed below are for the memory bus. The ECC signals are supported only by the Sandy Bridge-Mbl+ECC processor.

Table 4. Memory Bus Signals for the Sandy Bridge-Mbl+ECC Processor

Signal Name	Description
Dual-Channel – Data Signal Group	
SA_DQ [63:0], SB_DQ [63:0]	Data Bus
SA_DM [7:0], SB_DM [7:0]	Data Mask
SA_DQS [7:0], SA_DQS# [7:0], SB_DQS [7:0], SB_DQS# [7:0]	Data Strobe

Dual-Channel - ECC Signal Group	
SA_DQ [71:64], SB_DQ [71:64]	ECC Check Data Bits
SA_DQS [8], SA_DQS# [8], SB_DQS [8],SB_DQS# [8]	ECC Data Strobes
Dual-Channel – Command Signal Group	
SA_MA [15:0], SB_MA [15:0]	Memory Address Bus
SA_BS [2:0], SB_BS [2:0]	Bank Select
SA_RAS#, SB_RAS#	Row Address Select
SA_CAS#, SB_CAS#	Column Address Select
SA_WE#, SB_WE#	Write enable
Dual-Channel – Control Signal Group	
SA_CS# [1:0],SB_CS# [1:0]	Chip Select(One Per Rank)
SA_CKE [1:0], SB_CKE [1:0]	Clock Enable(One Per Rank)
SA_ODT [1:0], SB_ODT [1:0]	On-Die Termination Select/Enable
Dual-Channel – Clock Signal Group	
SA_CK [1:0], SB_CK [1:0]	Differential Clocks
SA_CK# [1:0], SB_CK# [1:0]	Inverted Differential Clocks

Note: Refer to the *Huron River Platform Design Guide* for design considerations and guidelines for DDR3 Non-ECC SO-DIMM system memory.

ECC Check Data Bits - SA_DQ [71:64], SB_DQ [71:64]

SA_DQ [71:64] and SB_DQ [71:64] are not required for a DDR3 Non-ECC SO-DIMM implementation. They can be left floating on Sandy Bridge-Mbl+ECC.

ECC Data Strobes - SA_DQS [8], SA_DQS# [8], SB_DQS [8], SB_DQS# [8]

SA_DQS [8], SA_DQS# [8], SB_DQS [8] & SB_DQS# [8] are not required for a DDR3 Non-ECC SO-DIMM implementation. They can be left floating on Sandy Bridge-Mbl+ECC.

1.6 Thermal and Power Specifications

Table 5 and Table 6 provide the TDP specifications and package turbo parameters for the **Intel® Celeron® Processor 807UE.**

1.6.1 TDP specifications

The following Package TDP specifications apply to the **Intel® Celeron® Processor 807UE SKU**. It is also referred to as the Single Core Ultra-Low Voltage or "1 Core ULV" segment. For TDP specifications on all other mobile SKUs, refer to the *2nd*

Generation Intel® Core™ Processor Family Mobile External Design Specification (EDS), Volume 1 #445463.

Table 5. TDP specifications

Segment	State	CPU core Frequency	Processor Graphics Frequency	Thermal Design Power
Celeron 807UE (1 Core ULV)	HFM	1 GHz	350 MHz up to 800 MHz	10 W
	LFM	800 MHz	350 MHz up to 800 MHz	10 W

1.6.2 Package Turbo Parameters

The following package turbo parameters apply to the Intel® Celeron® Processor 807UE SKU. It is also referred to as the Single Core Ultra-Low Voltage or "1 Core ULV" segment.

This SKU has turbo support only for the Processor Graphics cores. It does not support Intel Turbo Boost Technology on the CPU Core.

For package turbo parameters on all other mobile SKUs, refer to the *2nd Generation Intel® Core™ Processor Family Mobile External Design Specification (EDS), Volume 1 #445463.*

Table 6. Package Turbo Parameters Information

Segment	Symbol	Package Turbo Parameter	Min	H/W Default	Max	Units
Single Core Intel® Celeron® processor ULV (1 Core ULV)	Turbo Time Parameter (Package)	Processor turbo long duration time window (POWER_LIMIT_1_TIME in TURBO_POWER_LIMIT MSR 0610h bits [23:17])	0.001	28	32	S
	Long P (Package)	Long duration turbo power limit (POWER_LIMIT_1 in TURBO_POWER_LIMIT MSR 0610h bits [14:0])	8	10	12	W
	Short P (package)	Short duration turbo power limit (POWER_LIMIT_2 in TURBO_POWER_LIMIT MSR 0610h bits [46:32])	8	10 x 1.25	16	W

1.7 DC Specifications

The following DC specifications apply to the **Intel® Celeron® Processor 807UE SKU**. It is also referred to as the Single Core Ultra-Low Voltage or "1 Core ULV" segment. Specifications that are different from the 2 Core 17 Watt ULV segment are shown in bold blue.

For DC Electrical specifications on all other mobile SKUs, refer to the *2nd Generation Intel® Core™ Processor Family Mobile External Design Specification (EDS), Volume 1 #445463.*

The processor DC specifications in this section are defined at the processor pins, unless noted otherwise.

See the *2nd Generation Intel® Core™ Processor Family Mobile – External Design Specification (EDS) Volume 1 of 2 (*or the *2nd Generation Intel® Core™ Processor Family Mobile – Datasheet - Volume 1 of 2)* Chapter 8 for the processor pin listings and Chapter 7 for signal definitions.

- Table 7 below lists the DC specifications for the processor and are valid only while meeting specifications for junction temperature, clock frequency, and input voltages. Care should be taken to read all notes associated with each parameter.
- AC tolerances for all DC rails include dynamic load currents at switching frequencies up to 1 MHz.

1.7.1 Voltage and Current Specifications

Table 7. Processor Core (VCC) Active and Idle Mode DC Voltage and Current Specifications

Symbol	Parameter	Segment	Min	Typ	Max	Unit	Note
HFM_VID	VID Range for Highest Frequency Mode (HFM)	1 Core ULV	**0.7**	–	**1.1**	V	1, 2, 6, 8
LFM_VID	VID Range for Lowest Frequency Mode (LFM)	1 Core ULV	0.65	–	0.9	V	1, 2, 8
V_{CC}	V_{CC} for processor core	1 Core ULV	0.3 – 1.52			V	2, 3, 11
I_{CCMAX}	Maximum Processor Core I_{CC}	1 Core ULV	–	–	**12.0**	A	4, 6, 8
I_{CC_TDC}	Thermal Design I_{CC}	1 Core ULV	–	–	**10.0**	A	5, 6, 8
I_{CC_LFM}	I_{CC} at LFM	1 Core ULV	–	–	**8.0**	A	5
$I_{C6/C7}$	I_{CC} at C6/C7 Idle-	1 Core ULV	–	–	2.6	A	10

Symbol	Parameter	Segment	Min	Typ	Max	Unit	Note
	state						
TOL_{VCC}	Voltage Tolerance	PS0	—	—	±15	mV	7, 9
		PS1	—	—	±12		
		PS2, PS3	—	—	±11.5		
Ripple	Ripple Tolerance	PS0 & Icc > TDC+30%	—	—	±15	mV	7, 9
		PS0 & Icc ≤ TDC+30%	—	—	±10		
		PS1	—	—	±13		
		PS2	—	—	-7.5 / +18.5		
		PS3	—	—	-7.5 / +27.5		
VR Step	VID resolution	1 Core ULV	—	5	—	mV	
$SLOPE_{LL}$	Processor Loadline	1 Core ULV	—	-2.9	—	mΩ	

NOTES:

1. Unless otherwise noted, all specifications in this table are based on post-silicon estimates and simulations or empirical data.
2. Each processor is programmed with a maximum valid voltage identification value (VID), which is set at manufacturing and cannot be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. Note that this differs from the VID employed by the processor during a power or thermal management event (Intel Adaptive Thermal Monitor, Enhanced Intel SpeedStep Technology, or Low Power States).
3. The voltage specification requirements are measured across VCC_SENSE and VSS_SENSE lands at the socket with a 100-MHz bandwidth oscilloscope, 1.5 pF maximum probe capacitance, and 1-M□ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe.
4. Processor core VR to be designed to electrically support this current.
5. Processor core VR to be designed to thermally support this current indefinitely.
6. This specification assumes that Intel Turbo Boost Technology is enabled.
7. Long term reliability cannot be assured if tolerance, ripple, and core noise parameters are violated.
8. Long term reliability cannot be assured in conditions above or below Max/Min functional limits.
9. PSx refers to the voltage regulator power state as set by the SVID protocol. Refer to the Huron River Platform Power Delivery Design Guide for more information.
10. Idle power specification is measured under temperature condition of 35 °C.

11. Refer Huron River Platform Power Delivery Design Guide for the minimum, typical, and maximum V_{CC} allowed for a given current.

Table 8. Processor Uncore (V_{CCIO}) Supply DC Voltage and Current Specifications

Symbol	Parameter	Segment	Min	Typ	Max	Unit	Note
V_{CCIO}	Voltage for the memory controller and shared cache defined at the motherboard V_{CCIO_SENSE} and $V_{SS\_SENSE\_VCCIO}$	1 Core ULV	—	1.05	—	V	
TOL_{CCIO}	V_{CCIO} Tolerance defined across V_{CCIO_SENSE} and $V_{SS\_SENSE\_VCCIO}$	1 Core ULV	DC: ±2% including ripple AC: ±3%			%	
I_{CCMAX_VCCIO}	Max Current for V_{CCIO} Rail	1 Core ULV	—	—	**3.0**	A	
I_{CCTDC_VCCIO}	Thermal Design Current (TDC) for V_{CCIO} Rail	1 Core ULV	—	—	**3.0**	A	

Note: Long term reliability cannot be assured in conditions above or below Max/Min functional limits.

Table 9. Memory Controller (V_{DDQ}) Supply DC Voltage and Current Specifications

Symbol	Parameter	Segment	Min	Typ	Max	Unit	Note
V_{DDQ}(DC+AC)	Processor I/O supply voltage for DDR3 (DC + AC specification)	1 Core ULV	—	1.5	—	V	
TOL_{DDQ}	V_{DDQ} Tolerance	1 Core ULV	DC= ±3% AC= ±2% AC+DC= ±5%			%	
I_{CCMAX_VDDQ}	Max Current for V_{DDQ} Rail	1 Core ULV	—	—	**2.5**	A	1
$I_{CCAVG\_VDDQ\ (Standby)}$	Average Current for V_{DDQ} Rail during Standby	1 Core ULV	—	66	133	mA	

NOTES:
1. The current supplied to the SO-DIMM modules is not included in this specification.

Table 10. System Agent (V_{CCSA}) Supply DC Voltage and Current Specifications

Symbol	Parameter	Segment	Min	Typ	Max	Unit	Note
V_{CCSA}	Voltage for the System Agent and V_{CCSA_SENSE}	1 Core ULV	0.75	—	0.90	V	

Symbol	Parameter	Segment	Min	Typ	Max	Unit	Note
TOL_{CCSA}	V_{CCSA} Tolerance	1 Core ULV	AC+DC= ±5%			%	
I_{CCMAX_VCCSA}	Max Current for V_{CCSA} Rail	1 Core ULV	—	—	**3**	A	
I_{CCTDC_VCCSA}	Thermal Design Current (TDC) for V_{CCSA} Rail	1 Core ULV	—	—	**3**	A	
Slew Rate	Voltage Ramp rate (dV/dT)	1 Core ULV	0.5	—	10	mV/us	

Note: Long term reliability cannot be assured in conditions above or below Max/Min functional limits.

Table 11. Processor PLL (V_{CCPLL}) Supply DC Voltage and Current Specifications

Symbol	Parameter	Segment	Min	Typ	Max	Unit	Note
V_{CCPLL}	PLL supply voltage (DC + AC specification)	1 Core ULV	—	1.8	v	V	
TOL_{CCPLL}	V_{CCPLL} Tolerance	1 Core ULV	AC+DC= ±5%			%	
I_{CCMAX_VCCPLL}	Max Current for V_{CCPLL} Rail	1 Core ULV	—	—	1.2	A	
I_{CCTDC_VCCPLL}	Thermal Design Current (TDC) for V_{CCPLL} Rail	1 Core ULV	—	—	1.2	A	

Note: Long term reliability cannot be assured in conditions above or below Max/Min functional limits.

Table 12. Processor Graphics (V_{AXG}) Supply DC Voltage and Current Specifications

Symbol	Parameter	Segment	Min	Typ	Max	Unit	Note[1]
GFX_VID	Active VID Range for V_{AXG}	1 Core ULV	0.65	—	1.35	V	2, 3, 5
VAXG	Processor Graphics core voltage	1 Core ULV	0 – 1.52			V	
I_{CCMAX_VAXG}	Max Current for Processor Graphics Rail	1 Core ULV	—	—	**11.0**	A	5
I_{CCTDC_VAXG}	Thermal Design Current (TDC) for Processor Graphics Rail	1 Core ULV	—	—	**5.5**	A	5

Symbol	Parameter	Segment	Min	Typ	Max	Unit	Note[1]
TOL_{AXG}	V_{AXG} Tolerance		PS0,PS1	—	±15	mV	4
			PS2,PS3	—	±11.5	mV	4
Ripple	Ripple Tolerance		PS0, PS1	—	±18	mV	4
			PS2	—	-7.5/+18.5	mV	4
			PS3	—	-7.5/+27.5	mV	
LL_{AXG}	V_{AXG} Loadline	1 Core ULV	-4.6			mΩ	

NOTES:
1. Unless otherwise noted, all specifications in this table are based on post-silicon estimates and simulations or empirical data.
2. Each processor is programmed with a maximum valid voltage identification value (VID), which is set at manufacturing and cannot be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. Note that this differs from the VID employed by the processor during a power or thermal management event (Intel Adaptive Thermal Monitor, Enhanced Intel SpeedStep Technology, or Low Power States).
3. The voltage specification requirements are measured across VCC_SENSE and VSS_SENSE lands at the socket with a 100-MHz bandwidth oscilloscope, 1.5 pF maximum probe capacitance, and 1-MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe.
4. PSx refers to the voltage regulator power state as set by the SVID protocol. Refer to the Huron River Platform Power Delivery Design Guide for more information.
5. Refer to the Huron River Platform Power Delivery Design Guide for the minimum, typical, and maximum V_{AXG} allowed for a given current.
6. Each processor is programmed with a maximum valid voltage identification value (VID), which is set at manufacturing and cannot be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. Note that this differs from the VID employed by the processor during a power or thermal management event (Intel Adaptive Thermal Monitor, Enhanced Intel SpeedStep Technology, or Low Power States).

1.8 Package

Table 13 and Table 14 provide the package information for the processor, pin information and the ball map for the Sandy Bridge- Mbl+ECC processor in the 1023 ball BGA package. For the X-Y coordinates of the pins please check the symbol files mentioned in the documents section.

Table 13. Processor Package Information

Item	Description	Sandy Bridge Mobile BGA	Sandy Bridge Mobile rPGA
Part Marking Code	The part marking code would be any text printed on the outside of the device that would uniquely identify it as the correct part. For example a Quad Ethernet Phy device may be marked with NH82580. This is used by our inspection to confirm that the correct devices have been received and fitted. We are not interested in date codes or manufacturing codes etc.	Both PGA and BGA will be marked per Intel standards with the substrate SLI, QDF, FPO etc. There is no room on the BGA for the full mark content	Please confirm with planning on the final ISET content as this is not determined by ATD
Terminal Finish	The Terminal finish in this case would be the chemical composition of the balls.	BGA has SnAgCu balls	Gold plated Cu pins
Lead Frame Material	Lead frame material may not be relevant in this case; it depends of the construction methods used by Intel. For the lead frame material I was interested in the chemical composition of any frame that may be used to connect the die to the balls on the BGA. For other package types it is often copper.	No lead frame in either BGA or PGA	No lead frame
The Moisture Sensitivity Level		Level 3	This is a socketed part and is not reflowed

Table 14. Sandy Bridge-Mbl+ECC Processor Pin Listing for the BGA1023 Package

PEG_RX#[8]	A11
VSS	A13
PEG_TX#[9]	A15
VSS	A17
PEG_RX#[4]	A19
VSS	A21
PEG_TX[1]	A23
VSS	A25
VCC	A26
VSS	A28

VCC	A29
VCC	A31
VSS	A33
VCC	A34
VCC	A35
VSS	A37
VCC	A38
VCC	A39
DC_TEST_A4	A4
VSS	A40

VCC	A42
VIDALERT#	A44
VSS	A45
PECI	A48
VSS	A49
VSS_NCTF	A5
CFG[4]	A51
VSS	A53
CFG[8]	A55
VSS_NCTF	A57
DC_TEST_A58	A58
DC_TEST_A59	A59
DC_TEST_A61	A61
PEG_RX#[11]	A8
VSS	A9
VSS	AA1
FDI0_LSYNC	AA10
FDI0_FSYNC	AA11
VSS	AA13
VCCIO	AA14
VCCIO	AA15
FDI1_TX[2]	AA3
DP_TX[1]	AA4
VAXG	AA46
VSS	AA50
VSS	AA51
VSS	AA52
VSS	AA53
VSS	AA55
VSS	AA56
FDI0_TX#[3]	AA6
FDI0_TX[3]	AA7
VSS	AA8
VSS	AB16
VCCIO	AB17
VSS	AB18

VCCIO	AB20
VSS	AB21
VAXG	AB47
VSS	AB48
VAXG	AB50
VAXG	AB51
VAXG	AB52
VAXG	AB53
VAXG	AB55
VAXG	AB56
VAXG	AB58
VAXG	AB59
VSS	AB61
DP_TX[0]	AC1
VSS	AC10
FDI1_FSYNC	AC12
VCCIO	AC13
VSS	AC14
DP_TX#[0]	AC3
DP_TX#[1]	AC4
VSS	AC46
VSS	AC6
VAXG	AC61
FDI1_TX[3]	AC8
FDI1_TX#[3]	AC9
VCCIO	AD16
VSS	AD17
VCCIO	AD18
DP_ICOMPO	AD2
VSS	AD20
VCCIO	AD21
VSS	AD4
VAXG	AD47
VAXG	AD48
VAXG	AD50
VAXG	AD51

VAXG	AD52
VAXG	AD53
VAXG	AD55
VAXG	AD56
VAXG	AD58
VAXG	AD59
VSS	AD61
DP_TX[2]	AE10
DP_TX#[2]	AE11
VSS	AE13
VCCIO	AE14
VCCIO	AE15
VAXG	AE46
DP_TX[3]	AE6
DP_TX#[3]	AE7
VSS	AE8
VSS	AF1
VCCIO	AF16
VSS	AF17
VCCIO	AF18
VCCIO	AF20
VSS	AF21
DP_COMPIO	AF3
DP_AUX	AF4
VCCIO	AF46
VSS	AF47
VSS	AF48
VSS	AF50
VSS	AF51
VSS	AF52
VSS	AF53
VSS	AF55
VSS	AF56
VSS	AF58
VSS	AF59
SB_DQ[62]	AF61

DPLL_REF_SSCLK#	AG1
VSS	AG10
DP_HPD	AG11
RSVD	AG13
VSS	AG14
VCCIO	AG15
VCCIO	AG16
VCCIO	AG17
VSS	AG18
VCCIO	AG20
VCCIO	AG21
DPLL_REF_SSCLK	AG3
DP_AUX#	AG4
VSS	AG47
VCCIO	AG48
VCCIO	AG50
VCCIO	AG51
VSS	AG52
SA_DQ[59]	AG53
SA_DQ[62]	AG55
SA_DQ[58]	AG56
SB_DQ[58]	AG58
SB_DQ[59]	AG59
SA_DQ[0]	AG6
VSS	AG61
VSS	AG7
FDI1_LSYNC	AG8
RSVD	AH2
VSS	AH4
VSS	AH58
SB_DQ[63]	AH60
SA_DQ[4]	AJ10
SA_DQS[0]	AJ11
VSS	AJ13
VCCIO	AJ14
VCCIO	AJ15

VSS	AJ16
VCCIO	AJ17
VSS	AJ20
VCCIO	AJ21
VSS	AJ22
VCCIO	AJ25
VSS	AJ26
VDDQ	AJ28
VSS	AJ30
VDDQ	AJ33
VSS	AJ34
VDDQ	AJ36
VSS	AJ38
VDDQ	AJ40
VSS	AJ42
VCCIO	AJ43
VSS	AJ45
VCCIO	AJ47
VSS	AJ48
SA_DQ[1]	AJ6
VSS	AJ7
SA_DQ[5]	AJ8
VSS	AK1
SB_DQ[5]	AK3
SB_DQ[4]	AK4
VCCIO	AK50
VCCIO	AK51
VSS	AK52
SA_DQS[7]	AK54
SA_DQS#[7]	AK55
SA_DQ[63]	AK56
SB_DQ[56]	AK58
SB_DQS#[7]	AK59
SB_DQS[7]	AK61
SB_DQ[1]	AL1
VSS	AL10

SA_DQS#[0]	AL11
VSS	AL13
VCCIO	AL14
VCCIO	AL15
VCCIO	AL16
VSS	AL17
VCCIO	AL20
VSS	AL21
VCCIO	AL22
VSS	AL25
VCCIO	AL26
VSS	AL28
SB_DQS#[0]	AL3
VDDQ	AL30
VSS	AL33
VDDQ	AL34
VSS	AL36
VDDQ	AL38
SB_DQ[0]	AL4
VSS	AL40
VDDQ	AL42
VSS	AL43
VCCIO	AL45
VSS	AL47
VCCIO	AL48
SB_DQ[57]	AL58
SB_DQ[61]	AL59
SA_DQ[3]	AL6
VSS	AL61
SA_DQ[7]	AL7
SA_DQ[6]	AL8
VSS	AM13
RSVD	AM14
RSVD	AM15
VCCIO	AM16
VCCIO	AM17

SB_DQS[0]	AM2
VSS	AM20
VCCIO	AM21
VSS	AM22
VCCPQE	AM25
VSS	AM26
VCCDQ	AM28
VSS	AM30
VDDQ	AM33
VSS	AM34
VDDQ	AM36
VSS	AM38
VSS	AM4
VDDQ	AM40
VSS	AM42
VCCIO	AM43
VSS	AM45
VCCIO	AM47
VSS	AM48
VSS	AM58
SB_DQ[60]	AM60
VSS	AN1
VCCIO_SENSE	AN16
VSSIO_SENSE	AN17
VCCIO	AN20
VSS	AN21
VCCPQE	AN22
VSS	AN25
VCCDQ	AN26
VSS	AN28
SB_DQ[2]	AN3
VDDQ	AN30
VSS	AN33
VDDQ	AN34
VSS	AN36
VDDQ	AN38

SB_DQ[6]	AN4
VSS	AN40
VCCIO	AN42
VSS	AN43
VCCIO	AN45
VSS	AN47
VCCIO	AN48
VSS	AN50
SA_DQ[61]	AN52
SA_DQ[57]	AN53
VSS	AN54
SA_DQ[60]	AN55
SA_DQ[56]	AN57
SB_DQ[54]	AN58
SB_DQ[51]	AN59
SB_DQ[50]	AN61
VSS	AP10
SA_DQ[2]	AP11
SA_DQ[50]	AP50
VSS	AP51
SA_DQ[55]	AP52
SA_DQ[51]	AP53
VSS	AP55
SA_DQ[54]	AP56
SA_DQ[9]	AP6
VSS	AP7
SA_DQ[13]	AP8
SB_DQ[7]	AR1
SA_DQS[1]	AR10
SA_DQ[8]	AR11
VSS	AR13
SA_DQ[25]	AR14
VSS	AR17
SA_DQ[27]	AR19
VSS	AR21
SB_CKE[0]	AR22

VDDQ	AR26
VDDQ	AR28
SB_DQ[13]	AR3
VDDQ	AR30
VDDQ	AR32
VDDQ	AR34
VDDQ	AR36
SB_DQ[3]	AR4
VDDQ	AR40
VSS	AR41
SA_DQ[33]	AR43
SA_DQ[37]	AR45
VSS	AR48
SB_DQ[55]	AR58
SB_DQS[6]	AR59
SA_DQ[12]	AR6
VSS	AR61
VSS	AR7
SA_DQS#[1]	AR8
SA_DQ[14]	AT13
VSS	AT14
SA_DQS#[3]	AT17
VSS	AT19
SB_DQ[9]	AT2
SA_DQ[66]	AT21
SB_BS[2]	AT22
SB_MA[14]	AT26
SB_MA[11]	AT28
SM_DRAMRST#	AT30
SA_MA[7]	AT32
SA_MA[4]	AT34
VSS	AT36
VSS	AT4
SA_CLK[1]	AT40
SA_WE#	AT41
SB_ODT[0]	AT43

VSS	AT45
SA_DQ[38]	AT48
RSVD	AT49
VSS	AT52
SA_DQ[53]	AT54
SA_DQS#[6]	AT55
SA_DQS[6]	AT56
VSS	AT58
SB_DQS#[6]	AT60
VSS	AU1
VSS	AU11
SA_DQ[15]	AU13
SA_DQ[29]	AU14
SA_DQS[3]	AU17
SA_DQS#[8]	AU19
SA_DQS[8]	AU21
SB_MA[15]	AU22
SA_MA[15]	AU26
VSS	AU28
SB_DQ[12]	AU3
SB_MA[3]	AU30
VSS	AU32
SA_MA[5]	AU34
SA_CLK[0]	AU36
SB_DQ[8]	AU4
SA_CLK#[1]	AU40
SA_DQ[45]	AU49
VSS	AU51
SB_DQ[49]	AU58
SB_DQ[52]	AU59
SA_DQ[10]	AU6
SB_DQ[53]	AU61
VSS	AU7
SB_DQS[1]	AV1
SA_DQS#[2]	AV11
SA_DQ[24]	AV14

VSS	AV17
SA_DQ[65]	AV19
VSS	AV21
VSS	AV22
SB_MA[12]	AV28
SB_DQS#[1]	AV3
SB_MA[5]	AV30
SA_MA[9]	AV32
VSS	AV34
SA_CLK#[0]	AV36
SB_DQ[10]	AV4
VSS	AV40
VDDQ	AV41
SB_CAS#	AV43
SA_DQS#[4]	AV45
VSS	AV48
SA_DQ[41]	AV49
SA_DQS[5]	AV51
SA_DQ[52]	AV54
VSS	AV55
SA_DQ[49]	AV56
SA_DQ[11]	AV9
VSS	AW13
VDDQ	AW26
SA_MA[13]	AW41
VSS	AW43
SA_DQS[4]	AW45
SA_DQ[34]	AW48
SB_DQ[48]	AW58
SB_DQ[47]	AW59
VSS	AW61
VSS	AW7
SA_DQS[2]	AY11
SA_DQ[23]	AY13
VSS	AY14
SA_DQ[26]	AY17

VSS	AY19
SB_DQ[14]	AY2
SA_DQ[69]	AY21
SA_DQ[71]	AY22
SA_CKE[0]	AY26
SA_MA[14]	AY28
VSS	AY30
SA_MA[8]	AY32
SB_CLK#[0]	AY34
VSS	AY36
VSS	AY4
SA_ODT[0]	AY40
VSS	AY41
SM_VREF	AY43
VSS	AY45
SA_DQ[39]	AY48
VSS	AY49
SA_DQS#[5]	AY51
SA_DQ[43]	AY53
VSS	AY55
VSS	AY58
SB_DQ[43]	AY60
VSS	AY9
PEG_RX#[9]	B10
PEG_RX#[6]	B14
PEG_TX[5]	B18
PEG_RX#[2]	B22
VIDSCLK	B43
UNCOREPWRGOOD	B46
CFG[0]	B50
CFG[2]	B54
PEG_RX#[12]	B6
VSS	BA1
VSS	BA11
SA_DQ[18]	BA13
SA_DQ[28]	BA14

VSS	BA17
SA_DQ[64]	BA19
VSS	BA21
SA_DQ[70]	BA22
VSS	BA26
SA_BS[2]	BA28
SB_DQ[15]	BA3
SA_MA[11]	BA30
VSS	BA32
SB_CLK[0]	BA34
SB_CLK[1]	BA36
SB_DQ[11]	BA4
VDDQ	BA40
SA_ODT[1]	BA41
VSS_SENSE_VDDQ	BA43
SA_DQ[32]	BA45
VSS	BA48
SA_DQ[40]	BA49
VSS	BA51
SA_DQ[46]	BA53
SA_DQ[48]	BA55
SB_DQ[46]	BA58
SB_DQS#[5]	BA59
SB_DQS[5]	BA61
SA_DQ[20]	BA7
SA_DQ[21]	BA9
SA_DQ[19]	BB11
SA_DQ[30]	BB14
SA_DQ[31]	BB17
SA_DQ[68]	BB19
SA_DQ[67]	BB21
SA_CKE[1]	BB26
VDDQ	BB28
VCCPLL	BB3
SA_MA[6]	BB32
SA_MA[1]	BB34

SB_CLK#[1]	BB36
SA_CS#[0]	BB40
SA_DQ[44]	BB49
SA_DQ[42]	BB51
VSS	BB53
SA_DQ[47]	BB55
SA_DQ[17]	BB7
SA_DQ[22]	BB9
VCCPLL	BC1
VSS	BC13
VCCIO_SEL	BC22
SA_MA[12]	BC30
VCCPLL	BC4
SA_CS#[1]	BC41
VDDQ_SENSE	BC43
SA_DQ[36]	BC45
SA_DQ[35]	BC48
VSS	BC5
VSS	BC57
SB_DQ[42]	BC59
VSS_NCTF	BC61
SA_DQ[16]	BC7
DC_TEST_BD1	BD1
SB_DQ[21]	BD10
VSS	BD12
SB_DQ[18]	BD13
SB_DQ[22]	BD14
VSS	BD16
SB_DQS#[3]	BD17
SB_DQS[3]	BD18
VSS	BD19
SB_DQ[64]	BD21
SB_DQ[65]	BD22
VSS	BD23
SB_DQ[66]	BD25
SB_DQ[67]	BD26

VSS	BD27
SB_MA[7]	BD29
VSS_NCTF	BD3
SB_MA[4]	BD30
VSS	BD32
SB_MA[2]	BD33
SA_MA[3]	BD35
VSS	BD36
SA_BS[0]	BD37
SA_RAS#	BD39
VSS	BD40
SB_BS[1]	BD42
SB_MA[10]	BD43
VSS	BD44
SB_WE#	BD45
SB_MA[13]	BD46
VSS	BD48
SB_DQ[36]	BD49
SB_DQ[32]	BD50
VSS	BD52
SB_DQ[34]	BD53
SB_DQ[38]	BD54
VSS	BD56
VSS_NCTF	BD59
DC_TEST_BD61	BD61
VSS	BD8
SB_DQ[17]	BD9
DC_TEST_BE1	BE1
SB_DQS[2]	BE11
SB_DQ[23]	BE13
SB_DQ[28]	BE14
SB_DQ[25]	BE17
SB_DQ[26]	BE18
SB_DQ[27]	BE21
SB_DQ[69]	BE22
SB_DQS[8]	BE24

SB_DQ[71]	BE26
SB_MA[9]	BE28
DC_TEST_BE3	BE3
SB_MA[8]	BE30
SB_MA[1]	BE33
SA_MA[2]	BE35
SA_MA[10]	BE37
SA_CAS#	BE39
VSS_NCTF	BE4
SB_CS#[0]	BE41
SM_RCOMP[1]	BE43
SM_DRAMPWROK	BE45
SB_CS#[1]	BE47
SB_DQ[37]	BE49
VSS	BE5
SB_DQS[4]	BE51
SB_DQ[39]	BE53
SB_DQ[44]	BE54
SB_DQ[41]	BE57
VSS_NCTF	BE58
DC_TEST_BE59	BE59
DC_TEST_BE61	BE61
RSVD	BE7
SB_DQ[16]	BE9
SB_DQ[19]	BF12
SB_DQ[24]	BF16
SB_DQ[31]	BF19
SB_DQS#[8]	BF23
SB_CKE[1]	BF27
SB_MA[0]	BF32
SA_BS[1]	BF36
SB_RAS#	BF40
SM_RCOMP[0]	BF44
SB_DQ[33]	BF48
SB_DQ[35]	BF52
SB_DQ[40]	BF56

SB_DQ[20]	BF8
DC_TEST_BG1	BG1
SB_DQS#[2]	BG11
VSS	BG13
SB_DQ[29]	BG14
VSS	BG17
SB_DQ[30]	BG18
VSS	BG21
SB_DQ[68]	BG22
VSS	BG24
SB_DQ[70]	BG26
VSS	BG28
DC_TEST_BG3	BG3
SB_MA[6]	BG30
VDDQ	BG33
SA_MA[0]	BG35
VSS	BG37
SB_BS[0]	BG39
DC_TEST_BG4	BG4
VSS	BG41
SM_RCOMP[2]	BG43
VSS	BG45
SB_ODT[1]	BG47
VSS	BG49
VSS_NCTF	BG5
SB_DQS#[4]	BG51
VSS	BG53
SB_DQ[45]	BG54
VSS_NCTF	BG57
DC_TEST_BG58	BG58
DC_TEST_BG59	BG59
DC_TEST_BG61	BG61
RSVD	BG7
VSS	BG9
PEG_RX[8]	C11
PEG_RX[6]	C13

PEG_TX[9]	C15
PEG_TX#[5]	C17
PEG_RX[4]	C19
PEG_RX[2]	C21
PEG_TX#[1]	C23
VCC	C26
VCC	C27
VSS	C29
VSS_NCTF	C3
VCC	C32
VCC	C34
VSS	C35
VCC	C37
VCC	C39
DC_TEST_C4	C4
VSS	C40
VCC	C42
VIDSOUT	C44
PROCHOT#	C45
PM_SYNC	C48
CATERR#	C49
PEG_RX[12]	C5
CFG[1]	C51
CFG[5]	C53
CFG[6]	C55
PROC_DETECT#	C57
VSS_NCTF	C58
DC_TEST_C59	C59
DC_TEST_C61	C61
PEG_RX[11]	C8
PEG_RX[9]	C9
DC_TEST_D1	D1
VSS	D10
PEG_RX[7]	D12
PEG_RX#[7]	D13
VSS	D14

PEG_RX[5]	D16
PEG_RX#[5]	D17
VSS	D18
PEG_RX[3]	D19
PEG_RX#[3]	D21
VSS	D22
PEG_TX#[2]	D23
PEG_TX[2]	D24
VSS	D26
VCC	D27
VSS	D29
DC_TEST_D3	D3
VCC	D32
VCC	D34
VSS	D35
VCC	D37
VCC	D39
VSS	D4
VSS	D40
VCC	D42
VSS	D43
RESET#	D44
THERMTRIP#	D45
VSS	D46
VCCSA_VID[0]	D48
VCCSA_VID[1]	D49
VSS	D50
CFG[16]	D52
CFG[3]	D53
VSS	D54
VSS	D58
VSS_NCTF	D59
VSS	D6
DC_TEST_D61	D61
PEG_TX[14]	D8
PEG_TX#[14]	D9

VSS_NCTF	E1
PEG_TX[8]	E14
PEG_TX[3]	E21
VSS	E25
VCC	E26
VCC	E28
VSS	E29
VSS	E3
VCC	E32
VCC	E34
VSS	E35
VCC	E37
VCC	E38
VSS	E40
PEG_RX#[14]	E5
BPM#[1]	E55
BPM#[2]	E59
VSS_NCTF	E61
PEG_TX#[13]	F10
VSS	F13
PEG_TX#[8]	F14
VSS	F15
PEG_TX#[7]	F17
VSS	F19
PEG_TX#[3]	F21
PEG_TX[0]	F22
VCC	F25
VCC	F26
VCC	F28
VSS	F29
VCC	F32
VCC	F34
VSS	F35
VCC	F37
VCC	F38
VSS	F40

VCC	F42
VCC_SENSE	F43
VAXG_SENSE	F45
RSVD	F48
SANDY BRIDGE_IVB#	F49
CFG[15]	F51
CFG[12]	F53
VSS	F55
PEG_RX[14]	F6
PEG_RX[10]	F8
PEG_ICOMPO	G1
PEG_TX[13]	G10
PEG_TX[11]	G13
PEG_TX[7]	G17
PEG_TX[4]	G19
PEG_TX#[0]	G22
PEG_ICOMPI	G3
PEG_RCOMPO	G4
VCC	G42
VSS_SENSE	G43
VSSAXG_SENSE	G45
VSS	G48
VSS	G51
CFG[13]	G53
BPM#[3]	G55
BPM#[0]	G58
BPM#[4]	G59
VSS	G6
VSS	G61
PEG_RX#[10]	G8
VSS	H10
PEG_TX#[11]	H13
VSS	H14
VSS	H17
PEG_TX#[4]	H19

BCLK#	H2
VSS	H21
PEG_RX#[0]	H22
VCC	H25
VCC	H26
VCC	H28
VCC	H29
VCC	H32
VCC	H34
VCC	H35
VCC	H37
VCC	H38
VSS	H4
VCC	H40
RSVD	H43
RSVD	H45
RSVD	H48
CFG[7]	H49
CFG[9]	H51
VSS	H53
VSS	H58
PEG_RX[13]	H6
BPM#[5]	H60
PEG_RX#[13]	H8
VSS	J1
PEG_TX#[10]	J14
PEG_RX#[1]	J21
VCC	J25
VCC	J26
VCC	J28
VCC	J29
BCLK	J3
VCC	J32
VCC	J34
VCC	J35
VCC	J37

VCC	J38
PEG_TX#[15]	J4
VCC	J40
VCC	J42
VSS	J49
VSS	J55
TRST#	J58
BPM#[6]	J59
BPM#[7]	J61
DMI_TX#[0]	K1
PEG_TX[12]	K10
VSS	K11
PEG_TX[10]	K13
PEG_TX#[6]	K15
PEG_TX[6]	K17
PEG_RX[1]	K19
VSS	K21
PEG_RX[0]	K22
RSVD	K24
VCC	K26
VCC	K27
VCC	K29
DMI_TX[0]	K3
VCC	K32
VCC	K34
VCC	K35
VCC	K37
VCC	K39
PEG_TX[15]	K4
VCC	K42
RSVD	K43
RSVD	K45
RSVD	K48
CFG[10]	K49
VSS	K51
CFG[11]	K53

DBR#	K58
PEG_RX[15]	K6
PEG_RX#[15]	K7
VSS	K8
VSS	L16
VCCSA	L17
VSS	L20
VCCSA	L21
VSS	L22
VCC	L25
VSS	L26
VCC	L28
VSS	L30
VCC	L33
VSS	L34
VCC	L36
VSS	L38
VCC	L40
RSVD	L42
VSS	L43
RSVD	L45
RSVD	L47
VSS	L48
CFG[14]	L51
CFG[17]	L53
TMS	L55
TCK	L56
TDO	L59
VSS	L61
PEG_TX#[12]	M10
VSS	M11
RSVD	M13
RSVD	M14
VSS	M15
DMI_RX#[0]	M2
VSS	M4

VSS	M58
VSS	M6
TDI	M60
DMI_TX[1]	M7
DMI_TX#[1]	M8
VSS	N1
VCCSA	N16
VSS	N17
VCCSA	N20
VSS	N21
VCCSA	N22
VSS	N25
VCC	N26
VSS	N28
DMI_RX[0]	N3
VCC	N30
VSS	N33
VCC	N34
VSS	N36
VCC	N38
DMI_TX#[2]	N4
VSS	N40
RSVD	N42
VSS	N43
VAXG	N45
VSS	N47
VSS	N48
RSVD	N50
VSS	N51
VSS	N52
PRDY#	N53
PREQ#	N55
VSS	N56
BCLK_ITP#	N58
BCLK_ITP	N59
VSS	N61

DMI_RX#[2]	P1
DMI_RX#[3]	P10
DMI_RX[3]	P11
RSVD	P13
VSS	P14
VSS	P16
VCCSA	P17
VSS	P18
VCCSA	P20
VSS	P21
DMI_RX[2]	P3
DMI_TX[2]	P4
VAXG	P47
VAXG	P48
VAXG	P50
VAXG	P51
VAXG	P52
VAXG	P53
VAXG	P55
VAXG	P56
VSS	P58
VSS	P59
DMI_RX#[1]	P6
VAXG	P61
DMI_RX[1]	P7
VSS	P9
VCCSA	R16
VSS	R17
VCCSA	R18
DMI_TX#[3]	R2
VSS	R20
VCCSA	R21
VSS	R4
VSS	R46
VSS	T1
DMI_TX[3]	T3

FDI1_TX[1]	T4
VSS	T47
VAXG	T48
VSS	T50
VSS	T51
VSS	T52
VSS	T53
VSS	T55
VSS	T56
VAXG	T58
VAXG	T59
VAXG	T61
VCCSA_SENSE	U10
FDI_INT	U11
VSS	U13
RSVD	U14
VCCSA	U15
VAXG	U46
FDI0_TX[0]	U6
FDI0_TX#[0]	U7
VSS	U8
VCCSA	V16
VCCSA	V17
VCCSA	V18
VSS	V20
VCCSA	V21
FDI1_TX#[1]	V4
VAXG	V47
VAXG	V48
VAXG	V50
VAXG	V51
VAXG	V52
VAXG	V53
VAXG	V55
VAXG	V56

VAXG	V58
VAXG	V59
VSS	V61
FDI0_TX#[2]	W1
FDI0_TX[1]	W10
FDI0_TX#[1]	W11
VSS	W13
RSVD	W14
VSS	W15
VCCIO	W16
VCCIO	W17
VSS	W18
VCCSA	W20
VSS	W21
FDI0_TX[2]	W3
VSS	W46
VAXG	W50
VAXG	W51
VAXG	W52
VAXG	W53
VAXG	W55
VAXG	W56
FDI1_TX#[0]	W6
VAXG	W61
FDI1_TX[0]	W7
VSS	W8
FDI1_TX#[2]	Y2
VSS	Y4
VSS	Y47
VAXG	Y48
VSS	Y58
VSS	Y59
VAXG	Y61

1.8.1 Sandy Bridge-Mbl + ECC Package Ball Map

Figure 2. Top Left Side

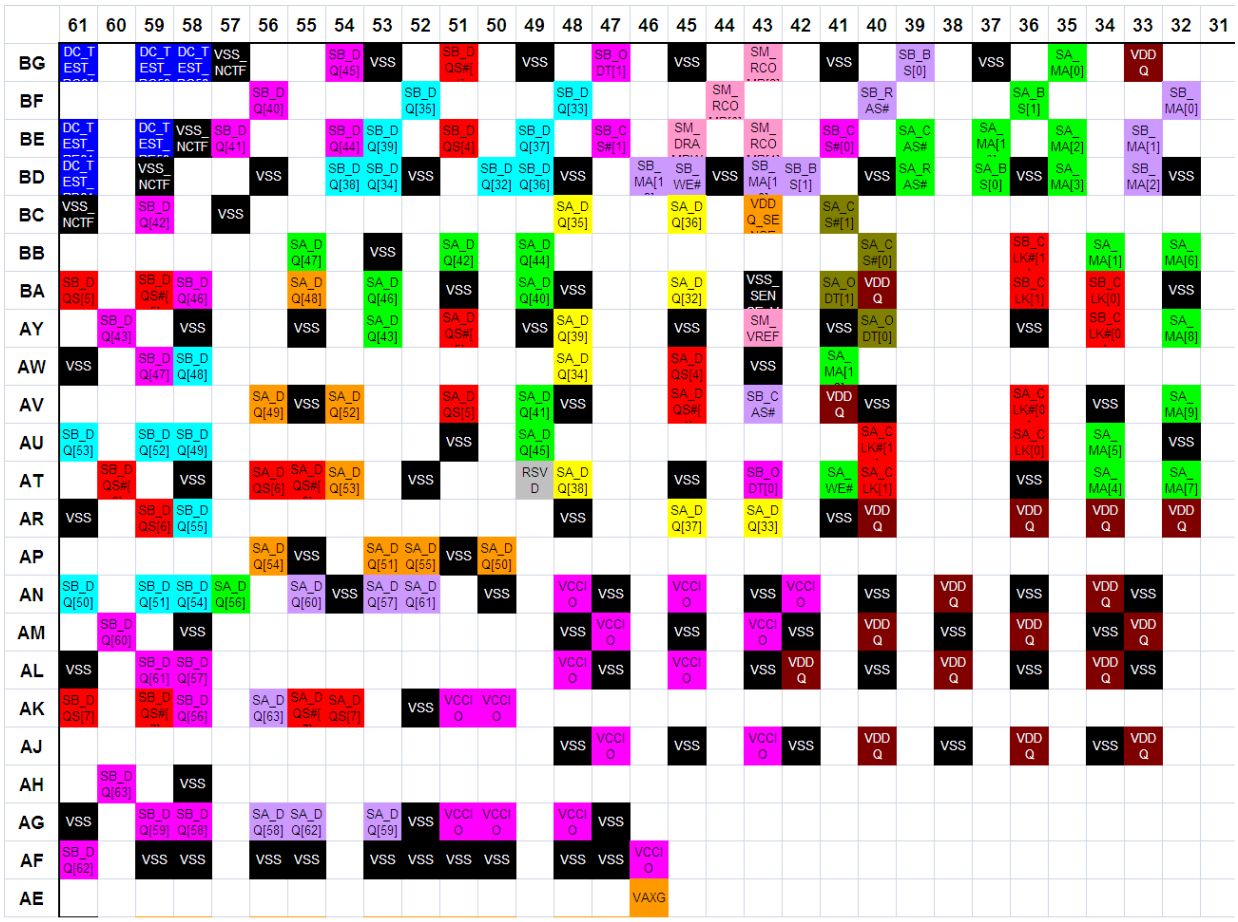


Figure 3. Top Right Side

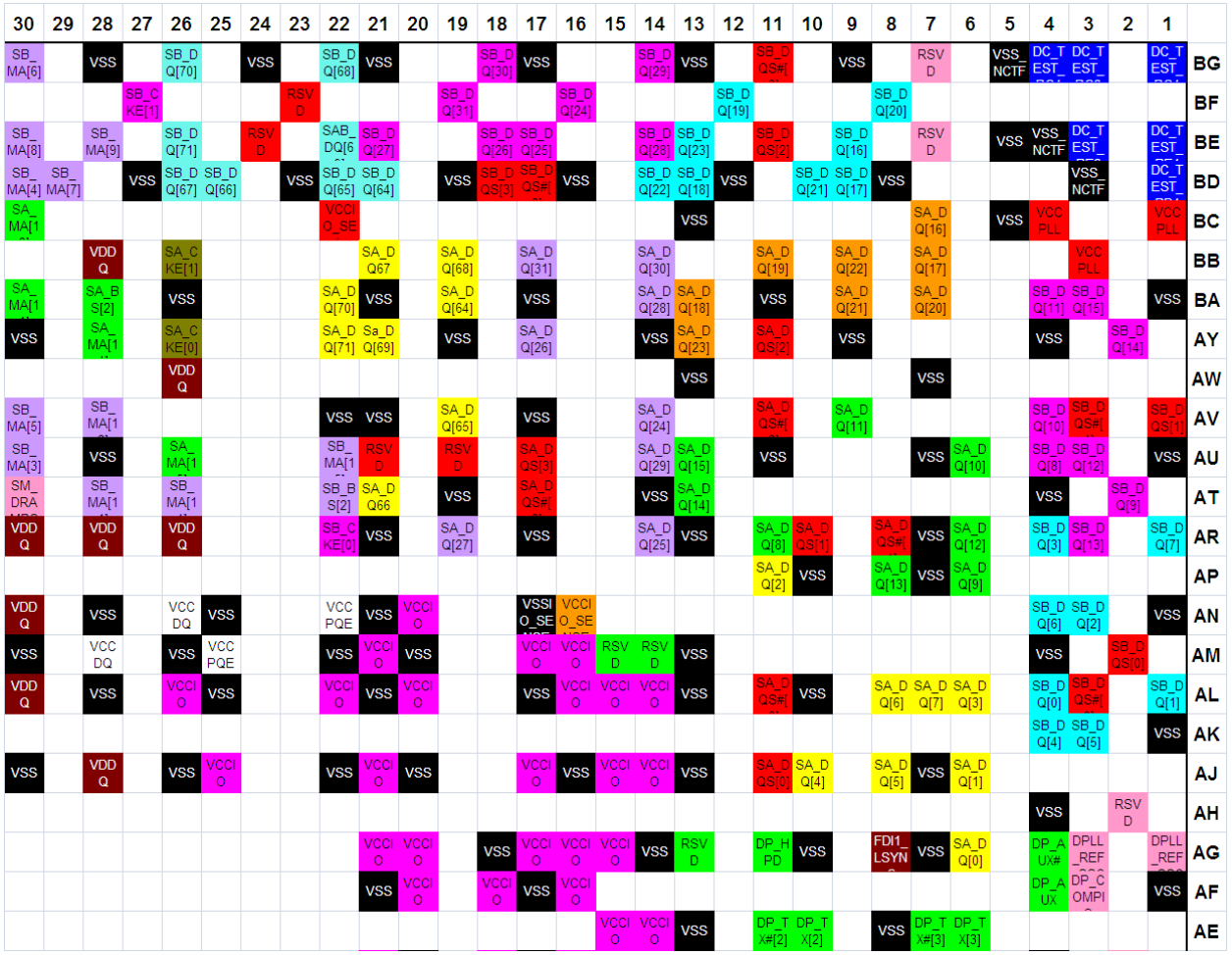
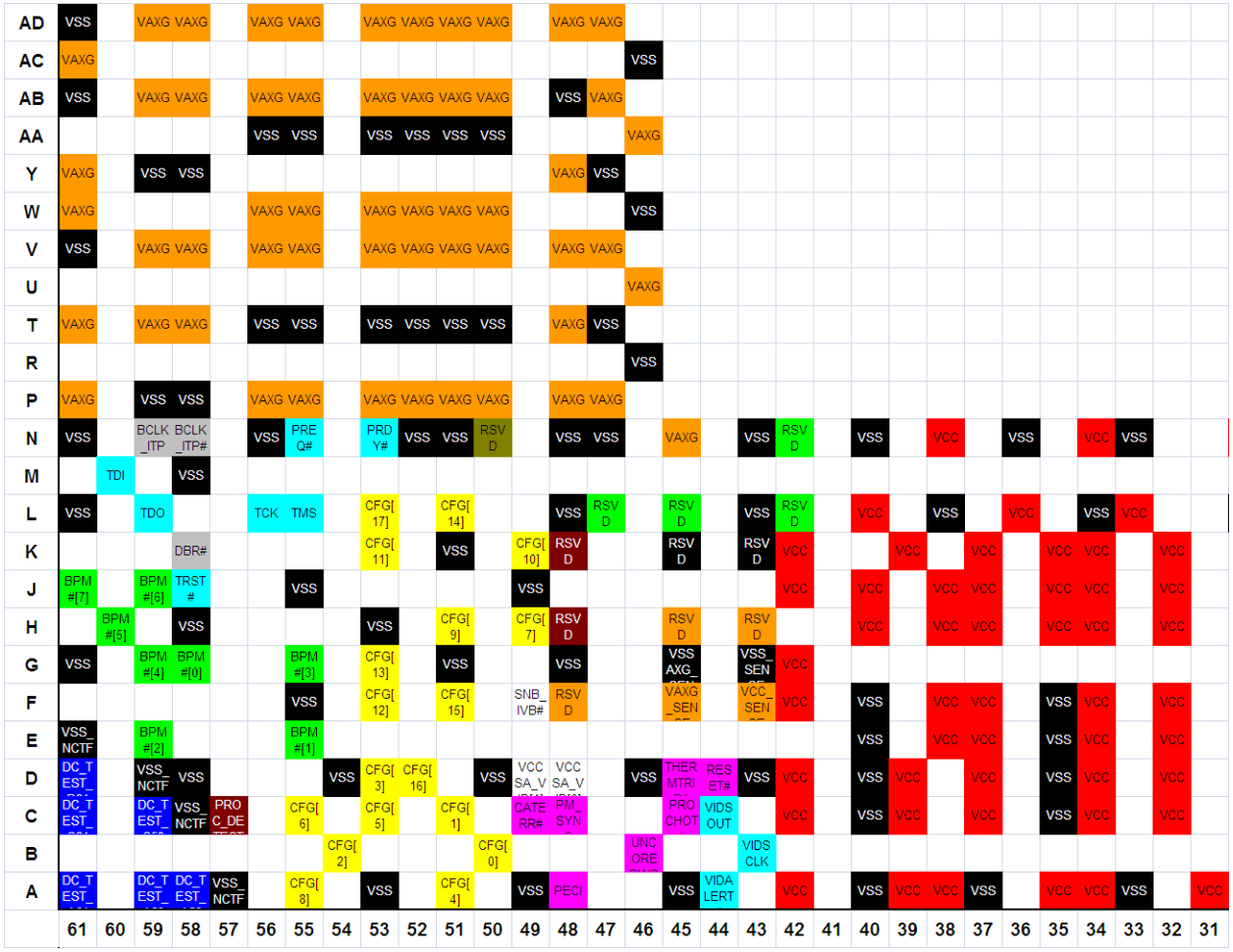


Figure 4. Bottom Ride Side

Figure 5. Bottom Left Side



Note - For the package mechanical details such as the pin metal/mask information and the coordinates of the pins please refer to the MAS document on IBL; Document number - 447158 - Manufacturing with Intel® [Huron River] Mainstream and Small Form Factor Platforms - Manufacturing Advantage Service (MAS) Presentation - rev 1.0

1.8.2 Package Mechanical Drawings

The following section contains the mechanical drawings for the BGA versions of the SNB-Mbl processor. Depending on the processor SKU, there are two versions of die available on the SNB-Mbl BGA package -- a four-core-die version and a two-core-die version. Both versions have the same 31 mm x 24 mm dimensions and 1023 ball configuration. The only differences are in the dimensions of the die on the top side of the package.

Remember to check the size differences between the two dies when designing your thermal solution.

The processors and their corresponding die-type are provided in Table 15 below.

Table 15. Sandy Bridge-Mbl+ECC BGA processor Sku Listing/Die type

Sandy Bridge –Mbl +ECC Sku	Die Type
Intel® Core™ i7-2715QE Processor 4C/6MB/2.1GHz/45W / HDG*3000	Four Core Die
Intel® Core™ i5-2515E Processor 2C/3MB/2.5GHz/35W / HDG*3000	Four Core Die
Intel® Core™ i3-2310E Processor 2C/3MB/2.1GHz/35W / HDG*3000	Four Core Die
Intel® Core™ i7-2655LE Processor 2C/4MB/2.2GHz/25W / HDG*3000	Four Core Die
Intel® Core™ i7-2610UE Processor 2C/3MB/1.5 GHz/17W / HDG*3000	Four Core Die
Intel® Core™ i3-2340UE Processor 2C/3MB/1.3GHz/17W / HDG*3000	Four Core Die
Intel®Celeron®B810E Processor 2C/2MB/1.6GHz/35W / HDG	Two Core Die
Intel® Celeron® 847E Processor 2C/2MB/1.1GHz/17W / HDG	Two Core Die
Intel®Celeron®827E Processor 1C/1.5MB/1.4GHz/17W / HDG	Two Core Die
Intel® Celeron® 807UE Processor 1C/1MB(Last Level Cache) 1GHz/10W(TDP) /HDG (Graphics)	Two Core Die

Figure 6. Sandy Bridge-Mbl +ECC Four-Core-Die 1023 Ball BGA Package Mechanical Drawing 1

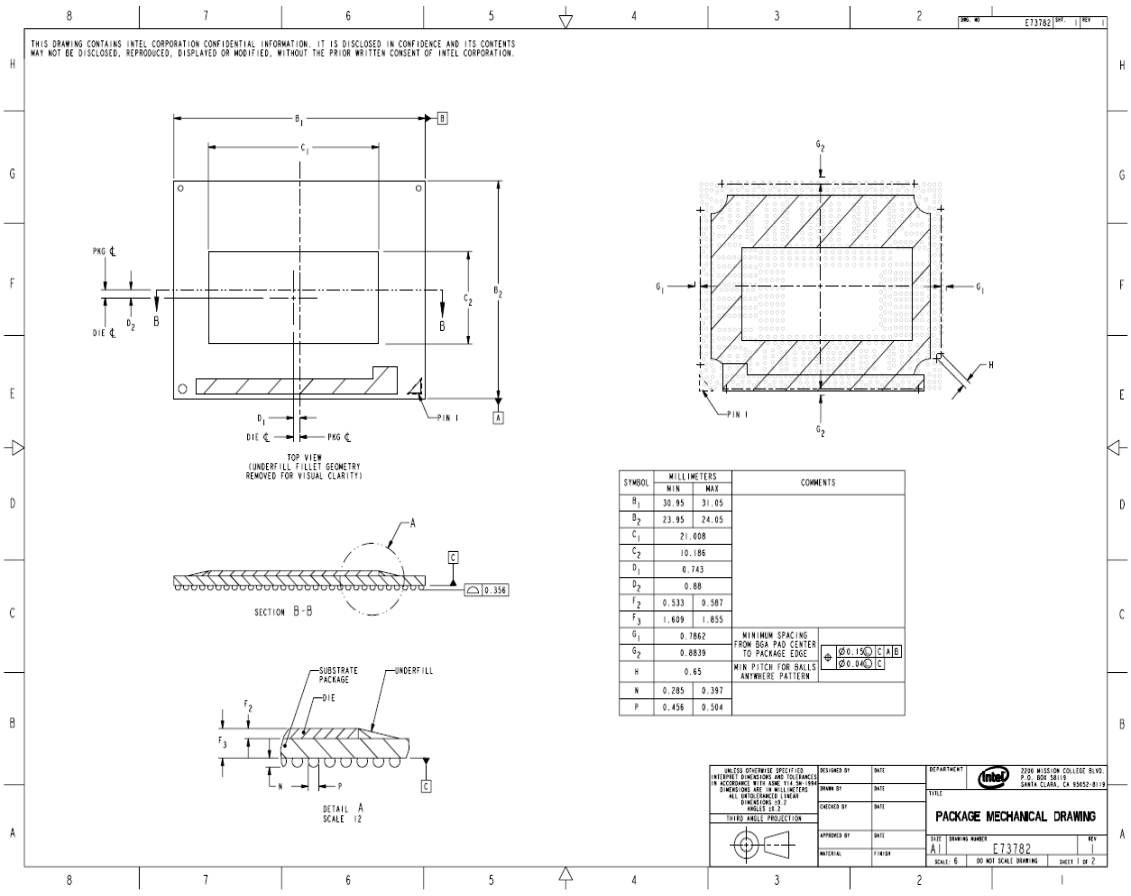


Figure 7. Sandy Bridge-Mbl +ECC Four-Core-Die 1023 Ball BGA Package Mechanical Drawing 2

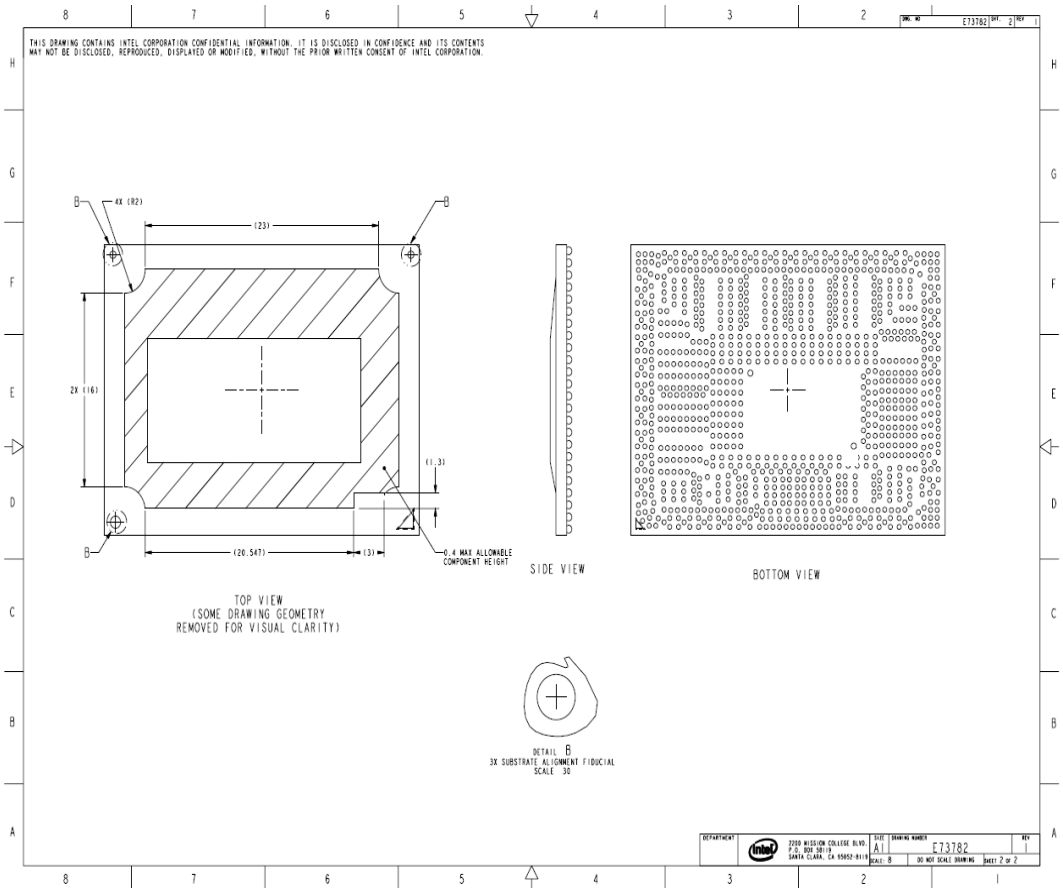


Figure 8. Sandy Bridge-Mbl Two-Core-Die 1023 Ball BGA Package Mechanical Drawing 1

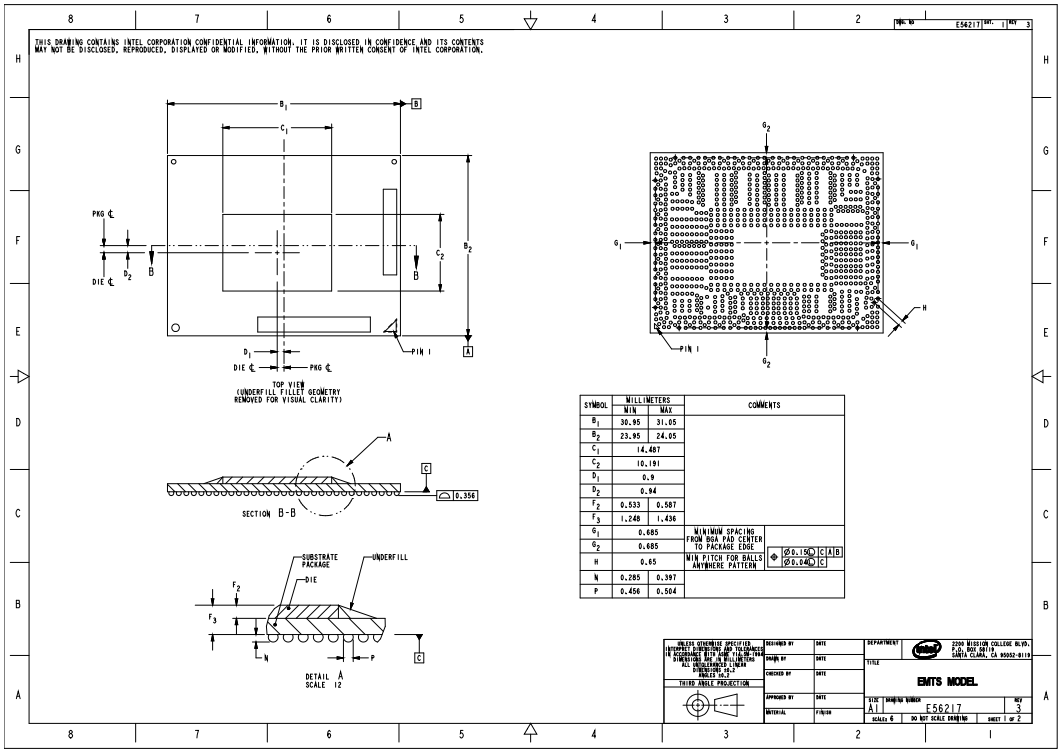


Figure 9. Sandy Bridge- Mbl BGA Two-Core-Die 1023 Ball Package Mechanical Drawing 2