Am186™CC/CH/CU Microcontroller Customer Development Platform

User's Manual

Order #22002B

AMD

Am186™CC/CH/CU Microcontroller Customer Development Platform User's Manual

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About the Am186™CC/CH/CU Microcontroller Customer Development Platform

The AMD Am186™CC/CH/CU microcontroller customer development platform (CDP) is a system used for customer evaluation and development for the Am186CC/CH/CU microcontrollers. The platform provides access to the major microcontroller interfaces and is an ideal tool for developing customer-specific applications by using the development module interface.

The CDP consists of two boards—a main board that contains the Am186CC communications controller and interfaces (shown in Figure 0-1), and the development module, which can be used for the development of various communications applications such as ISDN TAs and routers (shown in Figure 0-2).

The main board consists of a power supply that provides the necessary voltages for typical system applications of the Am186CC/CH/CU microcontroller. The main board also provides a glueless interface to Flash memory and DRAM or SRAM system main memory, communication interfaces such as a universal asynchronous receiver/transmitter (UART) and High-Speed UART, universal serial bus (USB), and four synchronous serial DCE connections. Other features include the debug interfaces that allow connection to the following:

- ROM-ICE
- Optional Test Interface Port (TIP) debug board
- HP logic analyzer headers to provide access to the Am186CC communications controller signals
- Expansion interface through the development module or the 104-pin Am186 processor expansion interface

The development module consists of an Am79C961A PCnet™-ISA II Ethernet Controller for 10BaseT Ethernet, an Am79C32A ISDN digital subscriber controller (DSC) circuit for an ISDN S/T connection, an ISDN U connection, and two POTS connections featuring the Am79C031 DSLAC™ device and two Am79R79 Ringing SLICs.

NOTE: Although the customer development board provides an Am186CC microcontroller, you can also use the board to develop Am186CH HDLC microcontroller applications and Am186CU USB microcontroller applications. The Am186CH and Am186CU microcontrollers support subsets of the Am186CC microcontroller features. The Am186CH HDLC microcontroller provides two HDLC channels and *does not* support USB or GCI. The Am186CU USB microcontroller *does not* support HDLC.

For more information about the Am186CC/CH/CU microcontrollers, refer to

- *Am186™CC/CH/CU Microcontroller User's Manual*, order #21914
- *Am186™CC Communications Controller Data Sheet*, order #21915
- *Am186™CH HDLC Microcontroller Data Sheet*, order #22024
- *Am186™CU USB Microcontroller Data Sheet*, order #22025
- *Am186™CC/CH/CU Microcontroller Register Set Manual*, order #21916

For more information about the CDP board features, refer to "Features" on page xvii, and Chapter 2, "Main Board Functional Description".

Main Board Block Diagram

Figure 0-1 shows the block diagram for the main board on the CDP.

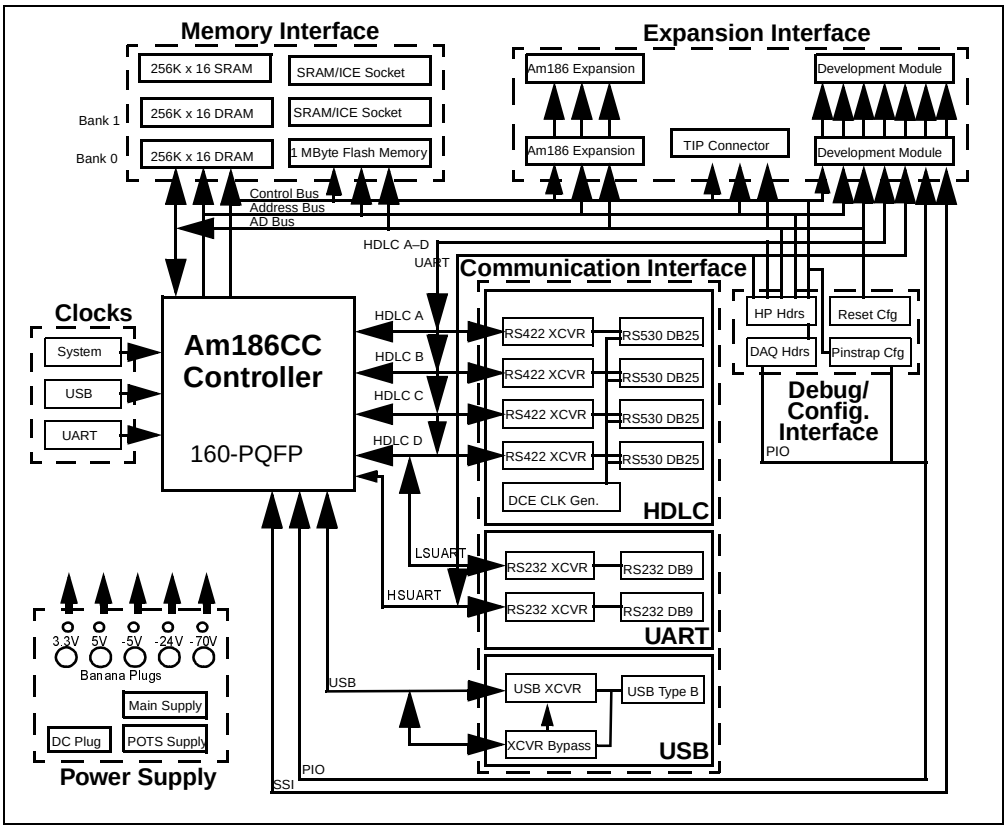


Figure 0-1. Main Board Block Diagram

Development Module Block Diagram

Figure 0-2 (or sheet 2 of the development module schematics included in your kit) shows the block diagram for the CDP's development module.

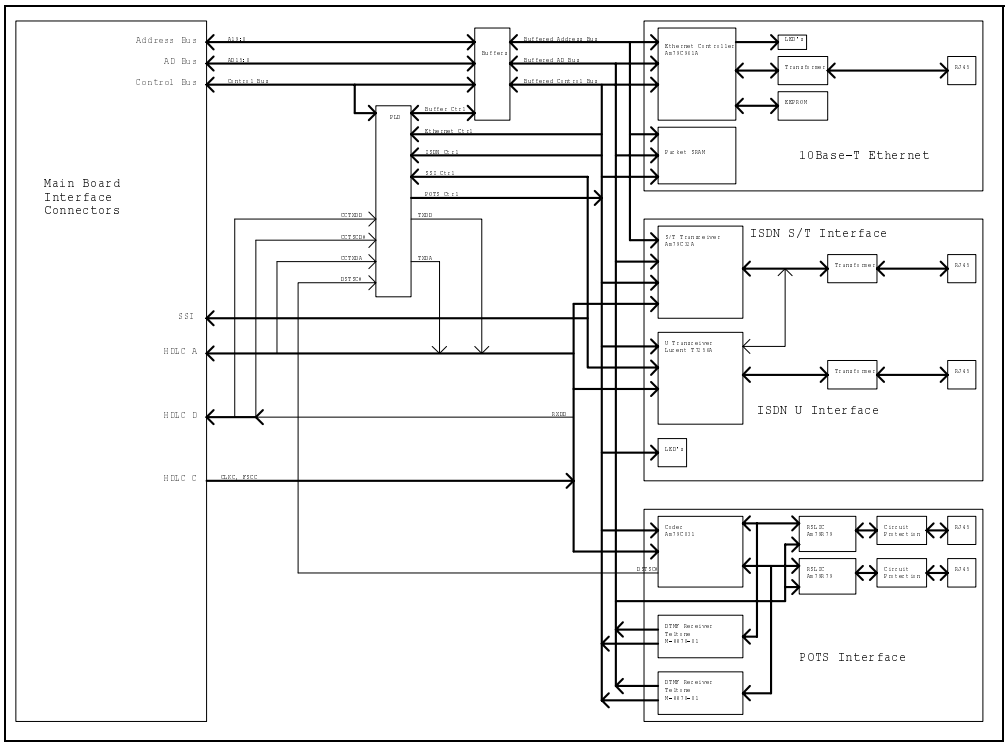


Figure 0-2. Router/ISDN Development Module Block Diagram

Theory of Operation

The Am186CC/CH/CU microcontroller CDP provides a comprehensive evaluation system to support Am186CC/CH/CU microcontroller-based designs. The combined features of the Am186CC/CH/CU microcontroller CDP offer designers a complete tool for hardware and software development with the Am186CC/CH/CU microcontrollers.

NOTE: If you are evaluating the Am186CH or Am186CU microcontroller, all of the features on the CDP are not available. The Am186CH and Am186CU microcontrollers support subsets of the Am186CC microcontroller features. The Am186CH HDLC microcontroller provides two HDLC channels and *does not* support USB or GCI. The Am186CU USB microcontroller *does not* support HDLC.

Features

The Am186CC/CH/CU microcontroller CDP provides the features described in the following sections.

Main Board

- Am186CC 3.3-V, 50-MHz Microcontroller
- Power Supply (generates 3.3 V, 5.0 V, -5.0 V, -24 V, and -70 V from a 12-V DC source)
- Memory Interfaces
  - Main system memory
    4-Mbit, 256K x 16, 40-ns EDO DRAM
    Two 1-Mbit 128K x 8, 35-ns SRAMs configured as 128K x 16
  - 8-Mbit configurable 512K x 16, or 1M x 8, 55-ns Flash memory

- Communication Interfaces
  - HDLC synchronous communications
    Four RS-422, DB-25 DCE/PCM connections clocked by the main board clock generator (Am186CH HDLC microcontroller supports only two connections)
    Dedicated 2 x 5 header for GCI (supported on Am186CC microcontroller only)
  - Peripheral USB port (supported on Am186CC and Am186CU microcontrollers only)
  - UARTs
    One 460-Kbaud, RS-232, DB-9 DCE connection
    One 120-Kbaud, RS-232, DB-9 DCE connection
- Debug and Configuration
  - 60-pin connector interface to the optional test interface port (TIP) debug board
  - Two 32-pin DIP sockets for use with a x16 ROM-ICE
  - Eight 2 x 10 shrouded headers to directly connect Am186CC/CH/CU microcontroller signals to HP analyzers
  - Two 4-segment switches to allow pinstrap configuration
  - Two 8-segment switches to allow system-specific configuration

Development Module

- 10BaseT Ethernet port
- ISDN interface
  - S/T interface
  - U interface
- Two POTS Interfaces

Documentation

The *Am186™CC/CH/CU Microcontroller Customer Development Platform User's Manual* provides information on the design and function of the Am186CC/CH/CU microcontroller CDP.

About This Manual

Chapter 1, "Quick Start" helps you quickly set up and start using the Am186CC/CH/CU microcontroller CDP.

Chapter 2, "Main Board Functional Description" describes the basic sections of the platform: layout, jumper and switch settings, microcontroller, power supply, memory interfaces, communication interfaces, debug and configuration, and development module.

Chapter 3, "Development Module Functional Description" describes the features and components on the development module, including a 10BaseT Ethernet port, ISDN interface, and POTS interfaces.

Appendix A, "Default Jumper and Switch Settings" provides a table with the default jumper and switch settings.

Appendix B, "Platform Pin Usage" provides tables describing the CDP's PIO, chip select, and interrupt pin usage.

Appendix C, "Main Board Bill of Materials" contains the bill of materials for the Am186CC/CH/CU microcontroller CDP main board.

Appendix D, "Development Module Bill of Materials" contains the bill of materials for the Am186CC/CH/CU microcontroller CDP module.

Appendix E, "PLD Equations" contains PLD code for the PLDs at locations U13, U20, and U24.

A standard index is also included.

Suggested Reference Material

- *Am186™CC/CH/CU Microcontroller User's Manual*
  Advanced Micro Devices, order #21914
- *Am186™CC Communications Controller Data Sheet*
  Advanced Micro Devices, order #21915
- *Am186™CH HDLC Microcontroller Data Sheet*
  Advanced Micro Devices, order #22024
- *Am186™CU USB Microcontroller Data Sheet*
  Advanced Micro Devices, order #22025
- *Am186™CC/CH/CU Microcontroller Register Set Manual*
  Advanced Micro Devices, order #21916
- *Am186™ and Am188™ Family Instruction Set Manual*
  Advanced Micro Devices, order #21076
- *E86MON™ Software User's Manual*
  Advanced Micro Devices, order #21891
- *E86™ Family Products and Development Tools CD*
  Advanced Micro Devices, order #21508

Documentation Conventions

Table 0-1. Notational Conventions

Symbol	Usage
Boldface	Indicates that characters must be entered exactly as shown, except that the alphabetic case is only significant when indicated.
`Typewriter face`	Indicates computer text input or output in an example or listing.

Chapter 1

Quick Start

This chapter provides information that will help you quickly set up and start using the Am186™CC/CH/CU Microcontroller CDP.

The CDP is supported by the E86MON™ board-resident debugger. The E86MON boot monitor software enables you to load, run, and debug programs on the CDP. For detailed information on using the E86MON software, refer to the *E86MON™ Software User's Manual* included in your kit.

For information on how to:

Connecting to a PC via a Serial Port

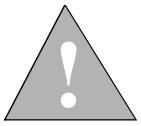
Follow the steps below to connect the Am186CC/CH/CU microcontroller customer development platform to your PC via your PC's serial port.

Installation Requirements

The items listed below are necessary to install and run the CDP:

- PC with an available COM port
- Terminal emulation software (such as Microsoft® Windows®Terminal or ProComm Plus) that supports ASCII file transfers, software flow control (Xon/Xoff), and send break capability.
- Power source for universal power supply

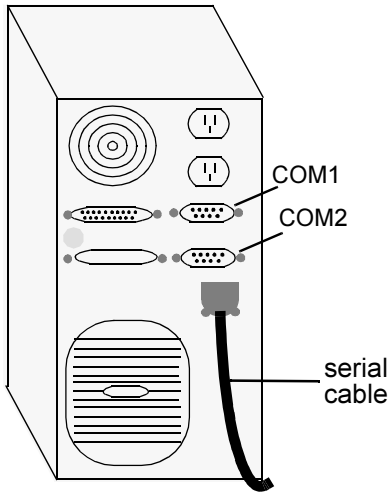
Main Board Installation



CAUTION: As with all computer equipment, the Am186CC/CH/CU microcontroller CDP's main board may be damaged by electrostatic discharge (ESD). Please take proper precautions when handling any board.

1. Remove the board from the shipping carton. Visually inspect the board to verify that it was not damaged during shipment.

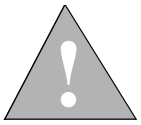
2. Connect either of the CDP main board's DB-9 serial ports to an available COM port. Use the serial cable included in the Am186CC/CH/CU microcontroller CDP kit and note that a DB-9 to DB-25 serial connector adapter is provided if your host system requires it.



3. Connect the power supply to the barrel connector (see P31 at location A-1 in Figure 2-2 on page 2-3) on the CDP's main board.

4. Apply power to the board by connecting the power supply to an electrical outlet. When the board is powered up, the LEDs (see CR12–CR8 at locations C-2–F-2 in Figure 2-2 on page 2-3) should be illuminated.

   If all of the LEDs are not illuminated, remove the power supply immediately and contact AMD technical support. See "If You Have Questions, We're Here to Help You." on page iii.



CAUTION: If using your own power supply, ensure that it is a 12-V supply and is capable of providing at least 2 A.

5. Invoke the terminal emulation program at 19200 baud, no parity, 8 data bits, and 1 stop bit; enable the software flow control (Xon/Xoff), if supported.
6. Reset the board by depressing and releasing the RESET switch (see SW1 at location T-23 in Figure 2-2 on page 2-3).

   Type an **a** in the terminal window within three seconds of reset to ensure that the E86MON software uses the correct baud rate. When the E86MON software receives an **a**, it adjusts its baud rate (if necessary) and displays the welcome message and prompt.

NOTE: If you type a character other than an **a**, or type no character at all, the E86MON software still displays the welcome message and prompt, but may be using an incorrect baud rate. Depressing and releasing the RESET switch (SW1 at location T-23) gives you another opportunity to type an **a**.

7. To display the version of the monitor and the commands available, type **?** and press Enter.

   For detailed information about using the E86MON software, refer to the *E86MON™ Software User's Manual* included in your kit.

Connecting to a PC via a USB port

NOTE: USB is *not supported* on the Am186CH HDLC microcontroller.

Follow the steps below to connect the Am186CC/CH/CU microcontroller customer development platform to your PC via your PC's USB port.

1. Insert the flat end of your USB cable into the USB port that is connected to your PC.
2. Connect the other end of the USB cable into the CDP's main board USB connector (see P18 at location I-1 in Figure 2-2 on page 2-3) that is located on the edge of the board near the power supply (see P31 at location A-1).

To drive the USB, download the USB driver CodeKit software from the AMD website. The CodeKit software package includes installation instructions for the USB host driver and the USB driver on the CDP.

Go to **www.amd.com**, then click on Embedded Processors to get to the Codekit software packages.

Connecting the Development Module to the Main Board

Follow the steps below to connect the router/ISDN development module to the Am186CC/CH/CU microcontroller CDP main board (see Figure 3-3 on page 3-5).

1. Orient the main board such that the AMD logo is in the lower right-hand corner, facing you. Orient the development module such that the AMD logo is in the lower leviathan corner, facing you.
2. Position the development module above the development module connectors (see P12 and P19 at locations M-22 and F-22, respectively, in Figure 2-2 on page 2-3) on the main board.
3. Carefully press the development module down onto the connectors on the main board.

Connecting a TIP to the Main Board

Follow the steps below to connect the test interface port (TIP) debug board to the Am186CC/CH/CU microcontroller CDP main board:

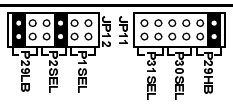
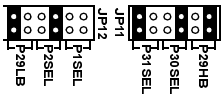
1. Orient the main board such that the AMD logo is in the lower righthand corner, facing you.
2. Place the TIP board to the left of the main board with the LCD display toward you.
3. Plug the TIP connector into the TIP board with the tab facing toward the left.
4. Plug the other end of the connector into the CDP's main board TIP (see P30 at location A-19 in Figure 2-2 on page 2-3) with the tab facing up.

Connecting a ROM-ICE to the Main Board

Follow the steps below to connect a ROM-ICE to the Am186CC/CH/CU microcontroller customer development platform main board:

1. Orient the main board such that the AMD logo is in the lower righthand corner, facing you.
2. Set the jumpers according to the configuration shown in Table 1-1 on page 1-7, and jumper your chip select on JP10 (see location F-9 in Figure 2-2 on page 2-3).
3. Position the ROM-ICE to the left of the main board.
4. Connect the ROM-ICE Low into the left DIP socket (see U28 at location B-12), which is labeled SRAM/ROM LOW.
5. Connect the ROM-ICE High into the right DIP socket (see U25 at location D-12), which is labeled SRAM/ROM HIGH.

Table 1-1. ROM-ICE Configuration

Device	JP12			JP11			Visual Detail
	P29LB	P2SEL	P1SEL	P31SEL	P30SEL	P29HB	
ROM 128K x 16	11-12	5-6	NC	NC	NC	1-2	
ROM 512K x 16	11-12	5-6	NC	11-12	5-6	1-2	

Troubleshooting Installation Problems

Table 1-2. Installation Troubleshooting

Problem	Solution
Nothing happens when pushing the RESET button.	Sometimes it is difficult to make a good connection when pushing the small RESET button. If all else fails, remove the power supply from the AC electrical outlet and disconnect and reconnect the power supply. The LEDs will light up when the reset is successful.
The computer does not respond with the E86MON software prompt.	Reset the board by pressing the RESET switch and typing an **a** immediately after power up. If this does not work, verify the power, check the cables, etc., and verify that the terminal program is configured correctly.
After typing **a** during reset, the terminal emulation software displays unreadable characters.	Check the baud rate setting for the terminal emulation software. It should be set to 19200. Also check the word length (8), stop bits (1), and parity (N), and turn off any hardware flow control.
The terminal emulation program locks up the software or PC.	Check the COM port connection with the target board. Make sure that the same COM port is selected in the terminal emulation software. In some PCs if the correct COM port is not specified, the software will fail to function—it will lock in a continuous loop waiting for an answer from the incorrect serial port.
The power LED does not turn on with power.	Immediately disconnect the power supply. Ensure that the polarity of the power connector is correct. This is a very serious failure of the hardware. If the power source is connected incorrectly, the board will be permanently damaged.
There is a problem you cannot resolve.	Contact the AMD Corporate Applications technical support services (see page iii for phone numbers and more information).

For More Information...

If you need more information about:

- Am186CC/CH/CU microcontroller CDP hardware,
  see Chapter 2 and Chapter 3.
- E86MON software,
  see the *E86MON™ Software User's Manual* included in your kit.
- Problems with the platform or the E86MON software,
  see the customer support information on page iii.
- The Am186CC/CH/CU microcontroller CDP's main board layout,
  see Chapter 2.
- The Am186CC/CH/CU microcontroller CDP's module layout,
  see Chapter 3.
- The Am186CC/CH/CU microcontroller CDP's main board schematics,
  see the schematics document included in your kit.
- The Am186CC/CH/CU microcontroller CDP's module schematics,
  see the schematics document included in your kit.
- The Am186CC/CH/CU microcontrollers,
  see the following documents, which are included in your kit:
  - *Am186™CC Communications Controller Data Sheet*
  - *Am186™CH HDLC Microcontroller Data Sheet*
  - *Am186™CU USB Microcontroller Data Sheet*
  - *Am186™CC/CH/CU Microcontrollers User's Manual*
  - *Am186™CC/CH/CU Microcontrollers Register Set Manual*

Chapter 2

Main Board Functional Description

The Am186CC/CH/CU microcontroller customer development platform (CDP) consists of two boards: a main board that contains an Am186CC communications controller and interfaces, and the development module, which you can use to develop ISDN and router applications. This chapter describes the main board. The development module is described in Chapter 3, “Development Module Functional Description”.

Read the following sections to learn more about the main board:

Main Board Layout

The Am186CC/CH/CU microcontroller customer development platform is easy to configure to fit your design requirements. Figure 2-1 shows the main board block diagram; Figure 2-2 shows the main board layout and component placement; and Table 2-1 lists the jumpers and switches. Note that the schematics referenced are in the separate schematic manual in your board kit.

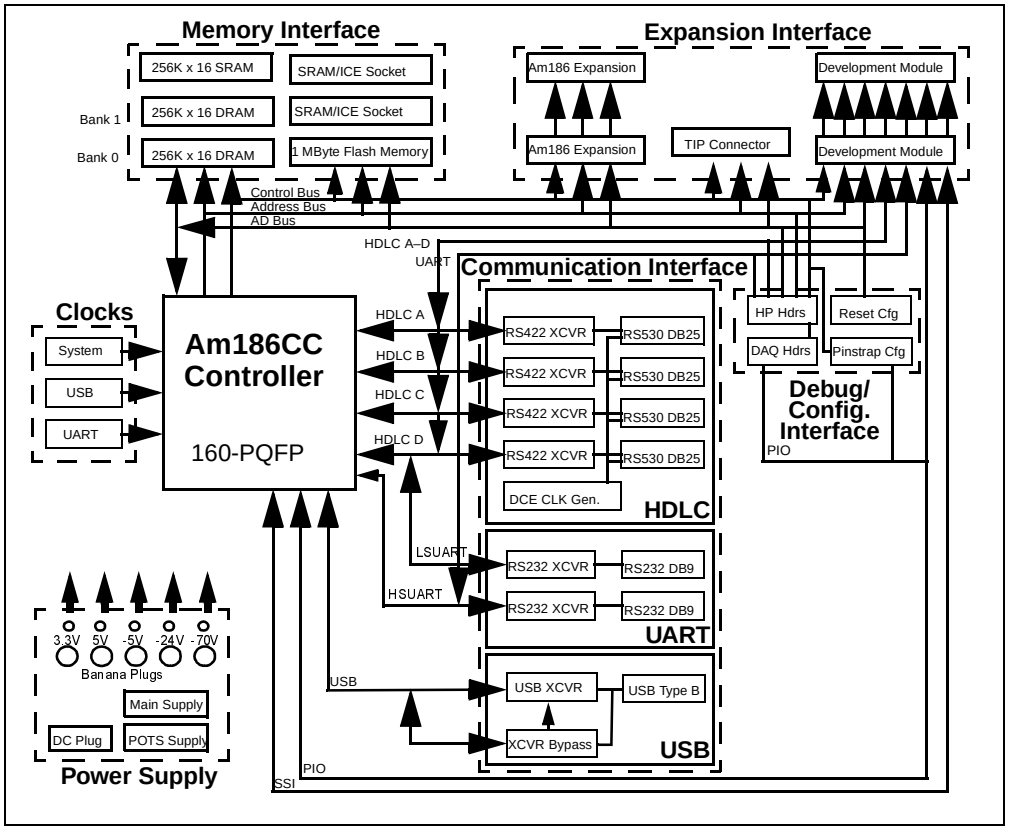


Figure 2-1. Main Board Block Diagram (Same as Figure 0-1)

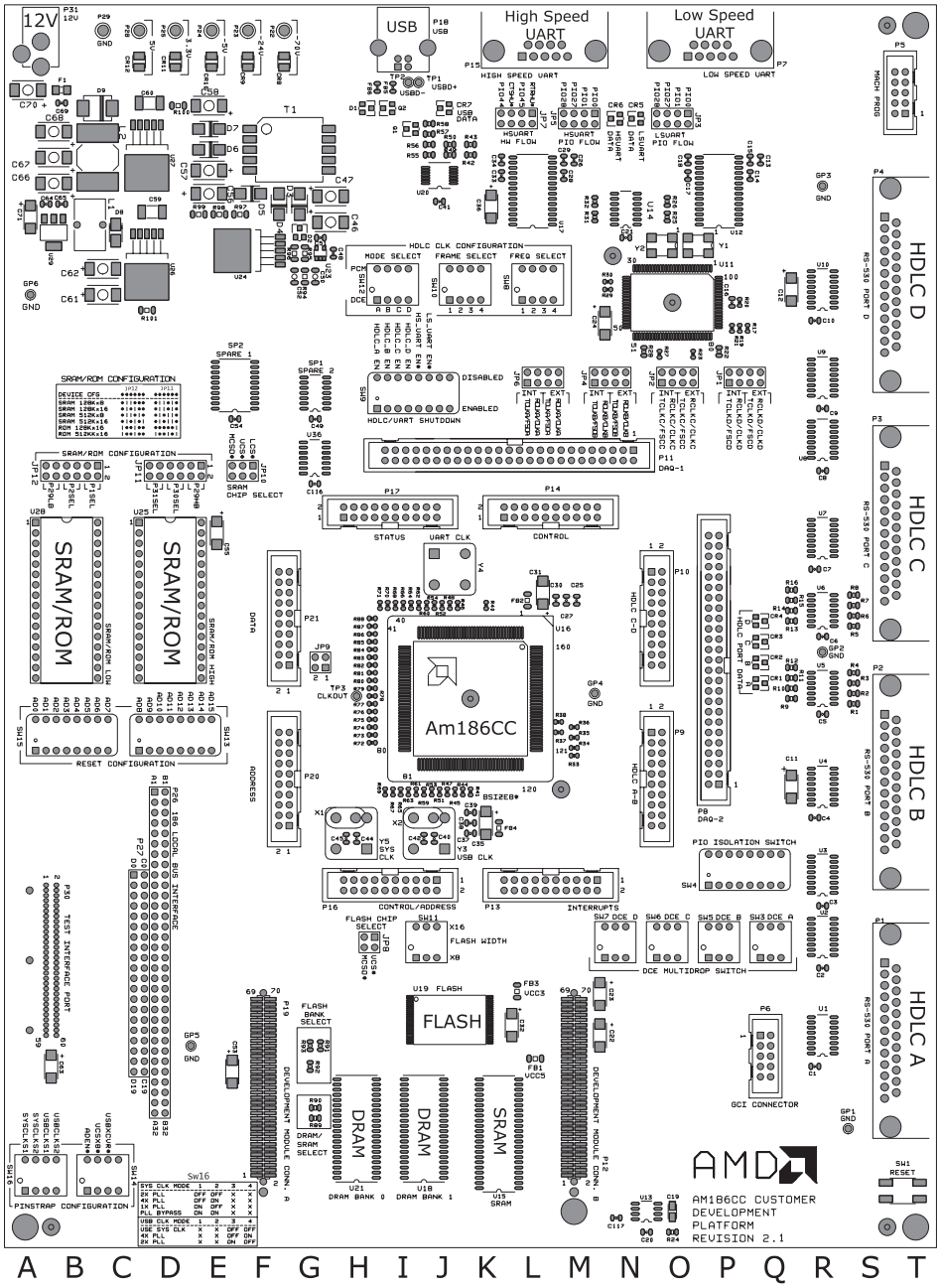


Figure 2-2. Main Board Layout

Table 2-1. Jumpers, Switches, and Adjustments

Part	Function	Description	Reference in Figure 2-2	Schematic Reference Sheet #
JP1	HDLC Channel D[1] and clock select	Used to route DCE clocks for HDLC Channel D.	P7	Main board Sheet 8
JP2	HDLC Channel C[1] and clock select	Used to route DCE clocks for HDLC Channel C.	O7	Main board Sheet 8
JP3	UART flow control output select	Used to provide PIO output for additional RS-232 flow control.	O3	Main board Sheet 9
JP4	HDLC Channel B[2] and clock select	Used to route DCE clocks for HDLC Channel B.	N7	Main board Sheet 8
JP5	UART flow control input select	Used to provide PIO input for additional RS-232 flow control.	M3	Main board Sheet 9
JP6	HDLC Channel A[2] and clock select	Used to route DCE clocks for HDLC Channel A.	L7	Main board Sheet 8
JP7	High-Speed UART flow control	Provides isolation to High-Speed UART flow control signals or alternate PIOs for flow control.	L3	Main board Sheet 9
JP8	Chip select for Flash memory	Used to select $\overline{\text{UCS}}$ or $\overline{\text{MCS0}}$ for Flash memory.	H18	Main board Sheet 4
JP9	Logic analyzer clock select	Used as a clock input on the logic analyzer header.	G13	Main board Sheet 11
JP10	SRAM/ROM-ICE device select	Used to select $\overline{\text{LCS}}$, $\overline{\text{UCSR}}$, or $\overline{\text{MCS0}}$ for SRAM/ROM-ICE.	F9	Main board Sheet 5
JP11	SRAM/ROM-ICE device select	Used to select various SRAM and ROM configurations.	D9	Main board Sheet 5

Table 2-1. Jumpers, Switches, and Adjustments (Continued)

Part	Function	Description	Reference in Figure 2-2	Schematic Reference Sheet #
JP12	SRAM/ROM-ICE device select	Used to select various SRAM and ROM configurations.	B9	Main board Sheet 5
SW1	Reset switch	Used to reset the CDP.	T22	Main board Sheet 3
SW3	HDLC DCE port A multidrop select	Used to enable multidrop mode for port A.[2]	Q18	Main board Sheet 15
SW4	PIO isolation select	Used to isolate PIOs from other usage on CDP.	P16	Main board Sheet 15
SW5	HDLC DCE port B multidrop select	Used to enable multidrop mode for port B.[2]	P18	Main board Sheet 15
SW6	HDLC DCE port C multidrop select	Used to enable multidrop mode for port C.[1]	O18	Main board Sheet 15
SW7	HDLC DCE port D multidrop select	Used to enable multidrop mode for port D.[1]	N18	Main board Sheet 15
SW8	HDLC clock configuration select	Selects HDLC ports A–D frequency options.[1,2]	L6	Main board Sheet 8
SW9	Serial interface transceiver select	Used to disable HDLC port A–D and UART transceivers. (Default: HDLC A–D off and UARTS on.)[1,2]	I8	Main board Sheet 3
SW10	HDLC clock configuration select	Selects HDLC ports A–D for PCM frame synchronization options.[1,2]	J6	Main board Sheet 8

Table 2-1. Jumpers, Switches, and Adjustments (Continued)

Part	Function	Description	Reference in Figure 2-2	Schematic Reference Sheet #
SW11	Flash memory data bus width select	Used to determine Flash memory width as 16 or 8 bits. Default: 16 bits.	J18	Main board Sheet 4
SW12	HDLC clock configuration select	Selects HDLC ports A–D for DCE or PCM clocks.[1,2]	I6	Main board Sheet 8
SW13	Reset configuration select	Platform user-specific system configuration.	D14	Main board Sheet 3
SW14	USB clock pinstrap select[3]	Used to select AD address enable, $\overline{\text{UCS}}$ data width, and external USB[3] transceiver.	C22	Main board Sheet 3
SW15	Reset configuration select	Platform user-specific system configuration.	B14	Main board Sheet 3
SW16	CPU and USB[3] clock pinstrap select	Used to select system and USB clock PLL mode pinstrap options.	A22	Main board Sheet 3
GP1	Ground	Ground post.	R21	Main board Sheet 15
GP2	Ground	Ground post.	R12	Main board Sheet 15
GP3	Ground	Ground post.	R4	Main board Sheet 15
GP4	Ground	Ground post.	M13	Main board Sheet 15
GP5	Ground	Ground post.	D20	Main board Sheet 15
GP6	Ground	Ground post.	A6	Main board Sheet 15

Table 2-1. Jumpers, Switches, and Adjustments (Continued)

Part	Function	Description	Reference in Figure 2-2	Schematic Reference Sheet #
TP1	Test point	Test point for USBD+ from USB connector (P18).[3]	I2	Main board Sheet 10
TP2	Test point	Test point for USBD– from USB connector (P18).[3]	I2	Main board Sheet 10
TP3	Test point	Test point for CLKOUT.	H13	Main board Sheet 2

1. HDLC channels C and D supported on the Am186CC communications controller only.
2. HDLC channels A and B supported on the Am186CC and Am186CH microcontrollers only.
3. USB is supported on the Am186CC and Am186CU microcontrollers only.

Main Board Features

The main board is a single-sided, 9- x 12-inch, printed circuit board that integrates the Am186CC communications controller, a power supply, memory interfaces, and I/O interfaces onto one board, enabling you to develop specific applications using the development module interface.

The main board contains debug and status features, and enables you to evaluate and develop different configurations of memory and I/O by using on-board configuration switches, jumper blocks, and expansion interfaces.

The following features are described in this section:

Am186™CC/CH/CU Microcontroller (J14)

The Am186CC/CH/CU microcontroller customer development platform supports a 160-pin PQFP Am186CC communications controller operating at 25, 40, or 50 MHz. The integrated features of the Am186CC communications controller provide a glueless interface to DRAM or SRAM system memory and Flash memory. The microcontroller also integrates UART and High-Speed UART (which require only external transceivers), a high-speed (12 Mbit/s) USB peripheral controller with internal transceiver (Am186CC and Am186CU microcontrollers only), and HDLC channels (Am186CC and Am186CH microcontrollers only) that provide external interfaces to gluelessly connect to communications peripherals.

NOTE: Although the CDP supports an Am186CC communications controller, you can also use this platform to evaluate the Am186CH and Am186CU microcontrollers. These microcontrollers support subsets of the Am186CC communications controller's features. Refer to the device data sheets for more information.

The Am186CC communications controller is designed as a cost-effective, high-performance microcontroller solution for communication applications. The Am186CC communications controller offers the advantages of the x86 development environment's widely available native development tools, applications, and system software. For detailed information about the specific features of the Am186CC/CH/CU microcontroller, refer to the corresponding data sheet and user's manual included in your kit. Figure 2-3 shows the Am186CC communications controller block diagram; Figure 2-4 on page 2-10 shows the Am186CH HDLC microcontroller block diagram; and Figure 2-5 on page 2-10 shows the Am186CU USB microcontroller block diagram.

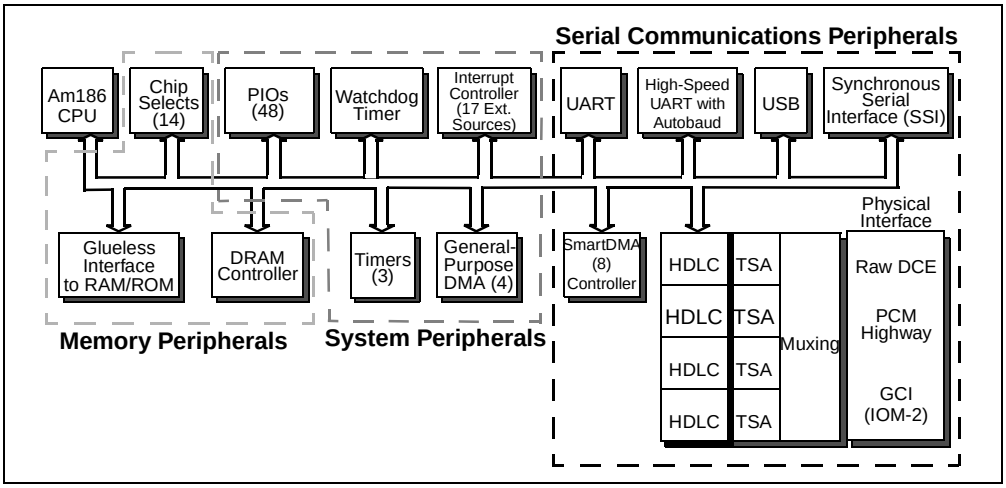


Figure 2-3. Am186CC™ Communications Controller Block Diagram

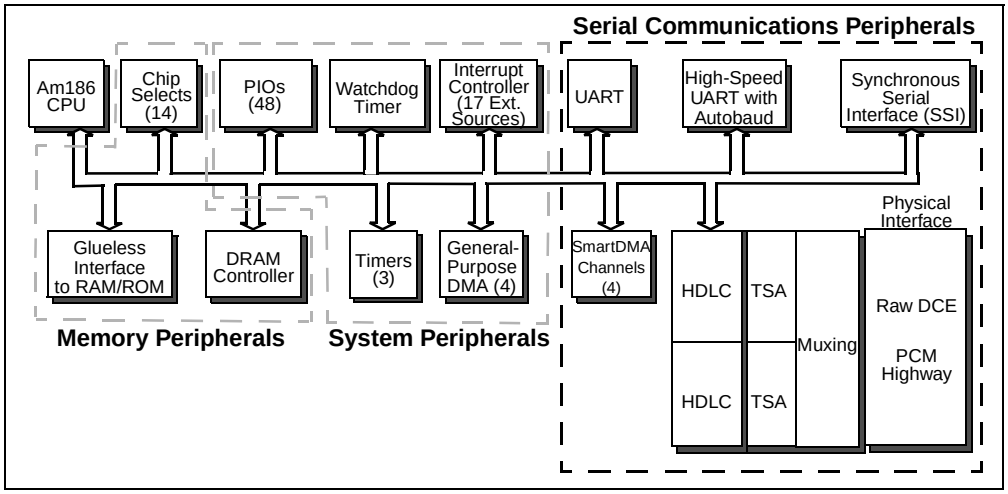


Figure 2-4. Am186CH™ HDLC Microcontroller Block Diagram

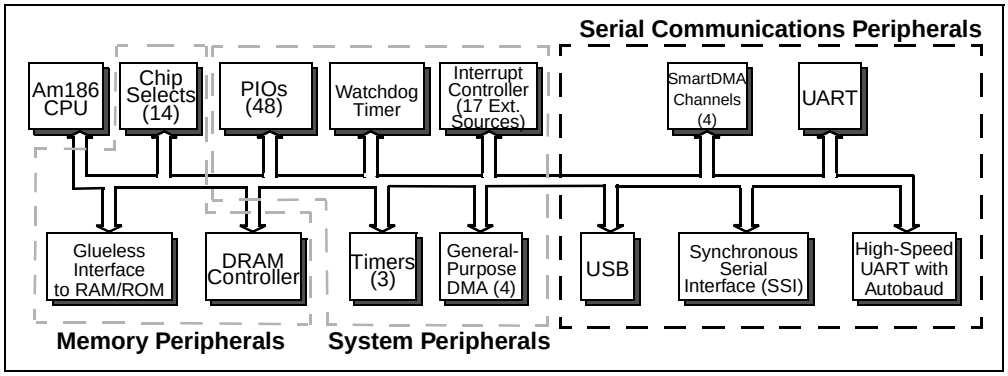


Figure 2-5. Am186CU™ USB Microcontroller Block Diagram

Am186CC™ Communications Controller Power Supply

The CDP main board provides a 3.3-V power supply for the Am186CC communications controller. The power supply is sourced from a 3.3-V low drop out (LDO) regulator (U29) from a 5-V switching power supply. The digital and analog power pins are isolated by filtering to prevent noise on the digital circuitry from affecting the internal analog block.

Am186™CC/CH/CU Microcontroller Clocking

Four types of input clocks are used on the main board: the system clock, USB clock (Am186CC and Am186CU microcontrollers only), UART clock, and HDLC clocks (Am186CC and Am186CH microcontrollers only).

The system and USB clocks, shown in Figure 2-6 and Figure 2-7, respectively, use internal oscillators and PLLs that enable the use of slower, less costly, fundamental mode crystals for providing system clock frequencies from 16 to 50 MHz, and a USB frequency of 48 MHz. The UART clock can be derived from the system clock frequency, or from the UCLK input by using an external oscillator. The on-board MACH device can be used for the DCE or PCM HDLC clocks at various frequencies and frame syncs (PCM mode only); or if you are using the development module interface, you can drive the HDLC clocks from a specific DCE, PCM, or GCI peripheral. For the available clock options, see Table 2-2.

Table 2-2. CPU and USB Clock Options

Clock	PLL Mode			PLL Bypass	Oscillator
	1x	2x	4x		
System clock	16–40 MHz	8–25 MHz	8–12.5 MHz	0–24 MHz	0–40 MHz
USB clock[1]	—	24 Mhz	12 MHz	—	12, 24 MHz
Shared system/USB clock	—	24 Mhz	12 MHz	—	12, 24 MHz
UART clock	—	—	—	—	0–40 MHz[2]

1. The USB clock is supported on the Am186CC and Am186CU microcontrollers only.
2. UCLK is limited to the maximum frequency of the system clock.

System Clock

The system clock, shown in Figure 2-6 on page 2-12 (or sheet 3 of the main board schematics included in your kit), can be derived from a fundamental mode crystal by doing one of the following:

- Driving X1 and X2 at location X1 into the integrated oscillator and using the internal PLL (see locations H16 and J16 in Figure 2-2 on page 2-3)
- Driving X1 and X2 at location X1 into the integrated oscillator and bypassing the internal PLL

The system clock can also be derived from an external oscillator by doing one of the following:

- Driving an external oscillator from Y5 into X1 and using the internal PLL (see location H16 in Figure 2-2 on page 2-3)
- Driving an external oscillator from Y5 into X1 and bypassing the internal PLL

The PLL can be configured in 1x, 2x (default), or 4x PLL mode or PLL bypass mode by appropriately setting the pinstraps on SW16. See “Debug and Configuration Circuitry” on page 2-39 for more information.

The maximum crystal input and oscillator frequencies are 40 MHz. The CDP provides pin sockets, allowing the designer to easily attain multiple clock configurations.

NOTE: When using an external oscillator or clock source to drive the system, USB, or UART clock, you must drive the clock with a source that does not exceed the Am186CC/CH/CU microcontroller’s V_{CC}.

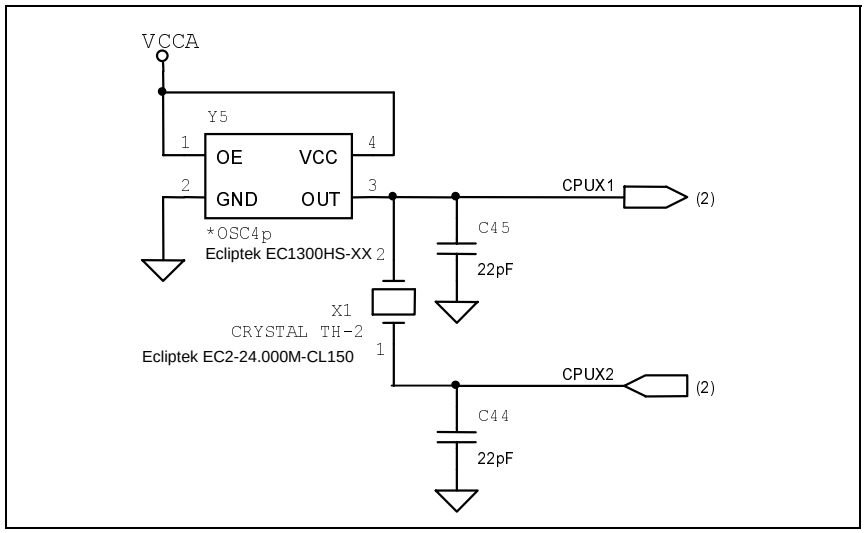


Figure 2-6. Am186™CC/CH/CU Microcontroller System Clock

USB Clock

- The USB clock (shown in Figure 2-7or sheet 3 of the main board schematics included in your kit), which must be 48 MHz, may be derived from one of the following:
- System clock
- Driving USBX1 and USBX2 at location X2 into the integrated oscillator and using the internal PLL (see location J16 in Figure 2-2 on page 2-3)
- Driving an external oscillator into USBX1 from Y3 and using the internal PLL

The PLL can be configured in 2x or 4x PLL mode by appropriately setting the pinstraps on SW16. See “Debug and Configuration Circuitry” on page 2-39 for more information.

The Am186CC and Am186CU microcontrollers’ USB block requires a 48-MHz clock input. The USB clocking options are 12 MHz in 4x PLL mode, 24 MHz in 2x PLL mode, or a system clock of 48 MHz.

NOTE: When using the system clock for USB clocking, USBX1 must be terminated to ground to prevent unwanted oscillation in the unused integrated USB oscillator. To accomplish this, populate C42 with a 0-Ω resistor.

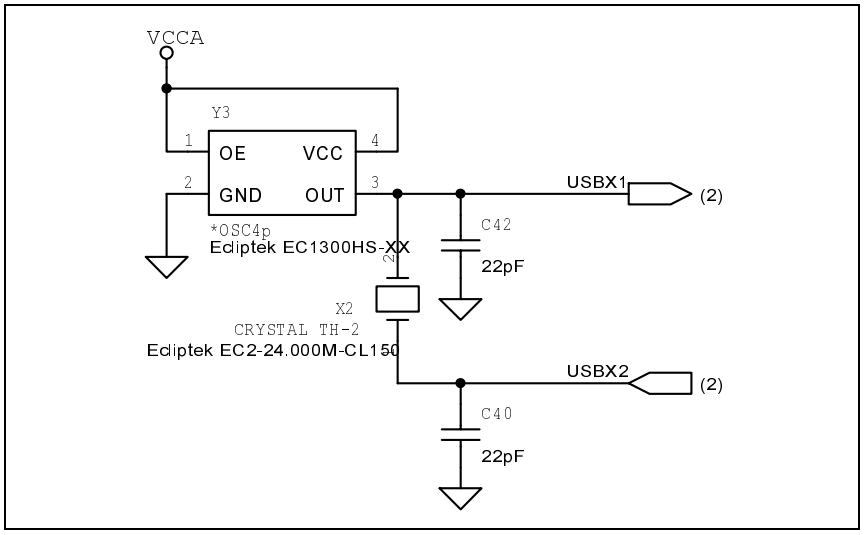


Figure 2-7. Am186CC or Am186CU Microcontroller USB Clock

The UCLK input at location Y4 (see location J11 in Figure 2-2 on page 2-3) is used to drive the UART or High-Speed UART with a unique clock source that is not derived from the system clock. The CDP provides oscillator pin sockets, enabling the use of standard 3.3-V half-can oscillators.

Am186CC™ Communications Controller Reset

The Am186CC communications controller requires the $\overline{RES}$ input to be asserted for at least 1 ms to allow the internal circuitry to stabilize. The CDP main board uses an external device that monitors the 3.3-V V_{CC} to provide a reset output with an internal 21-ms RC delay to drive the 3.3-V $\overline{RES}$ input to the Am186CC communications controller. Depressing the reset switch (SW1) causes a system reset without cycling power. Figure 2-8 (or sheet 3 of the main board schematics included in your kit) shows the reset circuitry.

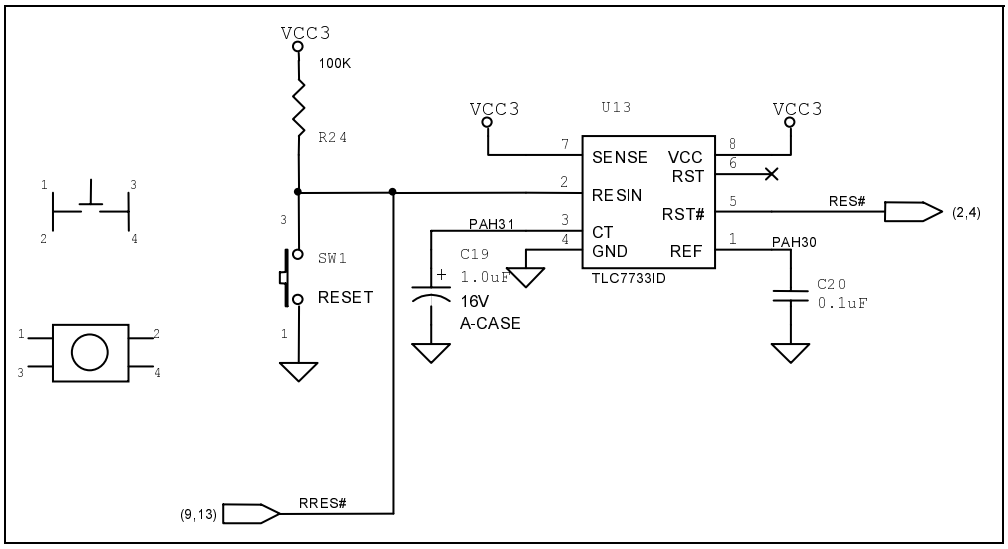


Figure 2-8. Main Board Reset Circuitry

Power Supply (A1)

The CDP is powered by a universal power supply that converts 100–200 V_{AC} power to 12 V_{DC}, 2.5 A. The 12 V enters the CDP main board through a 5.5-mm barrel connector, where the center post is V_{CC} and the outer ring is GND. From the 12-V_{DC} input, the CDP on-board power supply provides 5 V, 3.3 V, –5 V, –24 V, and –70 V. The CDP provides power indicators for these voltages at CR8–CR12. The CDP also provides test jacks that enable you to monitor the V_{CC} voltages at P22–P25, P28–P29. The following sections provide details about the power supply. Table 2-3 through Table 2-5, beginning on page 2-18, contain power estimates for the CDP main board, development module, and CDP totals.

5 V @ 3 A

A 5-V buck switching circuit from the 12-V source generates the 5 V, which provides power to a majority of the components on the CDP main board including the DRAM, SRAM, and Flash memory components; the DCE and UART transceivers; the HDLC clock generator; and the 3.3-V LDO regulator. This power supply is also routed to the CDP development module, TIP connector, and Am186 processor expansion interface connectors. For details, see Figure 2-9 or sheet 14 of the main board schematics included in your kit.

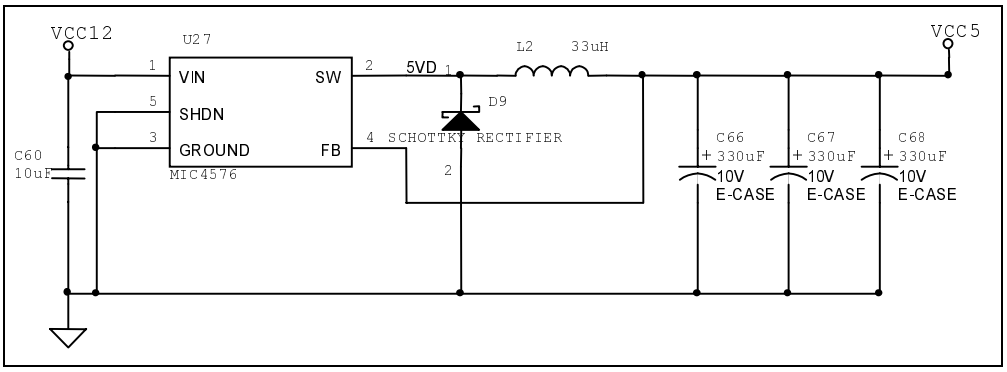


Figure 2-9. 5-V Power Supply

3.3 V @ 500 mA

The 3.3-V LDO regulator at location U29 generates the 3.3 V from the 5-V output. This power supply is used to provide power to the Am186CC communications controller, the USB detect circuitry, and to the optional external USB transceiver. A population option to use the 3.3-V source for the memory components is available. This option is available for the case where no 5-V devices are located on the Am186CC communications controller local bus. For details, see Figure 2-10 or sheet 14 of the main board schematics included in your kit.

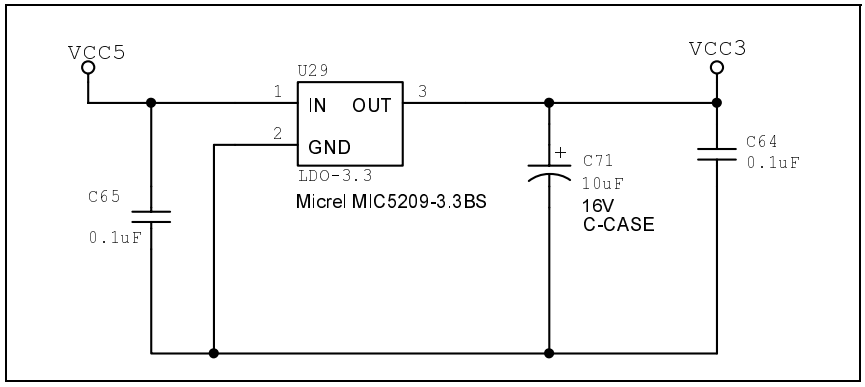


Figure 2-10. 3.3-V Power Supply

–5 V @ 200 mA

A 5-V buck-boost switching circuit from the 12-V source generates the –5 V. This power supply provides power to the CDP development module and POTS interface. For details, see Figure 2-11 or sheet 14 of the main board schematics included in your kit.

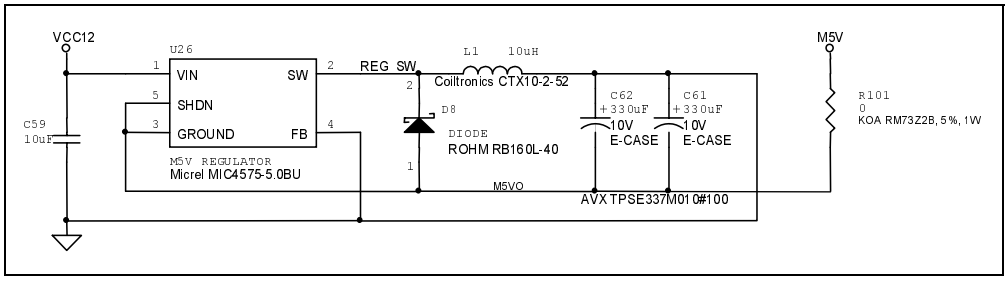


Figure 2-11. –5-V Power Supply

–24 V @ 50 mA and –70 V @ 60 mA

A switching flyback circuit from the 12-V source generates the –24 V and the –70 V. These outputs are routed to the CDP development module and are used in the POTS interface. For details, see Figure 2-12 or sheet 14 of the main board schematics included in your kit.

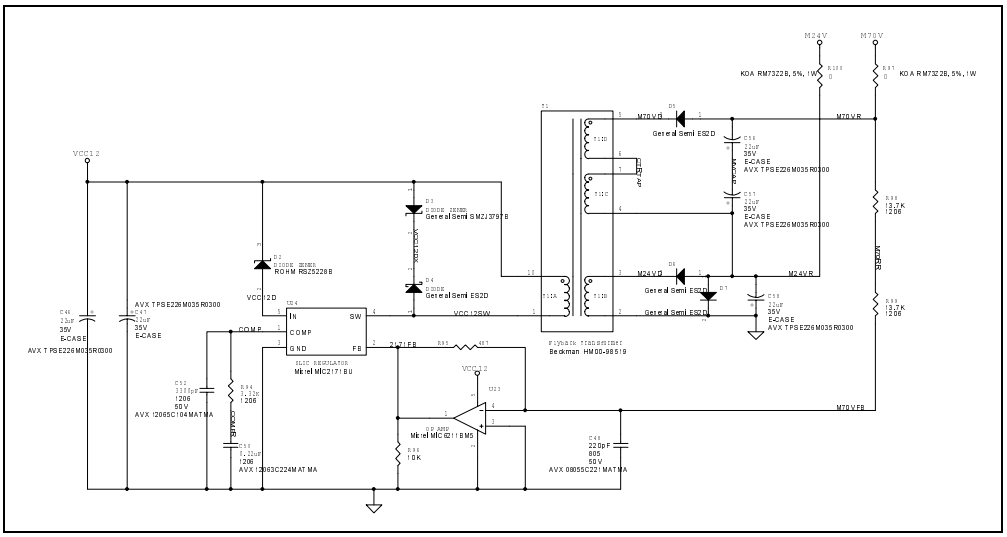


Figure 2-12. –24-V and –70-V Power Supplies

Table 2-3. Power Estimates for the CDP Main Board

Voltage (V)	Device	Qty	I_{typ}(mA)	I_{max}(mA)	P_{typ}(mW)	P_{max}(mW)
3.3	Am186CC communications controller	1	300[1]	380	1000	1250
3.3	USB transceiver[2]	1	10	30	33	99
5	DRAM 256K x 16	2	180	180	1800	1800
5	SRAM 128K x 8	2	20	35	200	350
5	Flash memory 1M x 8/512K x 16	1	36	60	180	300
5	CLK generator (PLD)	1	120	200	600	1000
5	UART transceiver	2	20	20	200	200
5	DCE driver	2	8	20	80	200
5	DCE receiver	4	16	23	320	460
3.3 5	Main board total		310 380	410 572	1023 1900	1353 2860

1. Average operating current at 50 MHz.
2. USB is supported on the Am186CC and Am186CU microcontrollers only.

Table 2-4. Power Estimates for the CDP Development Module

Voltage (V)	Device	Qty	I_{typ}(mA)	I_{max}(mA)	P_{typ}(mW)	P_{max}(mW)
5	Ethernet controller	1	75	75	375	375
5	ISDN S/T transceiver	1	31	38	155	190
5	ISDN U transceiver[1]	1	54	70	270	350
5	DTMF	2	3	7	30	70
5 –5	DSLAC	1	24 10	24 10	120 50	120 50
5 –5 –24 –70	RSLIC	2	6.5 0.70 2.70	9 1.10 5	65 7 129.60	90 11 240
5 –5 –24 –70	CDP development module total		203 10.7 2.70 2.70	239 11.1 5 5	101.5 53.5 64.8 189	1195 55.5 120 350

1. USB is supported on the Am186CC and Am186CU microcontrollers only.

Table 2-5. Total Power Estimates for the CDP

Voltage (V)	I_{typ}(ma)	I_{max}(ma)	P_{typ}(mw)	P_{max}(mw)
3.3	310	410	1023	1353
5	583	811	2915	4055
–5	10.7	11.1	53.5	55.5
–24	2.70	5	64.8	120
–70	2.70	5	189	350

Memory Interfaces

The Am186CC/CH/CU microcontroller customer development platform main board supports DRAM or SRAM system main memory and Flash memory. Figure 2-13 shows the DRAM or SRAM system and Flash memory map, Figure 2-14 on page 2-21 shows the DRAM and SRAM circuitry, and Figure 2-15 on page 2-22 shows the Flash memory circuitry.

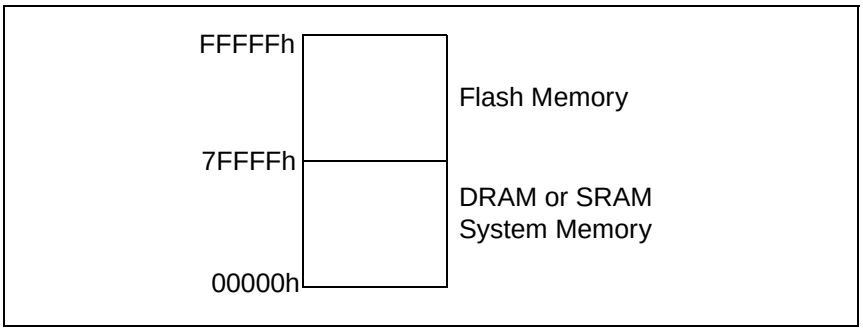


Figure 2-13. DRAM or SRAM System Memory and Flash Memory Map

Main Memory

The main board allows the use of two banks of DRAM, or SRAM as the main memory for the system. The default configuration is one bank of 256K x 16 EDO DRAM in an SOJ package, located at U21. See Figure 2-14 on page 2-21 or sheet 4 of the main board schematics included in your kit.

In the default configuration, one bank of 256K x 16 EDO, 40-ns DRAM allows zero wait state operation at up to 50 MHz. The DRAM resides in the lower 512 Kbyte of $\overline{\text{LCS}}$ memory space (0h–7FFFFh). The Am186CC communications controller provides the DRAM memory address on the odd Am186CC communications controller addresses A1–A17 to provide a direct connection to the DRAM device. The DRAM $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ signaling is provided on the $\overline{\text{LCS0}}$/$\overline{\text{RAS0}}$, $\overline{\text{MCS1}}$/$\overline{\text{CAS1}}$, and $\overline{\text{MCS2}}$/$\overline{\text{CAS0}}$ signals from the Am186CC communications controller when DRAM is selected as the main system memory.

An unpopulated component location, U18, is available for a 256K x 16 device for DRAM bank 1 to be used in the upper 512K of memory space ($\overline{\text{UCS}}$ space). This enables you to boot from Flash memory located in $\overline{\text{UCS}}$ space, and then remap $\overline{\text{UCS}}$ to DRAM bank 1. In this case, the $\overline{\text{MCS3}}/\overline{\text{RAS1}}$ signal becomes the $\overline{\text{RAS}}$ for bank 1 and the $\overline{\text{CAS}}$ signals remain the same.

To use SRAM as main system memory, a 256K x 16 SOJ SRAM can be populated at location U15. R89 must be depopulated, and R90 must be populated with a 10-kΩ resistor.

Another option for using SRAM as main system memory is to use two 32-pin DIP sockets at U25 and U28 for SRAM devices. The SRAM is configurable to be used as 128K x 8/512K x 8, or 128K x 16/512K x 16 via configuration jumper blocks JP11 and JP12. A jumper block, JP10, is also used to route either $\overline{\text{LCS}}$, $\overline{\text{UCS}}$, or $\overline{\text{MCS0}}$ to the SRAM sockets.

The CDP main board is populated with 128K x 8, 35-ns DIP SRAM devices as the optional system memory.

NOTE: The SRAM sockets are also used for the x16 ROM-ICE interface. Because of this, $\overline{\text{LCS}}$, $\overline{\text{UCS}}$, or $\overline{\text{MCS0}}$ can be used, allowing flexibility of chip selects between the ROM-ICE and on-board Flash memory (see Table 2-6 on page 2-24).

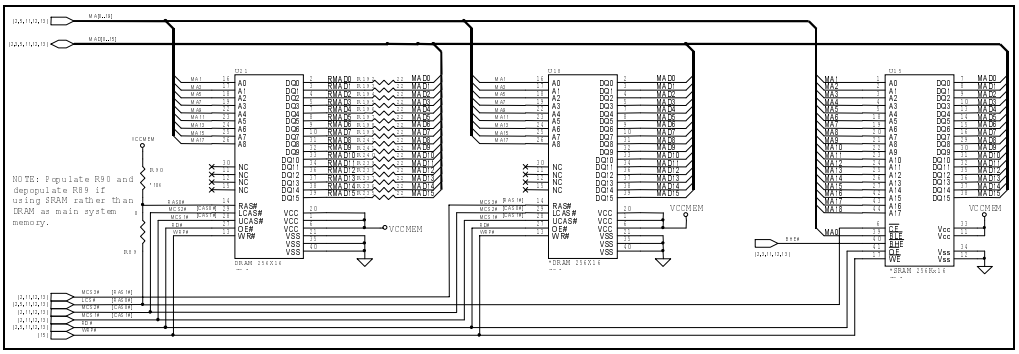


Figure 2-14. Main Memory DRAM Circuit

Flash Memory

A single, surface-mount, TSOP Am29F800, 55-ns, 8-Mbit Flash memory device is populated on the CDP main board to allow for zero wait state operation at 50 MHz. See Figure 2-15 or sheet 4 of the main board schematics included in your kit.

You can configure the Flash memory device as 512K x 16 or as a 1-Mbyte x 8 device via configuration switches SW11 and SW14. The default configuration defines the Flash memory as 512 Kbyte (256K x 16) in $\overline{\text{UCS}}$ space (80000h–FFFFFh). The highest order address bit of the Flash memory can be connected to PIO35 rather than A19 by populating R93 with a 0-Ω resistor and removing R92. This enables you to bank down to the lower half of the Flash memory to extend available code space to 1 Mbyte. You can also map the Flash memory to $\overline{\text{MCS0}}$ rather than $\overline{\text{UCS}}$ via jumper block JP8. For more information about jumper configuration, see page 2-23.

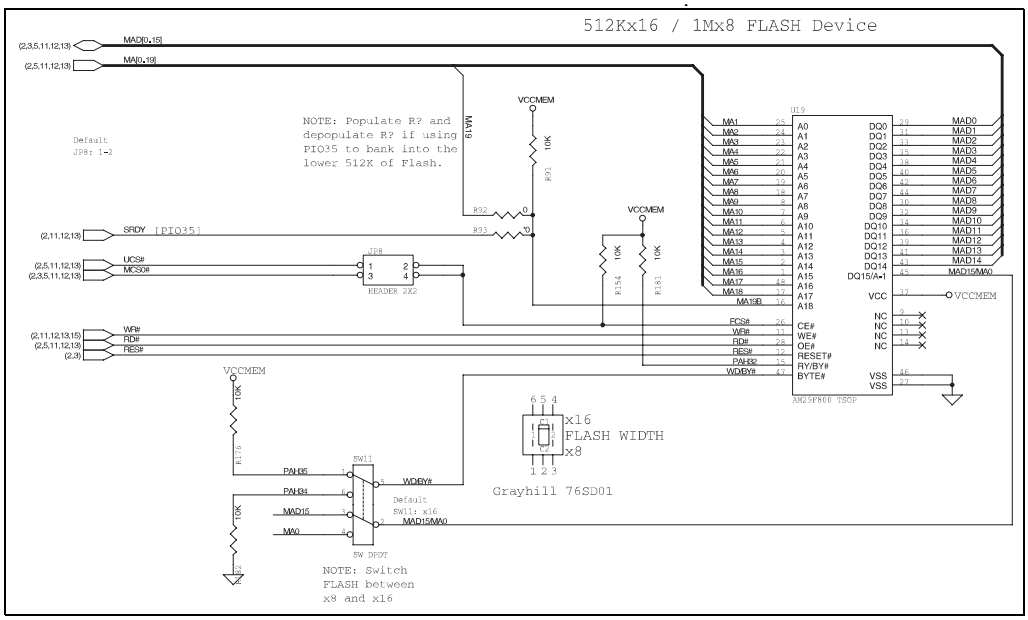


Figure 2-15. Flash Memory Circuit

Configuration Overview

This section describes the options associated with Flash memory and main system memory interfaces.

Flash Memory

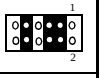
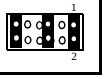
- Flash memory banking select
  Populating R92 enables the highest order address bit to the Flash memory to be routed from A19 (default). Populate R93 to use PIO35 as the Flash memory banking select. To operate the Flash memory in a banking scheme, PIO35 (which is normally High) should be configured to be driven Low when accessing the lower half of the Flash memory.
- JP8: Flash memory chip select
  Jumper block JP8 enables you to route $\overline{\text{UCS}}$ (default) or $\overline{\text{MCS0}}$ as the Flash memory chip select.
- SW11: Flash memory data bus width select
  Switch SW11 is used to determine the Flash memory device data width as x8 or x16 (default). When configuring the Flash data width to 8 bits, the pinstrap $\overline{\text{UCSX8}}$ at SW14 segment 2 must be set to the ON position during reset to configure the Am186CC communications controller to do 8-bit accesses.

SRAM Main Memory

- JP10: SRAM/ROM-ICE chip select
  Jumper block JP10 enables you to route $\overline{\text{LCS}}$, $\overline{\text{UCS}}$, or $\overline{\text{MCS0}}$ to the SRAM socket's chip select.
- JP11: SRAM/ROM-ICE device select
  Jumper block JP11 is used along with JP12 to select the different SRAM and ROM configurations.
- JP12: SRAM/ROM-ICE device select
  Jumper block JP12 is used along with JP11 to select the different SRAM and ROM configurations.

Table 2-6 on page 2-24 shows the jumper selections for the various SRAM and ROM options. Figure 2-16 on page 2-25 (or sheet 5 of the main board schematics included in your kit) shows the SRAM sockets. Table 2-7 on page 2-26 lists the SRAM and ROM pinouts.

Table 2-6. DIP x8/x16 SRAM, ROM-ICE Device Selection

Device	P29LB	JP12 P2SEL	P1SEL	P31SEL	JP11 P30SEL	P29HB	Visual Detail JP12	Visual Detail JP11
SRAM 128Kx8	9-10	7-8	NC	9-10	7-8	3-4		
SRAM 128Kx16	9-10	5-6	NC	9-10	7-8	3-4		
SRAM 512Kx8	9-10	7-8	3-4	9-10	5-6	3-4		
SRAM 512Kx16	9-10	5-6	1-2	9-10	5-6	3-4		
ROM 128Kx16	11-12	5-6	NC	NC	NC	1-2		
ROM 512Kx16	11-12	5-6	NC	11-12	5-6	1-2		

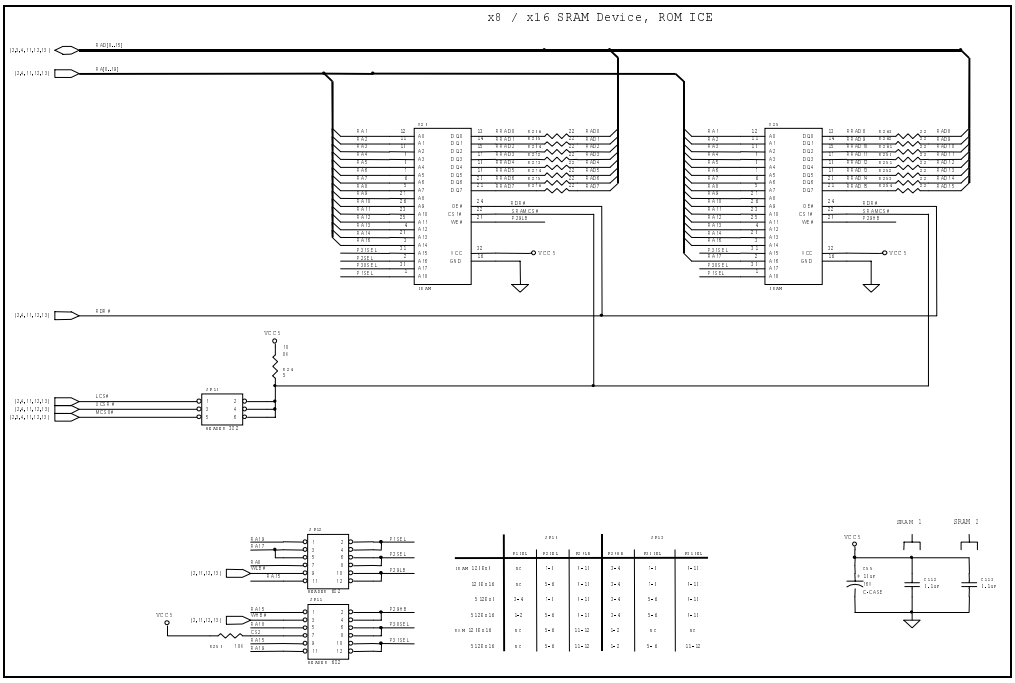


Figure 2-16. DIP SRAM Sockets

Table 2-7. SRAM and ROM Pinouts

Pin	SRAM (128K x 8)	SRAM (512K x 8)	ROM (128K x 8)	ROM (256K x 8)	ROM (512K x 8)
1	NC	A18	VPP	VPP	VPP
2	A16	A16	A16	A16	A16
3	A14	A14	A15	A15	A15
4	A12	A12	A12	A12	A12
5	A7	A7	A7	A7	A7
6	A6	A6	A6	A6	A6
7	A5	A5	A5	A5	A5
8	A4	A4	A4	A4	A4
9	A3	A3	A3	A3	A3
10	A2	A2	A2	A2	A2
11	A1	A1	A1	A1	A1
12	A0	A0	A0	A0	A0
13	D0	D0	D0	D0	D0
14	D1	D1	D1	D1	D1
15	D2	D2	D2	D2	D2
16	GND	GND	GND	GND	GND
17	D3	D3	D3	D3	D3
18	D4	D4	D4	D4	D4
19	D5	D5	D5	D5	D5
20	D6	D6	D6	D6	D6
21	D7	D7	D7	D7	D7
22	CE	CE	CE	CE	CE
23	A10	A10	A10	A10	A10
24	OE	OE	OE	OE	OE
25	A11	A11	A11	A11	A11
26	A9	A9	A9	A9	A9
27	A8	A8	A8	A8	A8
28	A13	A13	A13	A13	A13
29	WE	WE	A14	A14	A14
30	CS2	A17	NC	A17	A17
31	A15	A15	PGM	PGM	A18
32	VCC	VCC	VCC	VCC	VCC

Communication Interfaces

This section describes the communication interfaces available on the Am186CC/CH/CU microcontroller customer development platform's main board.

The communication interface I/O ports include two RS-232 DB-9 interfaces for the low- and high-speed serial ports derived from the integrated Am186CC communications controller UARTs, four RS-530 DB-25 DCE/PCM ports derived from the integrated Am186CC or Am186CH microcontroller HDLC interface, and a peripheral USB port derived from the integrated Am186CC or Am186CU microcontroller USB peripheral controller.

NOTE: The Am186CH HDLC microcontroller provides only two external HDLC interfaces and does not support USB; the Am186CU USB microcontroller provides a USB interface but does not support HDLC.

RS-232 Serial Ports

Two RS-232 serial ports (see Figure 2-17 on page 2-29 or sheet 9 of the main board schematics included in your kit) are configured as data communication equipment (DCE) ports to provide direct connection to a typical data terminal equipment (DTE) port on a PC. This enables you to use a straight serial cable (no null-modem) when connecting to a PC. The Am186CC communications controller High-Speed UART is connected to the DB-9 connector at P15 through an RS-232 transceiver and is capable of a data rate of up to 460 Kbit/s. The low-speed UART is connected to the DB-9 connector at P7 through an RS-232 transceiver and is capable of a data rate of up to 120 Kbit/s.

The CDP main board provides individual status LEDs for the high- and low-speed serial ports (CR6 and CR5, respectively), which illuminate green when data is being transmitted and red when data is being received by the Am186CC communications controller UARTs.

The high- or low-speed serial ports can also be configured to use up to four additional PIOs as additional hardware flow control at JP5 for the high-speed port, and JP3 for the low-speed port. The PIOs are defined in an RS232 serial port configuration as follows:

- PIO0 is used as an output for $\overline{\text{DCD}}$ (Data Carrier Detect).
- PIO1 is used as an input for $\overline{\text{DTR}}$ (Data Terminal Ready).
- PIO27 is used as an output for $\overline{\text{RI}}$ (Ring Indicate).
- PIO28 is used as an output for $\overline{\text{DSR}}$ (Data Set Ready).

Hardware flow control pins $\overline{\text{RTRHU}}$ and $\overline{\text{CTSHU}}$ can be isolated from the high-speed serial port at JP7, so you can use them as their alternate functions and use the serial port without hardware flow control. An alternative is to use PIO45 and PIO44 as the high-speed serial port $\overline{\text{RTRHU}}$ and $\overline{\text{CTSHU}}$ functions. Use this alternative when hardware control is required, and the standard flow control pins $\overline{\text{RTRHU}}$ and $\overline{\text{CTSHU}}$ are used as an alternate function.

You can shut down the serial port RS-232 transceivers by setting SW9 segment 5 (high speed) and 6 (low speed) to the ON position. This feature is used when the Am186CC communications controller UART signals are used for their alternate function.

NOTE: If HDLC Channel D pins are being used as DCE or PCM rather than the UART, SW9 segment 6 must be set to the ON position to prevent contention between the RS-232 transceiver and the desired function.

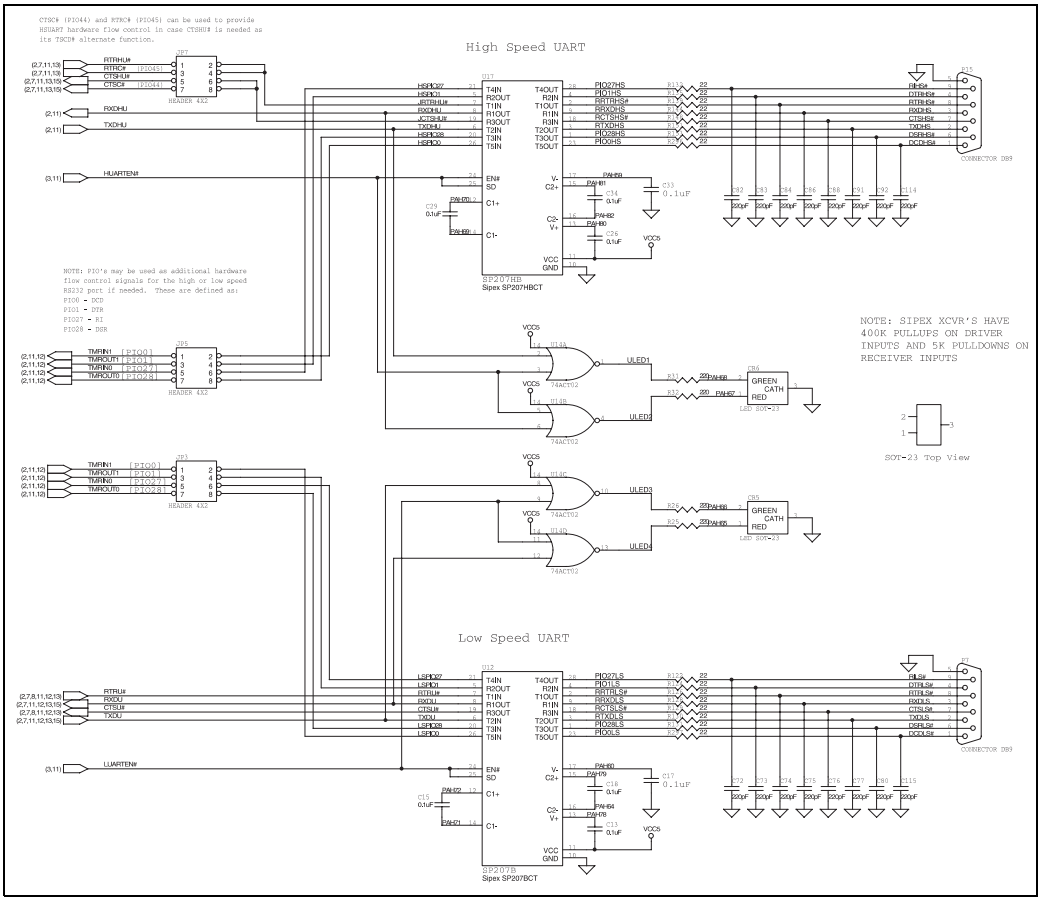


Figure 2-17. RS-232 Serial Port Routing

RS-530 DCE/PCM HDLC Ports

Four HDLC DCE/PCM ports are available on the Am186CC microcontroller (two for the Am186CH microcontroller) via RS-530 DB-25 connectors configured as DCE devices from the integrated HDLC controllers in the two microcontrollers. Figure 2-18 (or sheet 6 of the main board schematics included in your kit) shows a single HDLC RS-530 circuit.

The Am186CH HDLC microcontroller only provides external HDLC interfaces A and B and does not support USB; the Am186CU USB microcontroller provides a USB interface but does not support HDLC.

The RS-530 ports use RS-422 differential transceivers to support up to 10-Mbit/s data transfers. The actual pinout of the four DB-25 connectors allow an RS-530 device to directly connect to the CDP without using a null-modem-like cable adapter. The four RS-530 ports have individual transceiver shutdown switches, a clock generator for DCE and PCM modes, status indicators, and DCE multidrop mode.

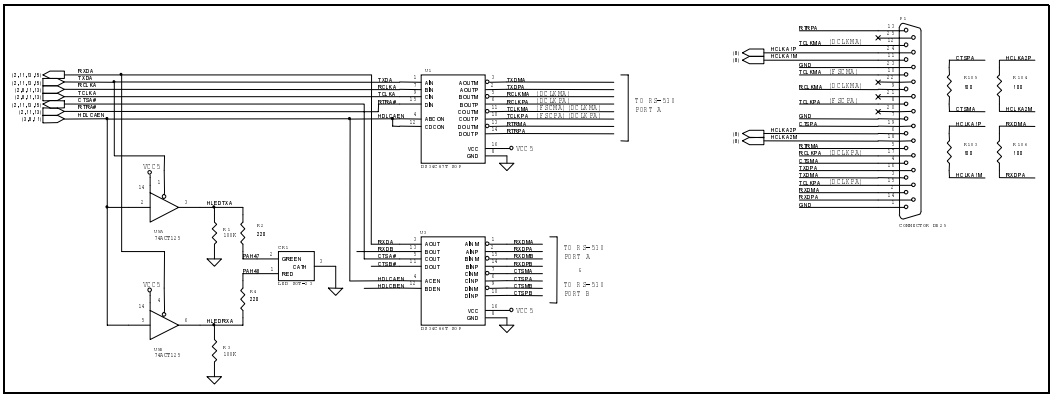


Figure 2-18. HDLC Circuit

You can shut down HDLC ports A–D by setting SW9 segments 1–4, respectively, to the ON position. This enables you to use an alternate function without affecting the board operation. For example, if you want to use GCI mode, set SW9, segment 1 to the ON position. Now you can use GCI mode as an alternate function on the development module.

NOTE: An HDLC interface being used as another function on the CDP must have that function's RS-530 port transceiver shut down to prevent contention between the RS-530 port and the desired HDLC function.

The CDP main board provides individual status LEDs for the four RS-530 DCE/PCM ports A–D, at CR1–CR4, respectively. The status LEDs illuminate green when data is being transmitted, and red when data is being received by the Am186CC or Am186CH microcontroller HDLC RS-530 ports.

The clocking of the DCE or PCM interface is derived from the HDLC clock generator at U11. SW12, SW10, and SW8 are used to define the clocking mode (DCE or PCM) and frequency. JP6, JP4, JP2, and JP1 define how the clocks are routed to each Am186CC or Am186CH microcontroller HDLC RS-530 port. See Table 2-13 on page 2-36. If the HDLC clocks are being generated by a peripheral on the development module, you must remove the appropriate jumper from JP6, JP4, JP2, and JP1.

DCE Mode

The DCE transmit and receive clock to the Am186CC or Am186CH microcontroller can be varied from 78.125 kHz to 10 MHz and can be routed to external devices through the RS-530 ports via a set of four jumper blocks. Three sets of switches define the DCE clocking. The DCE clock is achieved by setting the switches as follows:

- SW9: The HDLC clock generator does not operate for a particular HDLC RS-530 port (A–D) unless that port's shutdown switch SW9 segments 1–4 are in the OFF position. See Table 2-8 on page 2-32.
- SW12: Switch SW12 segments 1–4 must be in the OFF position to indicate DCE clocking mode for RS-530 ports A–D, respectively. See Table 2-8 on page 2-32.
- SW8: Switch SW8 segments 1–3 are used to vary the DCE clock frequency in increments from 78.125 kHz to 10 MHz. See Table 2-9 on page 2-32.

Table 2-8. Switch Options to Enable R-530 DCE Clocking

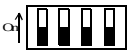
HDLC Port	SW9 Switch					SW12 Switch				
	Segment					Segment				
	1	2	3	4	Visual Detail	1	2	3	4	Visual Detail
A	OFF	–	–	–		OFF	–	–	–	
B	–	OFF	–	–		–	OFF	–	–	
C	–	–	OFF	–		–	–	OFF	–	
D	–	–	–	OFF		–	–	–	OFF	

Table 2-9. Switch Options to Set R-530 DCE Clocking Frequency

DCE Clock Frequency	SW8 Switch				
	Segment				
	1	2	3	4	Visual Detail
78.125 kHz	ON	ON	ON	–	
156.25 kHz	OFF	ON	ON	–	
312.5 kHz	ON	OFF	ON	–	
625 kHz	OFF	OFF	ON	–	
1.25 MHz	ON	ON	OFF	–	
2.5 MHz	OFF	ON	OFF	–	
5 MHz	ON	OFF	OFF	–	
10 MHz	OFF	OFF	OFF	–	

PCM Mode

PCM clocking mode configuration is controlled by the same switches as DCE clocking with the addition of SW10, which provides a variable PCM frame sync. The PCM data clock can be varied from 64 kHz to 8.192 MHz, and the frame sync can be 1, 2, 4, 8, or 16 data clocks wide with positive or negative polarity. The PCM data clock and frame sync are achieved by setting the switches as follows:

- The HDLC clock generator does not operate for a particular HDLC RS-530 port (A–D) unless that port's shutdown switch SW9 segments 1–4 are in the OFF position. See Table 2-10.
- SW12: Switch SW12 segments 1–4 must be in the ON position to indicate PCM clocking mode for RS-530 ports A–D, respectively. See Table 2-10.
- SW10: Switch SW10 segments 1–3 are used to vary the PCM frame sync to 1, 2, 4, 8, or 16 data clock widths (dependent upon data clock frequency) and positive or negative polarity. See Table 2-12 on page 2-35.
- SW8: Switch SW8 segments 1–3 are used to vary the PCM clock frequency in increments from 64 kHz to 8.192 MHz.

Table 2-10. Switch Options to Enable R-530 PCM Clocking

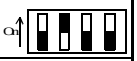
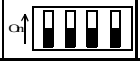
HDLC Port	SW9 Switch					SW12 Switch				
	Segment					Segment				
	1	2	3	4	Visual Detail	1	2	3	4	Visual Detail
A	OFF	–	–	–		ON	–	–	–	
B	–	OFF	–	–		–	ON	–	–	
C	–	–	OFF	–		–	–	ON	–	
D	–	–	–	OFF		–	–	–	ON	

Table 2-11. Switch Options to Set R-530 PCM Clocking Frequency

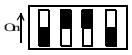
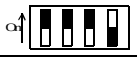
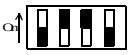
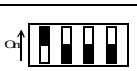
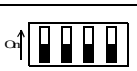
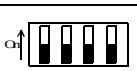
PCM Clock Frequency	SW8 Switch				
	Segment				
	1	2	3	4	Visual Detail
64 kHz	ON	ON	ON	–	
128 kHz	OFF	ON	ON	–	
256 kHz	ON	OFF	ON	–	
512 kHz	OFF	OFF	ON	–	
1.024 MHz	ON	ON	OFF	–	
2.048 MHz	OFF	ON	OFF	–	
4.096 MHz	ON	OFF	OFF	–	
8.192 MHz	OFF	OFF	OFF	–	

Table 2-12. Switch Options to Set R-530 PCM Frame Sync

Data Clock Width[1]	Polarity	SW10 Switch				
		Segment				
		1	2	3	4	Visual Detail
1	1	ON	ON	ON	–	
2^2	1	OFF	ON	ON	–	
4	1	OFF	ON	ON	–	
4^3	1	ON	OFF	ON	–	
8	1	ON	OFF	ON	–	
8^4	1	OFF	OFF	ON	–	
16^5	1	OFF	OFF	ON	–	
1	0	ON	ON	OFF	–	
2^2	0	OFF	ON	OFF	–	
4	0	OFF	ON	OFF	–	
4^3	0	ON	OFF	OFF	–	
8	0	ON	OFF	OFF	–	
8^4	0	OFF	OFF	OFF	–	
16^5	0	OFF	OFF	OFF	–	

1. Frame sync width = Width • Data Clock Period.
2. Only available at 64 kHz and 128 kHz data clocks.
3. At 64 kHz and 128 kHz data clocks only.
4. At 128 kHz data clock only.
5. Only available at 256 kHz–8.192 MHz data clocks.

Table 2-13. HDLC DCE/PCM Clock Routing Options

Clock Source	HDLC Mode		JP6	JP4	JP2	JP1	Visual Detail
	DCE	PCM					
Internal Internal	TCLKA RCLKA	FSCA CLKA	1–2 3–4	—	—	—	
External External	TCLKA RCLKA	FSCA CLKA	5–6 7–8	—	—	—	
Internal Internal	TCLKB RCLKB	FSCB CLKB	—	1–2 3–4	—	—	
External External	TCLKB RCLKB	FSCB CLKB	—	5–6 7–8	—	—	
Internal Internal	TCLKC RCLKC	FSCC CLKC	—	—	1–2 3–4	—	
External External	TCLKC RCLKC	FSCC CLKC	—	—	5–6 7–8	—	
Internal Internal	TCLKD RCLKD	FSCD CLKD	—	—	—	1–2 3–4	
External External	TCLKD RCLKD	FSCD CLKD	—	—	—	5–6 7–8	

DCE Multidrop Mode

Another feature of the CDP main board is the ability of the HDLC ports to operate in multidrop mode by using SW3, SW5, SW6, and SW7. When any of these switches are in the ON position, the transmit (TXD), receive (RXD), and $\overline{\text{CTS}}$ are shorted together.

NOTE: When operating in DCE multidrop mode, the Am186CC communications controller DCE interface TXD pins must be configured as open drain.

Peripheral USB Port

NOTE: USB is supported only on the Am186CC and Am186CU microcontrollers.

The CDP provides a full-speed (12 Mbps) peripheral USB port that enables the CDP to be used as a self-powered USB peripheral.

You can configure the CDP to use the Am186CC or Am186CU microcontroller full-speed (12 Mbps) USB peripheral controller's integrated USB transceiver, or an external transceiver. Using the internal USB transceiver enables the USB differential signaling (USBD+ and USBD–) to directly connect to the USB connector and to a USB host or hub through a standard USB full-speed cable.

When the USB port on the CDP is active, the Am186CC or Am186CU microcontroller's PIO8 signal is driven Low, which illuminates LED CR7.

Configure the optional external USB transceiver by doing the following:

- Remove R49 and R50.
- Populate R42 and R43 with 0-Ω resistors.
- Populate R55 and R56 with 24-Ω resistors.
- Set pinstrap ($\overline{\text{USBXCVR}}$) at SW14, segment 3, to the ON position during reset.

Refer to Figure 2-19 on page 2-38 (or sheet 10 of the main board schematics included in your kit) for the USB circuit diagram.

The Am186CC or Am186CU microcontroller can be used only as a self-powered USB peripheral because of the power requirements needed in the typical TA/modem applications. Because of the USB electrical requirements of self-powered USB peripherals, there is a small amount of glue logic needed to meet the USB specifications. The attach/detach scenarios addressed with this logic are described in the following paragraphs.

Attach

1. The Am186CC or Am186CU microcontroller polls PIO42 for logic High level to detect an active host/hub upstream connection (USBVCC is on). In the case where an active USB host/hub is connected to the CDP USB port and power is not applied to the CDP, Q2 isolates the USBVCC from the CDP to prevent damage to the Am186CC communications controller.
2. The Am186CC or Am186CU microcontroller drives PIO43 High to enable Q1, which pulls R58 up to 3.3 V. This pulls up the USBD+ signal to indicate to the host that a full-speed USB device is present.

Detach

1. Am186CC or Am186CU microcontroller polls PIO42 for a logic Low level to detect a disconnect condition from the host/hub.
2. The Am186CC or Am186CU microcontroller three states USBD+ and USBD– in response to the disconnect.
3. The Am186CC or Am186CU microcontroller drives PIO43 to a logic Low level, which disables Q1 and removes the pullup (R58) from USBD+.

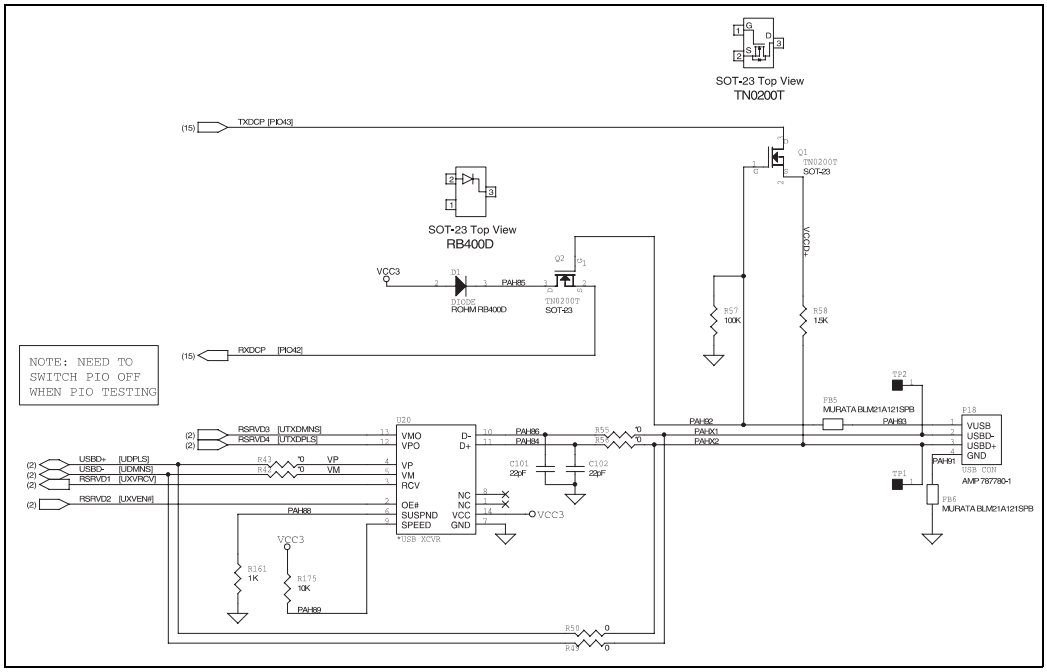


Figure 2-19. Universal Serial Bus Circuit

Debug and Configuration Circuitry

Several debug and configuration options make the Am186CC/CH/CU microcontroller customer development platform a useful tool for the development of specific applications. The CDP offers an interface to the Test Interface Port (TIP) debug card (not included in your kit) that provides status indicators and debug peripherals, debug headers to provide access to most critical pins on the microcontroller, a reset configuration switch to define specific system parameters, and a pinstrap configuration switch to define particular pin functions.

TIP Interface

The TIP is a small debug card to aid in testing, debug, and software development of system applications based on the Am186CC communications controller. The TIP provides the following features:

- An 8-bit on-board Flash device that you can select as the default boot device
- A 2-line x 20-character LCD to provide status information
- Eight hexadecimal LED displays to use for status codes
- Eight readable and writable LEDs for status indication
- Two RS-232 DCE serial ports to enable direct connection to a PC
- A PC-compatible parallel port
- A secondary reset button for the CDP
- A 10BaseT Ethernet port

The interface between the CDP and TIP is set up so it does not use many microcontroller resources. Refer to Figure 2-20 on page 2-41 (or sheet 13 of the main board schematics included in your kit) for a schematic of the TIP connector. The general interface between the CDP and TIP is as follows:

- A19–A0, AD7–AD0, $\overline{RD}$, and $\overline{WLB}$ on the Am186CC communications controller are used to provide communication between the TIP peripherals and the CDP.
- The $\overline{UCS}$ signal on the Am186CC communications controller provides a specific chip select to the 8-bit Flash memory on the TIP. When selecting the TIP as a boot device, the $\overline{UCS}$ signal must be routed to the TIP Flash memory by setting jumper JP1, 1–2 on the TIP and removing the jumper on JP7 of the CDP.

- INT0 on the Am186CC communications controller is used as the TIP Ethernet interrupt signal.
- INT7 on the Am186CC communications controller is used as the TIP serial port 1 interrupt signal.
- INT8 on the Am186CC communications controller is used as the TIP serial port 0 interrupt signal.
- $\overline{\text{PCS3}}$ on the Am186CC communications controller is used as a chip select (AEN) for the TIP Ethernet controller.
- ARDY can be used to add wait states for the TIP Ethernet controller.

NOTE: AD7 is also individually interfaced to the TIP card to identify the TIP being attached through the Am186CC/CH/CU microcontroller RESCON register.

NOTE: To share all TIP interrupts on the INT0 microcontroller input, populate R279, remove R294, and configure the TIP appropriately.

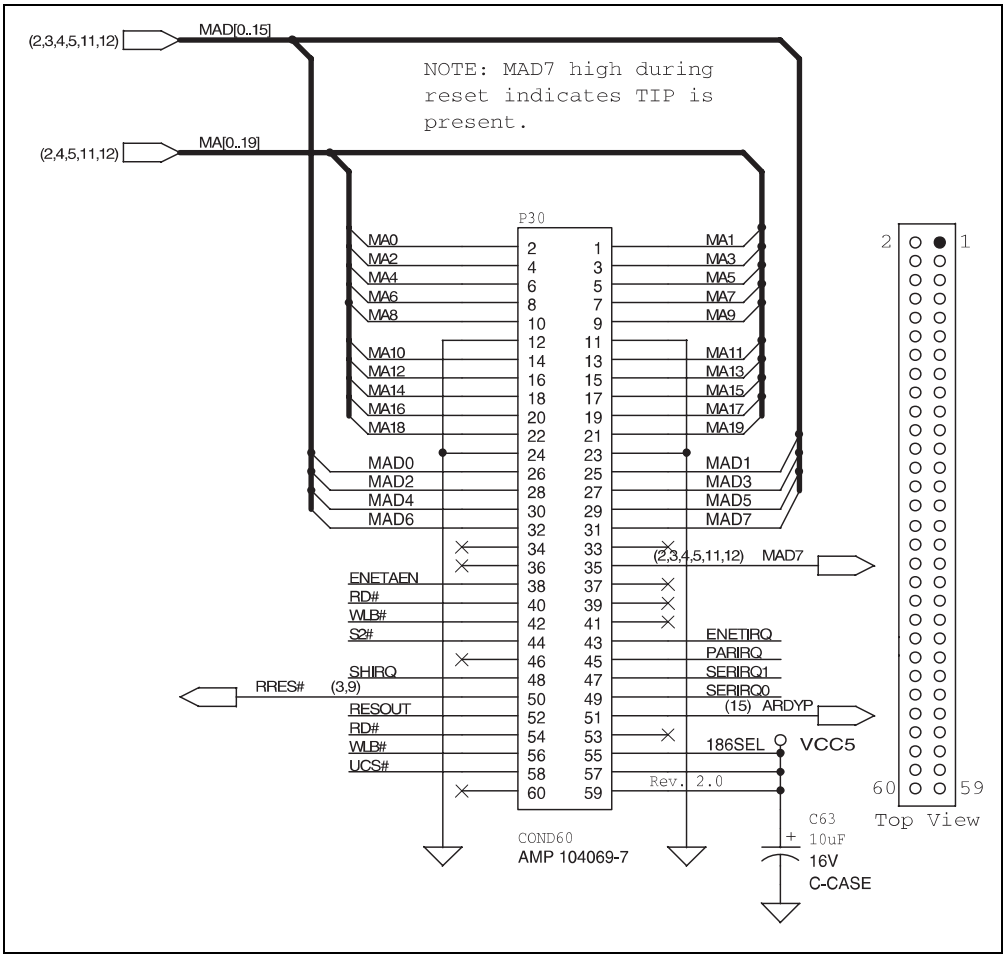


Figure 2-20. Test Interface Port Connector

Debug Headers

Eight 2 x 10 shrouded headers are used to directly interface to the HP 165xx series logic analyzer through HP series termination adapter to the CDP. Figure 2-21 on page 2-43 shows the header layout. Figure 2-22 on page 2-44 (or sheet 11 of the main board schematics included in your kit) shows the header circuit. A majority of the Am186CC communications controller signals are available from these headers with several clocking options for state mode triggering.

The headers are grouped as follows:

- P9: HDLC Ports A and B (Am186CC and Am186CH microcontrollers only), DRQ1–DRQ0
- P10: HDLC Ports C and D (Am186CC communications controller only), UCLK as clock input
- P13: INT8–INT0, NMI, TMRIN1–TMRIN0, TMROUT1–TMROUT0, HOLD, HLDA
- P14: $\overline{\text{PCS7}}$–$\overline{\text{PCS0}}$, SSI port
- P16: $\overline{\text{UCS}}$, $\overline{\text{LCS}}$, $\overline{\text{MCS3}}$–$\overline{\text{MCS0}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{WLB}}$, $\overline{\text{WHB}}$, $\overline{\text{RD}}$ as clock input
- P17: RESOUT, $\overline{\text{S2}}$–$\overline{\text{S0}}$, S6, $\overline{\text{BHE}}$, ALE, $\overline{\text{DEN}}$, DT/$\overline{\text{R}}$, SRDY, ARDY, QS1–QS0, $\overline{\text{BSIZE8}}$
- P20: A15–A0, $\overline{\text{WR}}$ as clock input
- P21: AD15–AD0, jumper option for CLKOUT as clock input

Two additional 2 x 25 shrouded headers at locations P8 and P11 are available to enable additional access to all PIOs, interrupt pins, chip selects, and to provide the ability to control (via software) the transceiver shutdown signaling for the UART and HDLC transceivers.

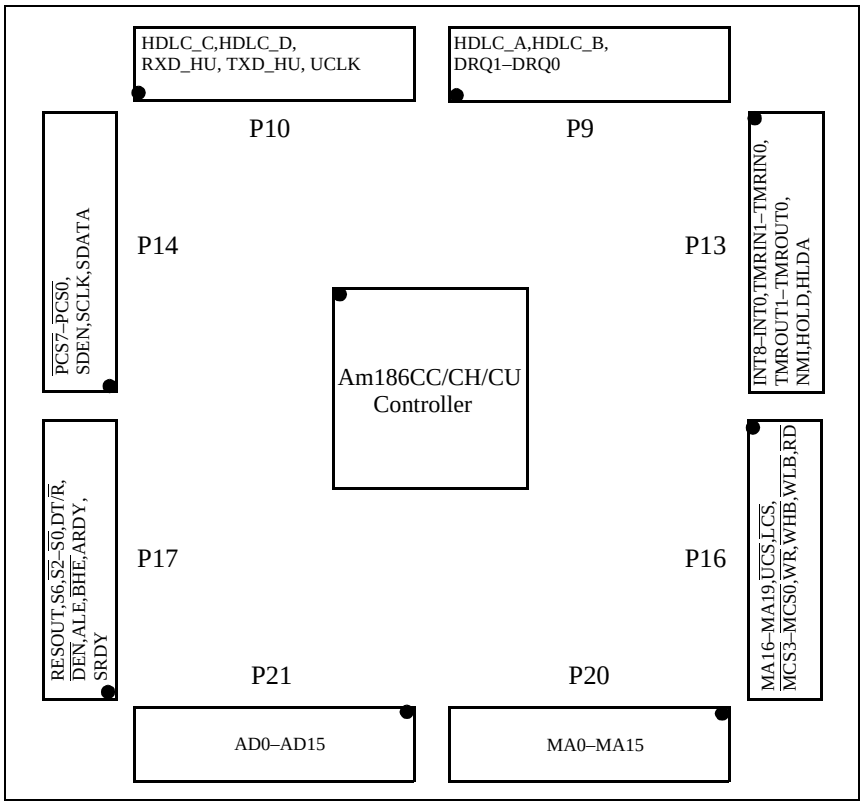


Figure 2-21. HP Header Grouping

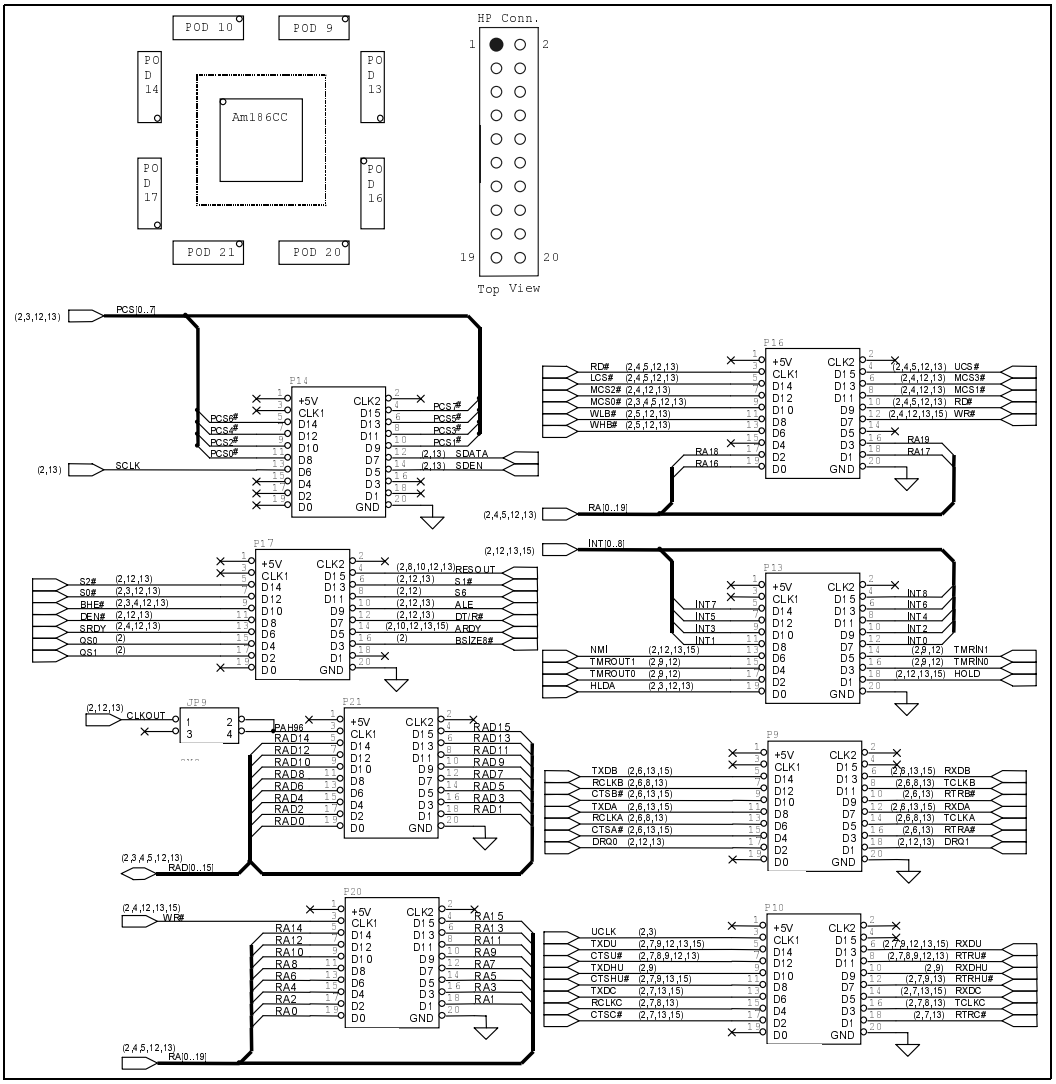


Figure 2-22. Debug Header Circuit

Reset Configuration

SW13 and SW15 are used to define the state of the RESCON register bits AD15–AD0. The RESCON register identifies a bit as a logic High when a switch segment is in the ON position. For details, see Figure 2-24 on page 2-46 or sheet 3 of the main board schematics included in your kit.

The RESCON register provides a way to make design-specific hardware configuration information available to software. This information is latched into the RESCON register from the state of AD[0..15] during reset. The Am186CC/CH/CU microcontroller's weak internal pulldowns default AD[0..15] Low during reset. SW13 and SW15 can be used to set individual bits AD[0..15] High by setting the appropriate switch segment to the ON position. Figure 2-23 shows the RESCON register bits.

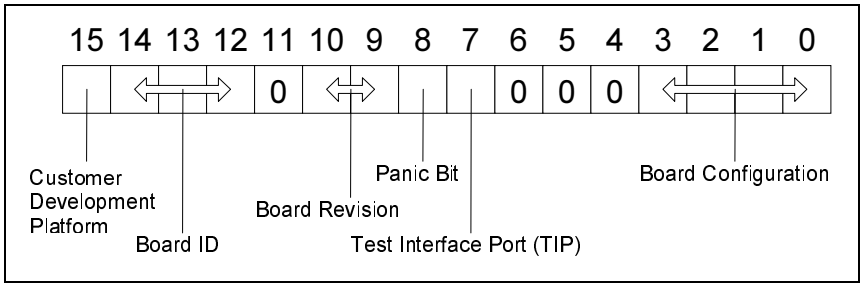


Figure 2-23. RESCON Register Bits

- **Customer Development Platform:** Identifies if the board is a CDP.
- **Board ID:** Unique board identifier that is used to determine what features are available to the software.
- **0:** Bits are reserved for future use.
- **Panic Bit:** Used by E86MON software to boot in a "safe mode".
- **TIP:** Identifies the TIP board as being present in the system.
- **Board Configuration:** Identifies particular population option for the board.

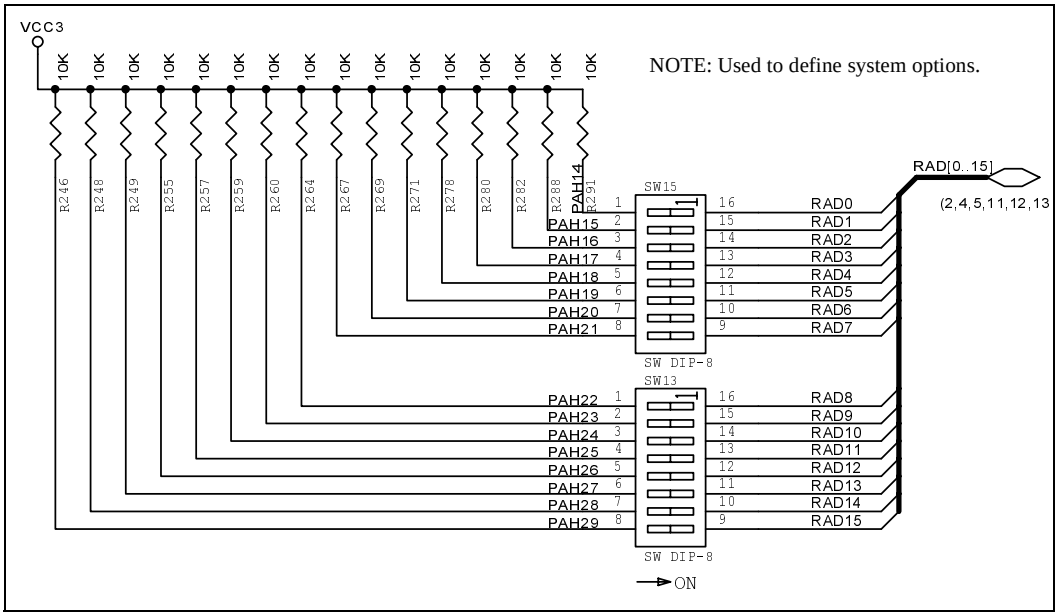


Figure 2-24. Reset Configuration Switches

Pinstrap Configuration

Pinstrap configuration is used to define a particular Am186CC communications controller function of a pin or interface at power up. All pinstraps have a logic High state during reset as the default. The pinstrap switches SW14 and SW16 enable you to define and vary system configuration as needed. The following options are available:

System and USB PLL clocking modes

SW16 segments 1 and 2 are used for the pinstraps controlling the system clock PLL mode on the CDP. The default setting for the system PLL is 2x PLL mode to attain a 40-MHz system frequency with the 20-MHz crystal input. Setting a segment of SW16 to the ON position during system reset indicates a logic 0, and setting a segment of SW16 to the OFF position indicates a logic 1.

SW16 segments 3 and 4 are used for the pinstraps controlling the USB clock PLL mode on the CDP. The default setting for the USB PLL is 2x PLL mode to attain a 48-MHz USB frequency with the 24-MHz crystal input. Setting a segment of SW16 to the ON position during system reset indicates a logic 0; setting a segment of SW16 to the OFF position indicates a logic 1. See Figure 2-25 (or sheet 3 of the main board schematics included in your kit), Table 2-14, and Table 2-15 for more information.

Table 2-14. System and USB Clock Modes[1]

CPU	PLL Mode	SW16 Segment 1	SW16 Segment 2	SW16 Segment 3	SW16 Segment 4
	1x	ON	OFF	X	X
	2x	OFF	OFF	X	X
	4x	OFF	ON	X	X
	Bypass	ON	ON	X	X
USB	**PLL Mode**	**SW16 Segment 1**	**SW16 Segment 2**	**SW16 Segment 3**	**SW16 Segment 4**
	System Clock	X	X	OFF	OFF
	2x	X	X	ON	OFF
	4x	X	X	OFF	ON

1. If you do not want to use the USB PLL or you are using the Am186CH HDLC microcontroller, which does not support USB, the USBX1 input must be tied to V_{SS}.To do this, install a 0-Ω resistor at location C42.

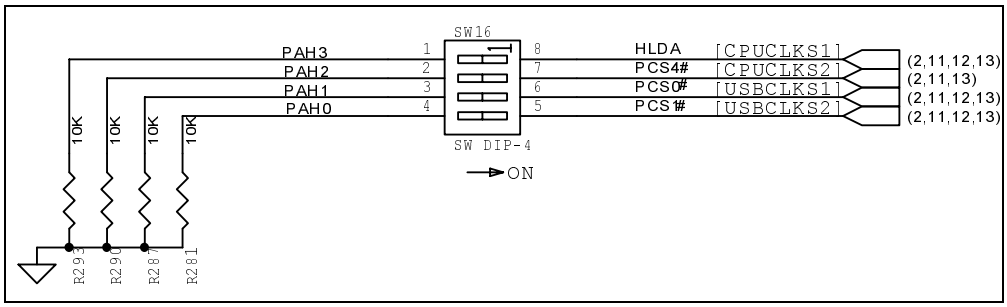


Figure 2-25. CPU/PLL Pinstrap Circuit

Table 2-15. CPU and USB Clocking Options

Clock	PLL Mode			PLL Bypass	Oscillator
	1x	2x	4x		
System clock	16–40 MHz	8–25 MHz	8–12.5 MHz	0–24 MHz	0–40 MHz
USB clock[1]	–	24 Mhz	12 MHz	–	12, 24 MHz
Shared system/ USB clock	–	24 Mhz	12 MHz	–	12, 24 MHz
UART clock	–	–	–	–	0–40 MHz[2]

1. The USB clock is supported on the Am186CC and Am186CU microcontrollers only.
2. UCLK is limited to the maximum frequency of the system clock.

Flash memory boot width

SW14 segment 2 is used to define the Flash memory boot width as x8 or x16. The default setting is 16 bits and is set when SW14 segment 2 is in the OFF position. Setting SW14 segment 2 to the ON position during reset defines the boot width as 8 bits. Refer to Figure 2-26 on page 2-49 (or sheet 3 of the main board schematics included in your kit).

NOTE: If booting from the CDP Flash memory in 8-bit mode, SW14 segment 2 must be in the ON position, and SW11 must be set to the x8 position.

Turn off address phase of the AD bus

You can turn off the address phase of the AD bus by setting SW14 segment 1 to the ON position during reset and setting the appropriate Am186CC communications controller registers. Refer to Figure 2-26 on page 2-49 (or sheet 3 of the main board schematics included in your kit).

Use an external USB transceiver

To use an external USB transceiver, move resistors R49 and R50 to locations R42 and R43, populate R55 and R56 with 24-Ω resistors, and set SW14 segment 3 to the ON position. Refer to Figure 2-19 on page 2-38 (or sheet 10 of the main board schematics included in your kit) and Figure 2-26 on page 2-49 (or sheet 3 of the main board schematics included in your kit).

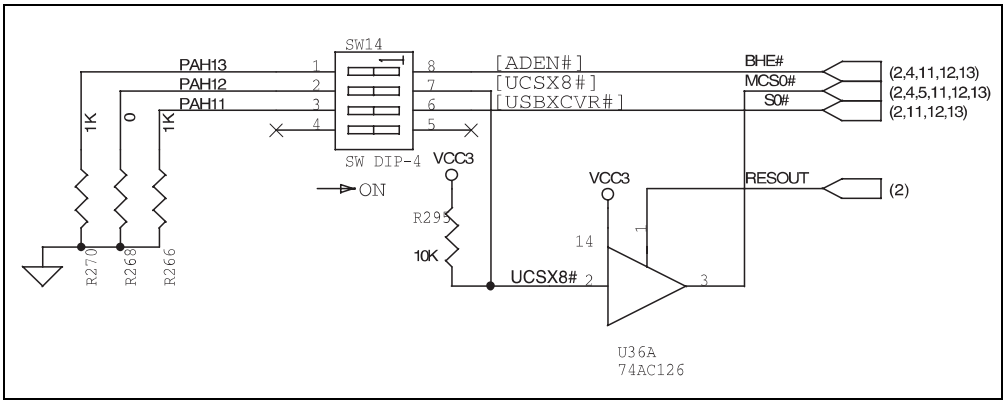


Figure 2-26. Miscellaneous Pinstrap Circuit

Expansion Interfaces

The Am186CC/CH/CU microcontroller customer development platform supports two expansion interfaces: the Am186 processor local bus expansion interface, which is electrically and physically compatible to the existing Am186 family demonstration boards, and the development module interface, which can be used for the ISDN/router development module.

Am186™ Processor Expansion Interface

The Am186 processor local bus expansion interface, located at P26 and P27, supports the PC/104 form-factor expansion connector for additional prototyping and testing. The traditional PC/104 signals are not present on the board; however, the Am186 processor expansion interface enables you to attach wirewrap or prototype boards that have the same standard physical interface. The electrical interface is similar to the PC104, but is not fully compatible to the PC104 electrical standard. The physical orientation and pinouts are shown in Figure 2-27 or sheet 12 of the main board schematics included in your kit.

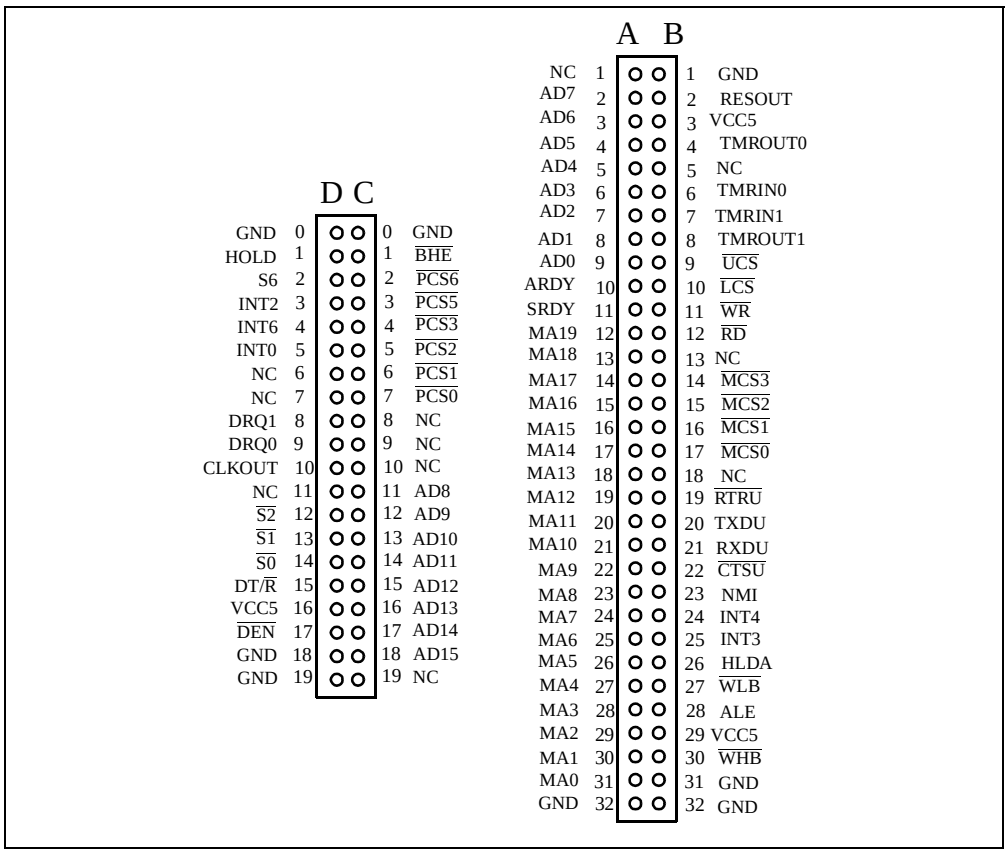


Figure 2-27. Am186™ Processor Expansion Interface

Development Module Interface

The development module interface, located at P19 and P12, is primarily used to provide an interface to the ISDN/router development module. This module enables the CDP to be used as a specific system application. The module connectors contain all the signals needed to develop particular applications based on the Am186CC communications controller. See Figure 2-28 on page 2-52 (or sheet 13 of the main board schematics included in your kit) for the development module interface.

Interfaces provided include the following:

- 3.3 V, 5 V, –5 V, –24 V, and –70 V power
- Full address and data buses
- All 14 memory and peripheral chip selects
- Nine external interrupt pins
- Full control and status pins
- Four full HDLC interfaces (HDLC Channels A and B supported on the Am186CC and Am186CH microcontrollers only. HDLC Channels C and D supported on the Am186CC communications controller only.)
- SSI interface

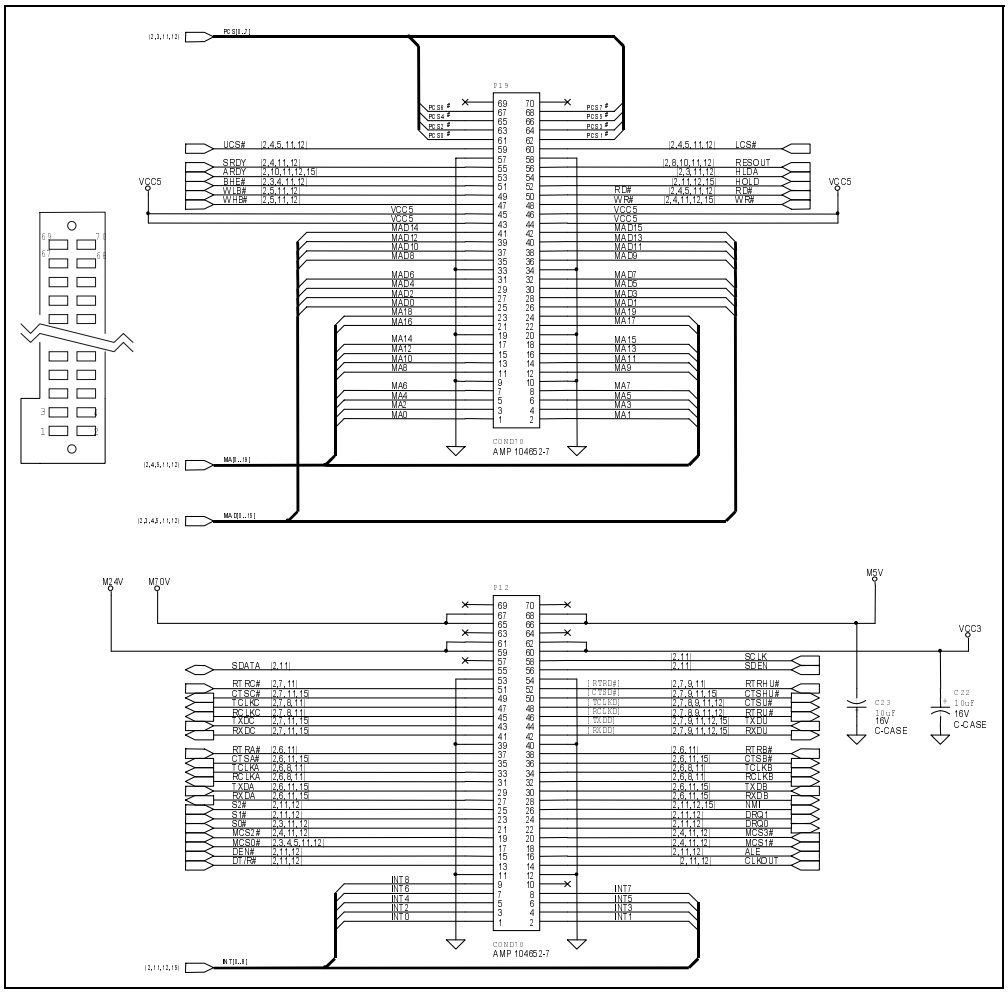


Figure 2-28. Router/ISDN Development Module Interface

Chapter 3

Development Module Functional Description

The Am186CC/CH/CU microcontroller customer development platform (CDP) consists of two boards: a main board that contains an Am186CC communications controller and interfaces, and the development module, which you can use to develop ISDN and router applications. This chapter describes the development module. The main board is described in Chapter 2, “Main Board Functional Description”.

Read the following sections to learn more about the development module:

Development Module Layout

Figure 3-1 (or sheet 2 of the development module schematics included in your kit) shows a block diagram of the Am186CC/CH/CU microcontroller CDP development module; Figure 3-2 on page 3-3 shows the layout of the development module.

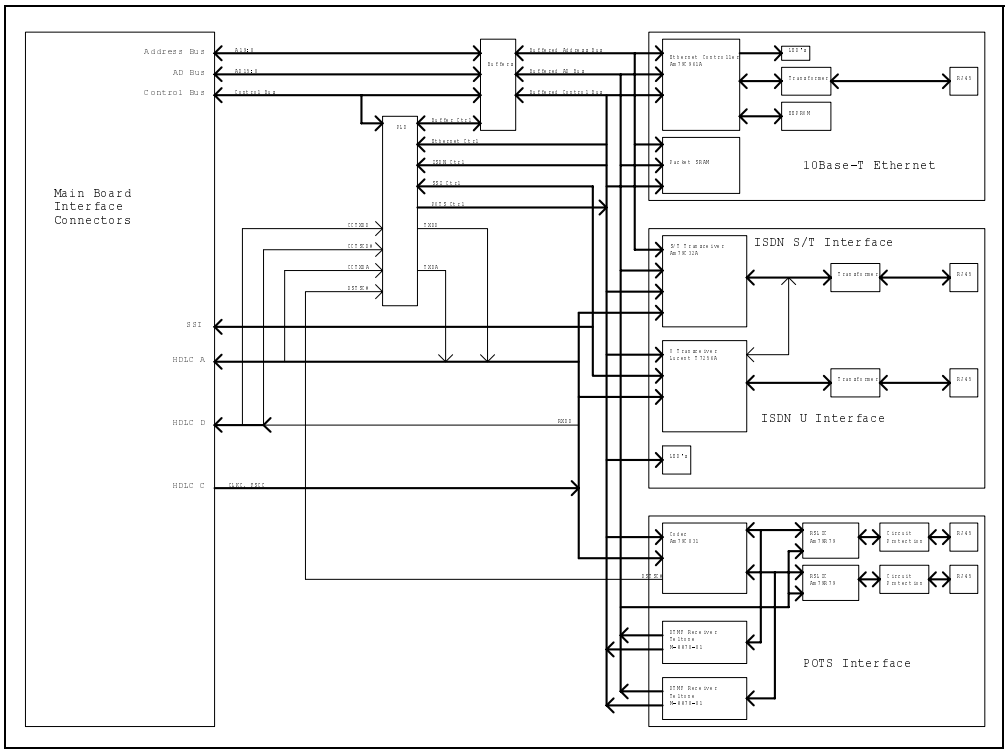


Figure 3-1. Router/ISDN Development Module Block Diagram (same as Figure 0-2)

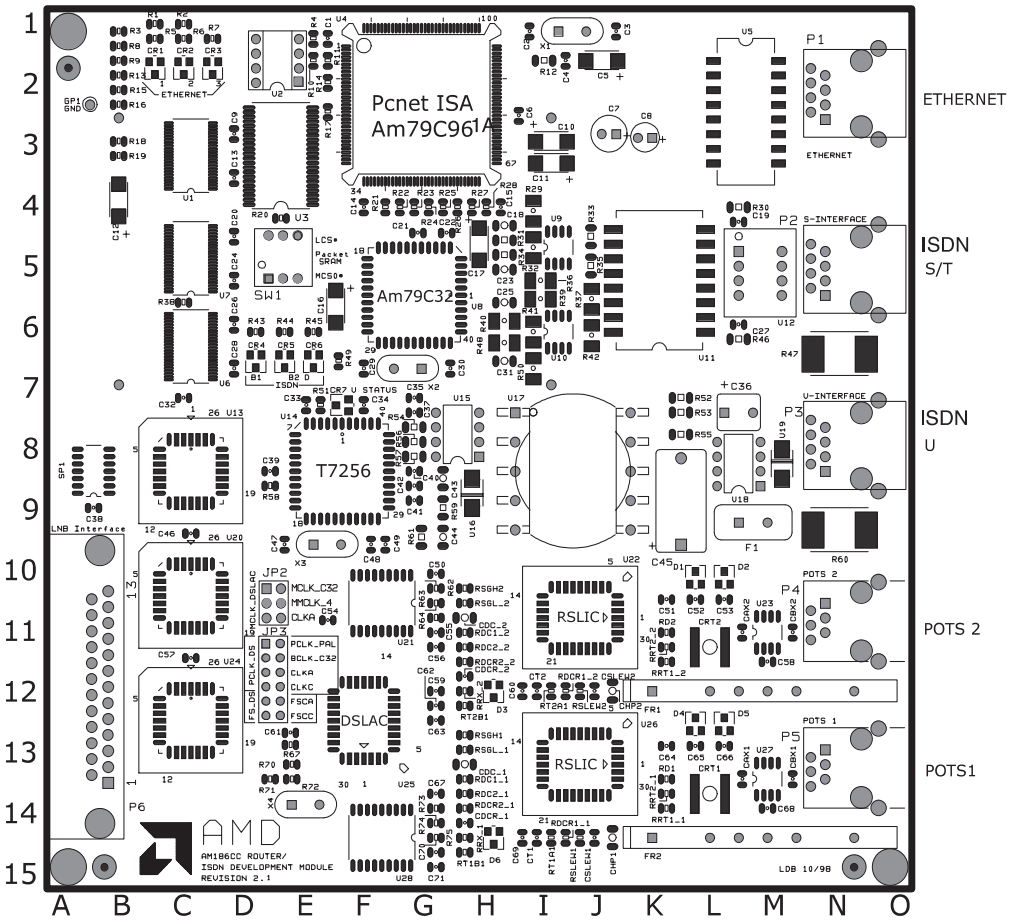


Figure 3-2. Router/ISDN Development Module Layout Diagram

Customer Development Platform Development Module Features

The development module is a 6-layer, 6- x 6-inch printed circuit board used to target specific communication-based system applications using the Am186CC communications controller. The development module interfaces to the CDP main board through two 2 x 35 pin connectors. This interface enables you to use the CDP development module and provides you with a vehicle to develop specific applications.

The development module contains the system components used in developing ISDN terminal adapter/modem and low-end router applications that use many AMD-specific devices.

This section describes the following development module features:

Main Board Interface

The development module is a printed circuit board that attaches to the Am186CC/CH/CU microcontroller CDP main board through two 2 x 35, surface-mount, keyed connectors (AMP104693-7). The connectors are three inches apart and have a 390-mil mated height clearance between the main board and the development module. Figure 3-3 on page 3-5 shows the connection between the main board and the development module. Figure 3-4 on page 3-6 (or sheet 3 of the development module schematics included in your kit) shows the connector layout.

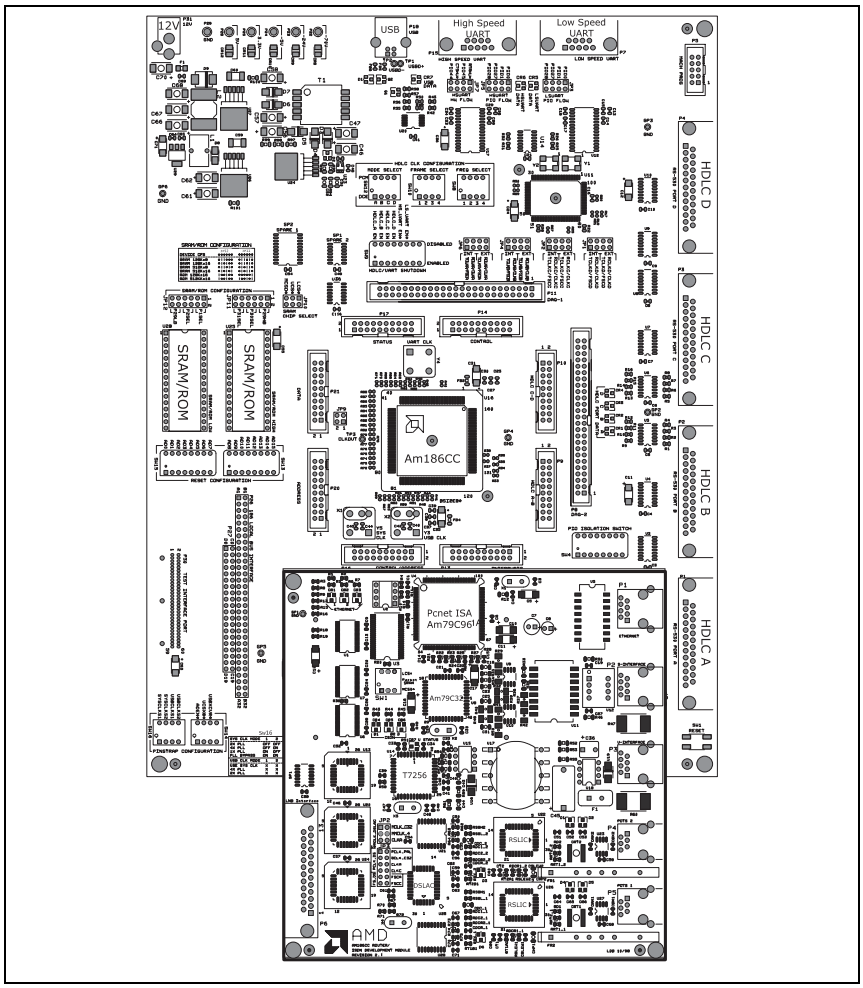


Figure 3-3. Main Board and Development Module Connection

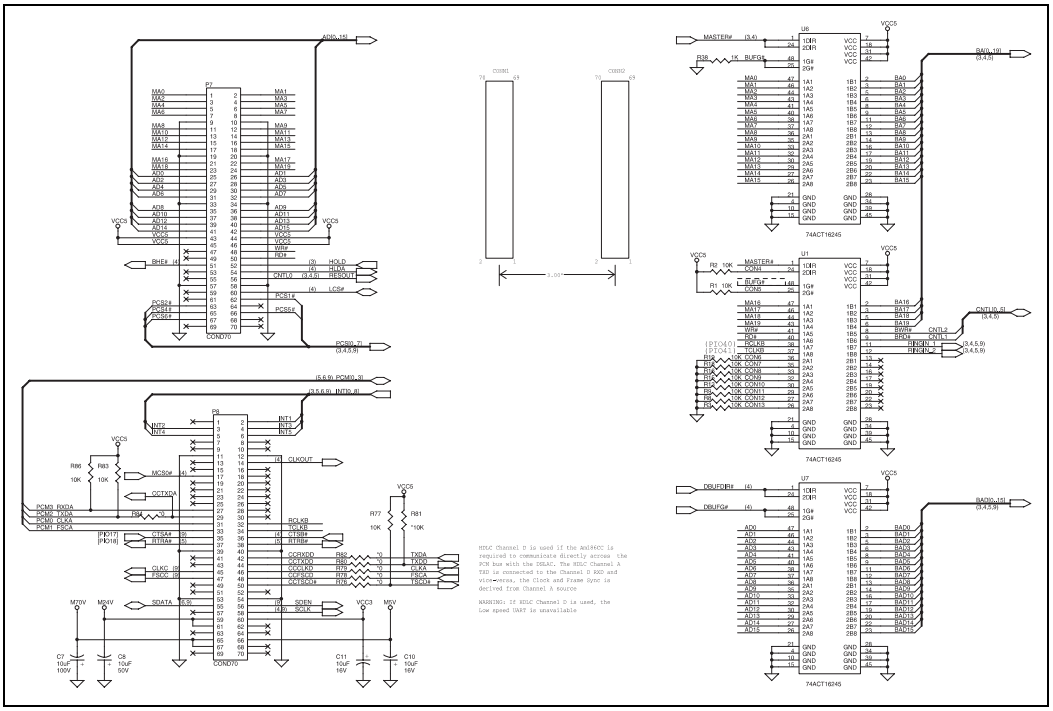


Figure 3-4. Router/ISDN Development Module Connector Layout Diagram

The interface between the Am186CC/CH/CU microcontroller CDP main board and development module incorporates the full Am186CC communications controller local bus address, data, and most control signals. The interface also supports the four external HDLC interfaces (see note), SSI, and the 3.3-V, 5-V, –5-V, –24-V, and –70-V power supplies.

NOTE: The Am186CC communications controller provides four HDLC channels. The Am186CH HDLC microcontroller provides two HDLC channels. The Am186CU USB microcontroller *does not* support HDLC. HDLC channel A, and optionally, HDLC channel D, are the only HDLC channels used on the ISDN development module.

The two module connectors separate the high-speed Am186CC communications controller local bus interface from the communications-specific interfaces such as the HDLC interfaces, SSI, and the power supply.

Because of the large number of devices connected to the Am186CC communications controller local bus on the CDP main board and development module, the full address bus, AD bus, and heavily loaded control signals are buffered. The buffering prevents excess loading, which can affect timing and possibly cause functional errors at higher bus frequencies.

The development module uses three 74ACT16245 16-bit transceivers to buffer the signals previously described. Typically, bidirectional buffering is not required for the address and control buses; however, because the module incorporates a bus mastering Ethernet controller (AMD Am79C961A), control of these buses is given to the bus mastering device. Control logic for the buffers is incorporated in a programmable logic device (PLD), U13, used on the development module (see Figure 3-4 on page 3-6).

10BaseT Ethernet Interface

The Am186CC/CH/CU microcontroller CDP development module uses an AMD Am79C961A PCnet™-ISA II Ethernet controller configured in bus master mode for its Ethernet interface. The Ethernet interface consists of a connection between the PCnet-ISA II twisted pair interface to an RJ45 connector, a 20-MHz crystal, an optional EEPROM for Plug-n-Play (PnP) capability, three status LEDs, SRAM used to transfer Ethernet packet data, and a small amount of glue logic required to interface the Am186CC communications controller to the PCnet-ISA II Ethernet controller.

The development module provides Ethernet through the PCnet-ISA II twisted pair interface with the addition of a single 10BaseT transformer (U5) to the RJ-45 connector at P1. To link the Ethernet station to a network, connect the straight-through cable provided in your kit to a hub that sits on the network.

Figure 3-5 on page 3-8 and Table 3-1 on page 3-8 show the pin assignment and pin functions for the RJ-45 connector.

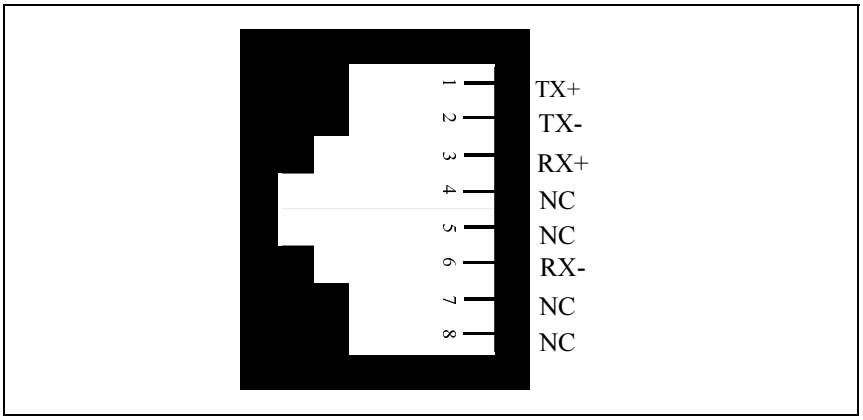


Figure 3-5. Front View of the RJ-45 Connector

Table 3-1. RJ-45 Connector Pin Functions

Pin Number	Function
1	TX+
2	TX-
3	RX+
4	Not used
5	Not used
6	RX–
7	Not used
8	Not used

Three LEDs (CR1–CR3) on the Ethernet controller interface provide status information for the port. The function of these LEDs is controlled by the ISA bus configuration registers on the PCnet-ISA II Ethernet controller and can be modified through software or the EEPROM. The default functions of the LEDs are shown in Table 3-2.

Table 3-2. PCnet™-ISA II Ethernet Controller LED Status Information

LED	Ethernet Controller Signal Name	LED Function
CR1	LED0	Indicates a good 10BaseT connection.
CR2	LED1	Indicates receive activity from the network.
CR3	LED3	Indicates transmit activity from the network.

The module can be configured to use the 64K x 16 on-board SRAM or main system memory as the Ethernet packet SRAM. When the main system memory is DRAM, the development module's 64K x 16 SRAM must be used as packet memory because the Ethernet controller DMAs directly to the SRAM and cannot bus master to DRAM.

The default configuration of the CDP uses DRAM as main system memory and the 64K x 16 SRAM as the Ethernet packet memory. In this configuration, the DRAM resides in the lower 512 Kbytes of memory space from 00000h–7FFFFh, and the 128 Kbytes of Ethernet packet SRAM uses $\overline{\text{MCS0}}$ space located from 80000h–9FFFFh.

When SRAM is used as main system memory, the Ethernet packet SRAM and the system memory both reside in $\overline{\text{LCS}}$ space from 00000h–7FFFFh. The packet SRAM configuration is selected by setting jumper JP1 at the appropriate position: $\overline{\text{LCS}}$ or $\overline{\text{MCS0}}$.

A small amount of glue logic is required to interface the PCnet-ISA II Ethernet controller to the Am186CC communications controller because the PCnet-ISA II Ethernet controller is an ISA peripheral device. The required logic is achieved through an Am22V10 PLD at location U13. Refer to location C8 in Figure 3-2 on page 3-3. The PLD controls three signals between the Ethernet controller and the Am186CC communications controller: $\overline{\text{SRAMCS}}$, $\overline{\text{SBHE}}$, and $\overline{\text{BHLDA}}$.

The PLD creates the Ethernet packet SRAM chip select, $\overline{\text{SRAMCS}}$, from the $\overline{\text{MASTER}}$ output when the PCnet-ISA II Ethernet controller is the bus master. When the Am186CC communications controller is the bus master, the $\overline{\text{SRAMCS}}$ output is three-stated and $\overline{\text{MCS0}}$ is used as the packet SRAM chip select.

$\overline{\text{SBHE}}$ is modified from the Am186CC communications controller $\overline{\text{BHE}}$ signal to meet ISA specifications required by the PCnet-ISA II Ethernet controller. $\overline{\text{BHLDA}}$ is an inverted Am186CC communications controller HLDA and becomes the PCnet-ISA II DMA acknowledge input ($\overline{\text{DACK}}$). Refer to Appendix G for a full listing of PLD equations.

Figure 3-6 (or sheet 4 of the main board schematics and sheet 5 of the development module schematics included in your kit) show the 10BaseT Ethernet interface. Figure 3-7 on page 3-11 (or sheet 4 of the development module schematics included in your kit) shows the Ethernet controller.

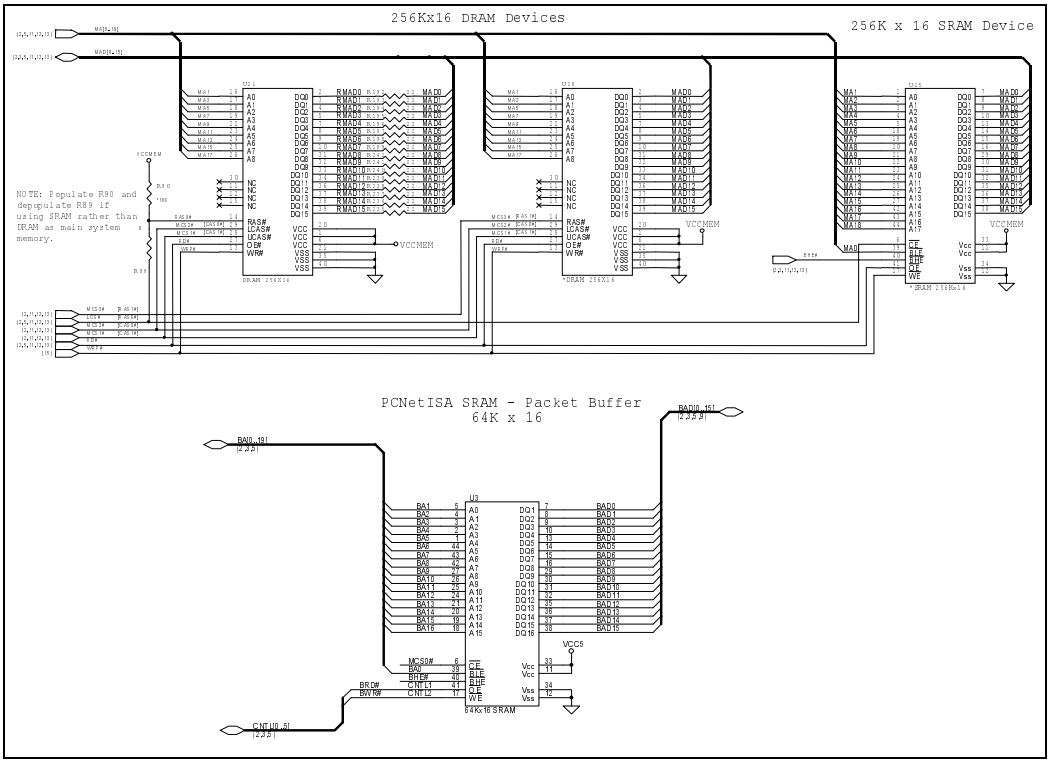


Figure 3-6. 10BaseT Ethernet Interface

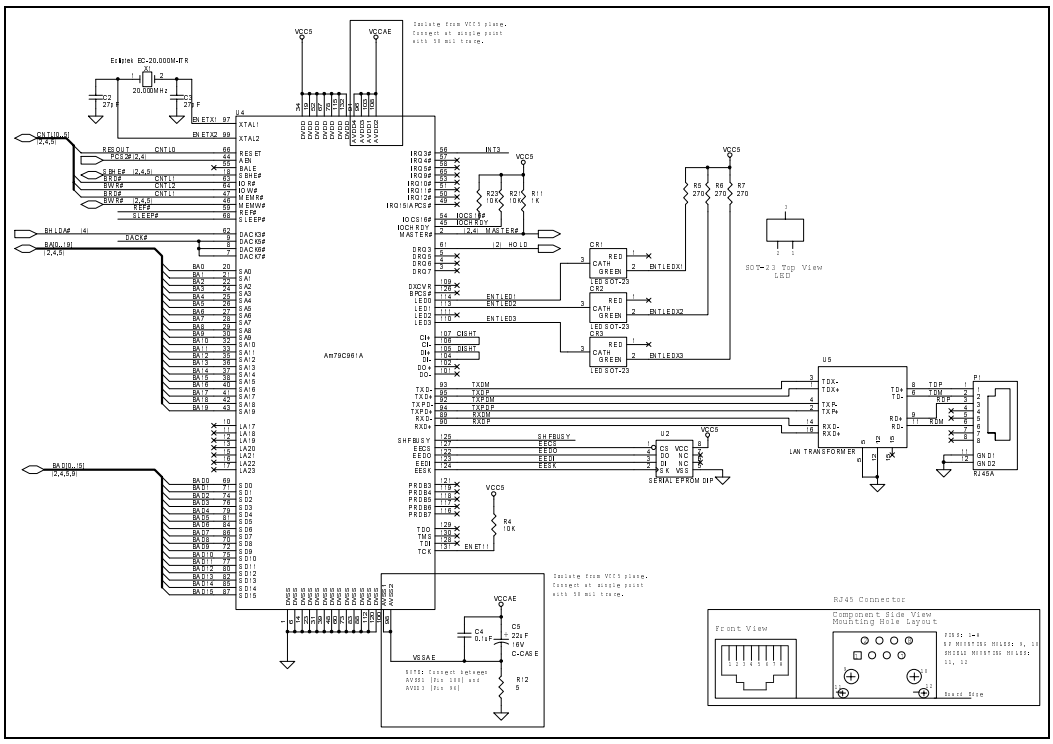


Figure 3-7. Ethernet Controller Schematic

ISDN Interface

The Am186CC/CH/CU microcontroller CDP development module provides both ISDN S/T and U interfaces. You must use these interfaces independently unless you have physically configured the module as a network termination (NT1) device through a population option. The four-wire 2B+D S/T interface connects through an RJ-45 connection at P2 by using the Am186CC communications controller with the AMD Am79C32A DSC circuit. This connection provides the path between a TE (terminal equipment) and NT1 device, and is the ISDN interface commonly used in businesses and in Europe.

The two-wire 2B+D U interface uses the Lucent T7256A NT1 device. The NT1 device provides the termination point at the RJ-45 connection at P3 between the local exchange (LE) and ISDN Terminal Equipment (TE1), and between the terminal adapter (TA) and non-ISDN terminal equipment (TE2). The U interface is the main ISDN interface provided in North America and Asia. The default configuration of the NT1 in this design is to provide a connection between a TA interface to a PC and a TE2 interface to two plain old telephone service (POTS) phones. Refer to Figure 3-8 for an illustration of the ISDN reference points.

Three LEDs (CR4–CR6) are used to indicate activity on the ISDN B1, B2, and D channels using Am186CC communications controller signals PIO18, PIO39, and PIO32, respectively.

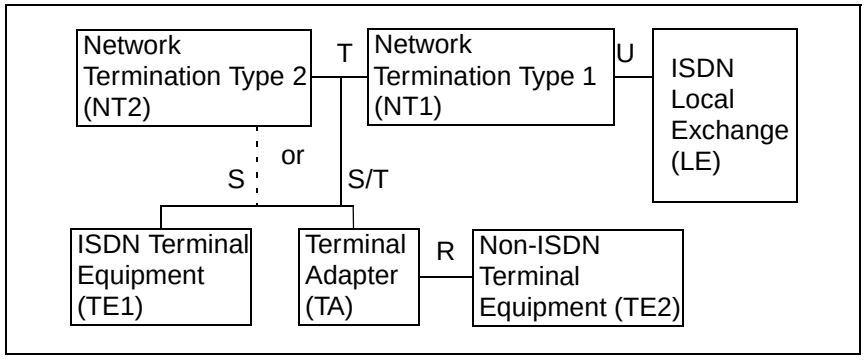


Figure 3-8. ISDN Reference Point Block Diagram

ISDN S/T Interface

The glueless connection between the Am186CC communications controller and the Am79C32A ISDN DSC circuit provides the four-wire 2B+D S/T interface. The DSC serial interface is capable of being configured as an IOM-2 or SBP serial microprocessor interface. This interface is used to transfer data to and from the Am186CC communications controller using the microcontroller's integrated HDLC in GCI or PCM mode; the Am186CC communications controller x86 microprocessor interface is used for configuration.

The Am186CC communications controller provides a full-duplex path between the TE and NT device or the PABX linecard. It processes the ISDN BRI bit stream, which consists of two 64-Kbit/s B channels and a single 16-Kbit/s D channel. The four-wire ISDN S/T interface is first directed through an S transformer and line filtering devices, which isolate and protect the modem from the outside lines. The schematic for the S/T interface block is shown in Figure 3-9 on page 3-14 (or sheet 6 of the development module schematics included in your kit).

In the default S/T configuration, the Am79C32A DSC circuit is operating in SBP mode. The Am79C32A DSC circuit is also providing the clock and frame sync to the Am186CC communications controller across the integrated HDLC A interface, which is configured in PCM mode, and to the Am79C031dual channel codec (DSLAC) device (PCM Codec) used for the POTS interface.

In a second configuration, the Am79C32A DSC circuit is operating in IOM-2 mode; the Am186CC communications controller is in GCI mode; and the DSLAC device is in PCM mode. In this configuration, the data clock for the DSLAC is generated by the BCLK output from the Am79C32A DSC circuit.

A third configuration uses the Am79C2A DSC circuit in an IOM-2 mode. The Am186CC communications controller provides a GCI-to-PCM conversion of the data clock and frame sync to enable the Am79C031 DSLAC device (PCM Codec), to communicate directly between the Am79C32A DSC circuit and the Am79C031 DSLAC device for the POTS interface. Refer to "POTS Interface" on page 3-18 for more information about this configuration.

The Am79C32A DSC circuit uses the $\overline{\text{PCS1}}$ (peripheral chip select 1) signal, which asserts between addresses 100h and 1FFh, and the INT6 (interrupt 6) signal is edge triggered as an active Low interrupt. The Am79C32A DSC circuit's MCLK output is programmed to be 4.096 MHz and is used to drive the MCLK input to the Am79C031 DSLAC device on the POTS interface through JP2.

A fourth configuration uses the Am79C32A DSC circuit with the T7256A U transceiver. In this mode, the data clock and frame sync are generated by the Am79C32A DSC circuit. Data is passed from the Am186CC communications controller or POTS interface through the Am79C32A DSC circuit to the T7256A U transceiver through the S/T interface. For configuration details, refer to "ISDN U Interface" on page 3-15.

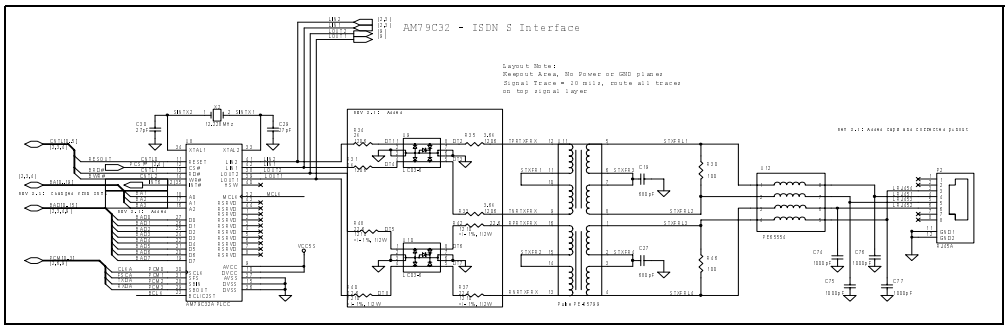


Figure 3-9. ISDN S/T Interface

ISDN U Interface

The Lucent T7256A NT1 device provides the two-wire 2B+D U interface to provide two-wire network termination. The NT1 device processes the ISDN BRI bit stream that consists of two 64-Kbit/s B channels and a single 16-Kbit/s D channel. The U interface circuit includes a line fuse, U transformer, DC termination IC, and opto-isolation circuitry.

The U interface default configuration uses the Am186CC or Am186CH microcontroller SSI interface to configure the NT1; the NT1 TDM bus is used to transfer data between the NT1 device and either the microcontroller's integrated HDLC in PCM mode, or the POTS interface.

The microcontroller's SSI interface to the NT1 microprocessor's serial interface is controlled by the PLD (U13). The PLD is required to select the NT1 microprocessor's serial interface because the NT1 device does not have an SSI chip enable, and the development module's POTS interface DSLAC device also has an SSI interface. The PLD uses the Am186CC or Am186CH microcontroller's PIO38 signal asserted Low to pass the SSI clock to the NT1 device during NT1 configuration.

The NT1 TDM bus is the PCM clock master and the upstream device to the Am186CC or Am186CH microcontroller and the DSLAC device in the POTS interface. In this configuration, the TDM bus drives the PCM data clock and frame sync, and transmits data directly to and from the Am186CC or Am186CH microcontroller and the DSLAC device in the POTS interface.

An alternate configuration option uses the Am79C32A DSC circuit and T7256A device together on the module. In this configuration, data is transferred between the Am186CC or Am186CH microcontroller's integrated HDLC and the Am79C32A DSC circuit. The T7256A NT1 device communicates with the Am79C32A DSC circuit through its S/T interface. See Table 3-3 on page 3-16 for configuration information.

CR7 is used for NT1 device status. The four states of the LED are off, on, 1 Hz, and 8 Hz. Table 3-4 on page 3-16 shows the U interface LED status. The schematic for the U interface block is shown in Figure 3-10 on page 3-17 (or sheet 7 of the development module schematics included in your kit).

Table 3-3. U Interface Configuration

Reference	U Interface Mode	
	T7256A	**Am79C32A/T7256A**
C18	Depopulate	Populate
C23	Depopulate	Populate
C25	Depopulate	Populate
C31	Depopulate	Populate
R29	Depopulate	Populate
R32	Depopulate	Populate
R36	Depopulate	Populate
R39	Depopulate	Populate
R41	Depopulate	Populate
R49	Populate	Depopulate
R50	Depopulate	Populate
R31	Populate	Depopulate
R34	Populate	Depopulate
R40	Populate	Depopulate
R48	Populate	Depopulate

Table 3-4. U Interface LED Status

CR7 State	CR7 Function
OFF	U and S/T interface not active
1 Hz Flashing	U interface activation in progress
8 Hz Flashing	U interface active, S/T not fully active
ON	U and S/T interface fully active

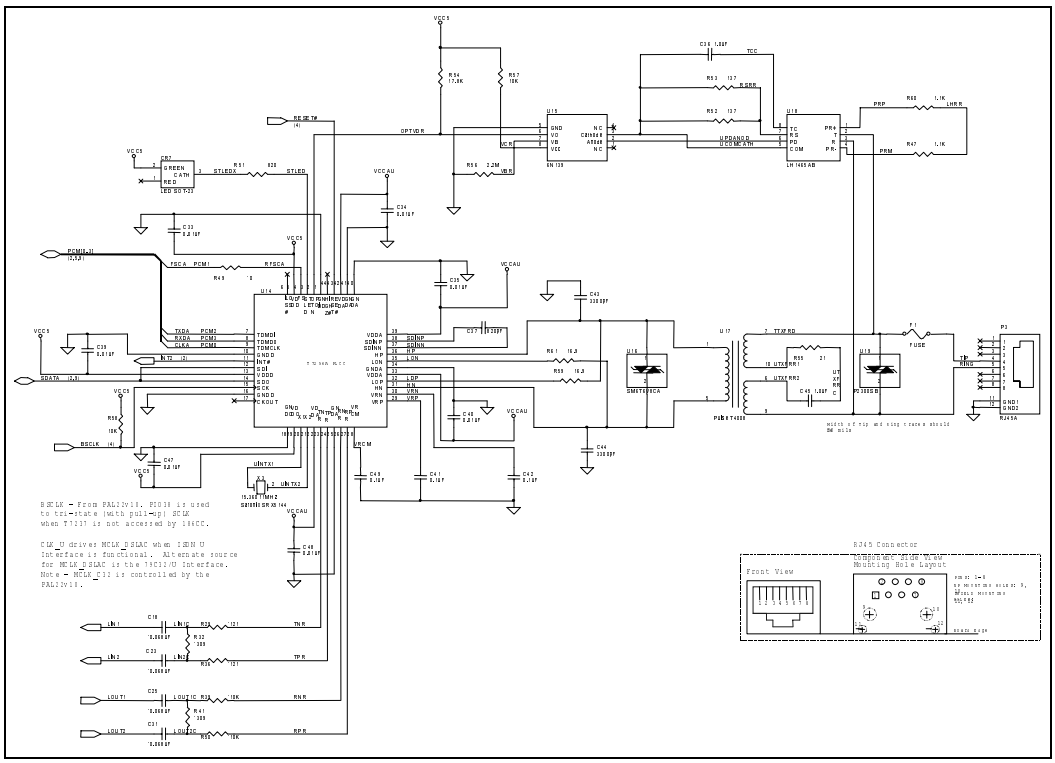


Figure 3-10. ISDN U Interface

In the ISDN U configuration, the Am186CC communications controller uses the SSI and INT2 as an edge-triggered, active Low interrupt to configure the T7256A device through its serial microprocessor interface. The T7256A 2B+D channel communication is performed across the T7256A time-division multiplex (TDM) bus, which is directly connected to Am186CC communications controller HDLC channel A, configured in PCM mode. The T7256A device provides a 2.048-MHz clock and frame sync to transfer data between the TDM and the Am186CC communications controller PCM interface, and the Am79C031 codec PCM bus for the POTS interface.

POTS Interface

The Am186CC/CH/CU microcontroller CDP development module provides two POTS connections on RJ-11 connectors at P5 and P4. These POTS connections are used to plug standard POTS telephones in an ISDN terminal adapter or router application.

To accomplish this, the development module's Am79R79 ringing SLIC (RSLIC) device and one half of an Am79C031 DSLAC device provide an interface to plug in a POTS telephone to communicate across an ISDN B channel.

The basic premise of this type of application is to bring all the functions normally performed at a central office on a normal POTS line to the user's home or office. The Am79R79 RSLIC device provides the DC power, ringing, and supervisory functions to the phone. The Am79C031 DSLAC device provides the analog voice-to-digital conversion to allow communication to the ISDN interface transceivers.

The development module also provides the appropriate voltages needed for the DSLAC and RSLIC devices, signaling for ring generation to the Am79R79 RSLIC device, and DTMF decoders that detect dial tone pairs from the POTS telephone, and transfer that information to the Am186CC communications controller. In addition, a low noise board (LNB) interface enables the user to disable the DSLAC and RSLIC used on the development module and use the LNB boards for the POTS interface.

DSLAC™ Device PCM Interface

The DSLAC device PCM interface connects directly to the following:

- Am79C32A DSC circuit S/T transceiver peripheral port bus, configured in serial bus port (SBP) or IOM-2 mode
- T7256A U transceiver TDM bus
- Am186CC communications controller HDLC channel A interface in PCM or GCI mode; channel D interface in PCM mode

Figure 3-11 on page 3-19 (or sheet 10 of the development module schematics included in your kit) shows the DSLAC device circuitry.

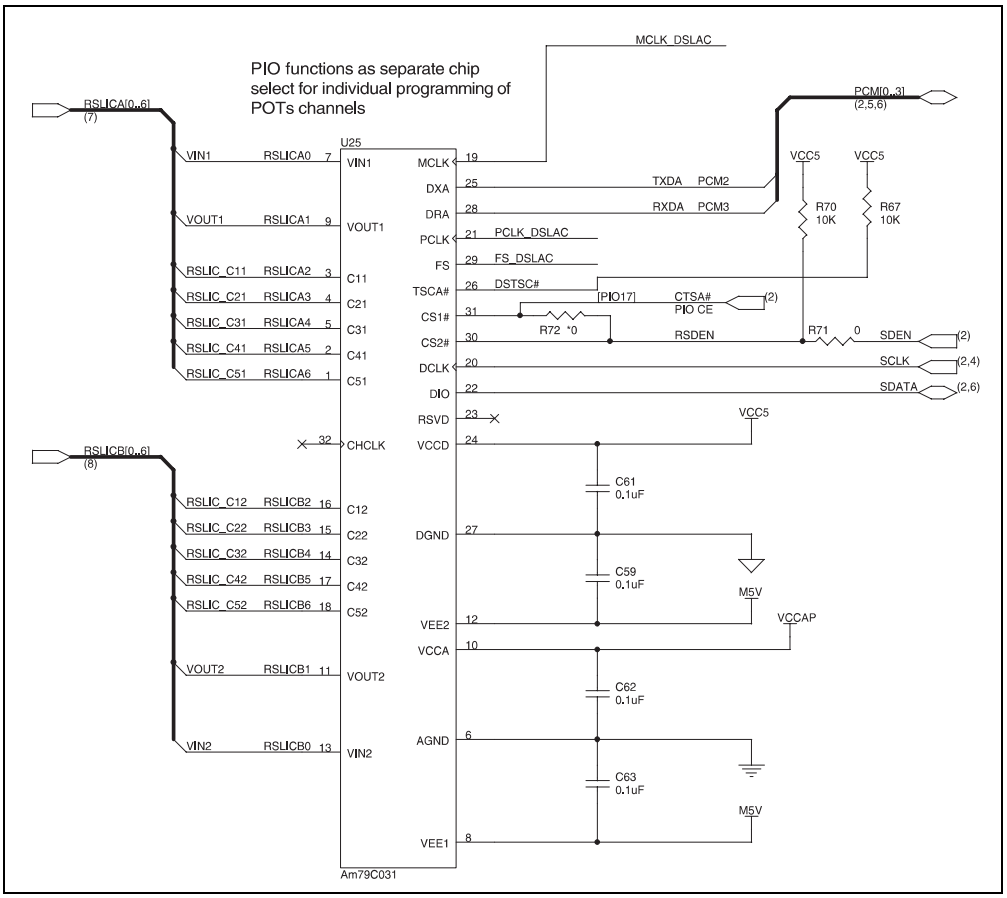


Figure 3-11. DSLAC™ Device Circuitry

In the default configuration, the S/T or U transceiver provides the clock and frame sync for the PCM interface and transfers data directly between the ISDN interface and the POTS interface.

Six DSLAC device clocking configurations are available for use on the CDP development module, as listed below. See Table 3-5 on page 3-21 for jumper settings of each mode.

S/T SBP Mode

The DSLAC device's PCLK and MCLK can be generated from the Am79C32A DSC circuit's CLKA and FSCA outputs. In this case, PCLK is a 192-kHz data clock, and MCLK is configured as a 4.096-MHz master clock driven directly into the DSLAC device.

S/T SBP mode with PLD (module_20_u20_pcm_00)

U20 is used to modify the PCLK and MCLK inputs to the DSLAC device to address a potential Am79C32A DSC circuit-to-DSLAC jitter anomaly. Contact customer support for more information. In this case, the MCLK output from the Am79C32A DSC circuit is configured as 12.288 MHz, and the PLD generates the DSLAC device's 768-kHz PCLK and 4.096-MHz MCLK from the 12.288-MHz source.

S/T IOM-2

The DSLAC device's PCLK and MCLK are generated from the Am79C32A DSC circuit's 768-kHz BCLK and programmable 4.096-MHz MCLK outputs, respectively.

S/T IOM-2 with PLD (module_20_u20_gci_00)

U20 is used to modify the PCLK and MCLK inputs to the DSLAC to address a potential Am79C32A DSC circuit-to-DSLAC device jitter anomaly. Contact customer support for more information. In this case, the MCLK output from the Am79C32A DSC circuit is configured as 12.288 MHz, and the PLD generates the DSLAC device's 768-kHz PCLK and 4.096-MHz MCLK from the 12.288-MHz source.

S/T IOM-2 with GCI-to-PCM Conversion

The DSLAC device's PCLK and FS are generated by the Am186CC communications controller CLKC and FSCC outputs, respectively. The DSLAC device's MCLK is generated by the Am79C32A DSC circuit's MCLK output. In this case, the Am79C32A DSC circuit generates the master data clock and frame sync. The Am186CC communications controller receives the master clocks from the Am79C32A DSC circuit and generates a 768-kHz PCM data clock and an 8-kHz frame sync to be used by the DSLAC device.

U PCM

The T7256 U transceiver generates a 2.048-MHz PCLK that can be directly connected to the DSLAC device's PCLK and MCLK inputs.

NOTE: HDLC channel C and GCI are supported only on the Am186CC communications controller.

MCLK is the master clock used to drive the DSLAC device's internal DSP. MCLK must be 2.048 MHz or 4.096 MHz and can be asynchronous to the DSLAC device's PCLK input. The MCLK input is derived from whichever ISDN transceiver is being used as the upstream ISDN device. If the U interface is selected using the T7256 as the clock master, MCLK is derived directly from the 2.048-MHz CLKA output from the T7256A. If the S/T interface is selected as the clock master, PCLK is derived from the Am79C32A DSC circuit MCLK output (MCLK_C32) or from the output and PLD U20, which synchronizes the DSLAC MCLK input to its PCLK input. Table 3-5 shows MCLK jumper configuration.

Table 3-5. Am79C031 DSLAC™ Device PCLK/FS/MCLK Configuration

ISDN Master Mode	DSLAC Device Clocking		
	JP3 Settings		JP2 Settings
	PCLK-DSLAC	FS-DSLAC	MCLK-DSLAC
S/T SBP	5-6	9-10	1-2
S/T SBP PAL[1,2]	1-2	9-10	3-4
S/T IOM-2	3-4	9-10	1-2
S/T IOM-2 PAL	1-2	9-10	3-4
S/T IOM-2 GCI/PCM Conversion[3]	7-8	11-12	3-4
U PCM	5-6	9-10	5-6

1. U20 is used to modify the clocks to properly synchronize to the DSLAC device's PCM timing.
2. Requires PAL at U20 to use PLD code module_20_u20_gci_00 for IOM-2 mode, and module_20_u20_PCM_00 for SBP mode.
3. PCLK and FS for the DSLAC device are generated by the Am186CC communications controller.

Because the Am186CC communications controller and the Am79C031 DSLAC device are both downstream devices to the ISDN controller, the PCM/GCI data is driven from the ISDN device transmit pin (TXD) to the Am186CC communications controller and the DSLAC receive pins (RXD) and vice-versa. This configuration causes a problem when the Am186CC communications controller needs to communicate directly with the DSLAC device on the PCM bus (e.g., for PABX applications).

To solve this problem, the development module has a configuration option to use Am186CC communications controller HDLC interface D to transmit directly to the DSLAC device on the PCM bus. This is achieved by using the Am186CC communications controller PCM time-slot control ($\overline{\text{TSCD}}$) pin and the DSLAC device time-slot control ($\overline{\text{TSC}}$) to transmit only PCM data on the appropriate time slot. PLD U24 controls these functions on the development module. Table 3-6 on page 3-23 shows configuration options.

NOTE: Using HDLC channel D on the development module causes the CDP main board UART to be nonfunctional because the HDLC channel D pins are multiplexed with the UART. The High-Speed UART flow control is also unavailable because the HDLC channel D time-slot control is multiplexed with one of these pins.

The Am186CC communications controller SSI interfaces to the DSLAC device's microprocessor interface for programming and control of the DSLAC device. The default configuration uses PIO17 for the SSI enable for POTS channel 1, and the SDEN signal is used for the SSI enable for POTS channel 2. This allows the two channels to be individually configured. An optional configuration allows the two DSLAC channels to be identically programmed by using SDEN as the SSI enable for both channels. This is achieved by populating R72 and configuring PIO17 as a PIO input.

Table 3-6. Am186™CC Communications Controller/Am79C031 DSLAC™ Communication Configuration

Am186CC Communications Controller/Am79C031 DSLAC Communication				
Component		**Mode**		
Reference	**Value**	**PCM A**	**PCM D**	**GCI A**
R76	0	Depopulate	Populate	Depopulate
R77	10K	Populate	Populate	Populate
R78	0	Depopulate	Populate	Depopulate
R79	0	Depopulate	Populate	Depopulate
R80	0	Depopulate	Populate	Depopulate
R81	10K	Depopulate	Populate	Depopulate
R82	0	Depopulate	Populate	Depopulate
R83	10K	Populate	Populate	Populate
R84	0	Depopulate	Depopulate	Populate
R85	0	Populate	Populate	Depopulate
R86	10K	Populate	Populate	Populate

RSLIC Device Interface

The DSLAC device provides a direct connection to the Am79R79 RSLIC through two sets of data and control I/O signals used for each channel. The data signals are analog signals from the RSLIC device. These analog signals are digitized and transmitted to the PCM bus. The control signals are used to control telephone states and to detect status.

The RSLIC device ringing is generated via a 20-Hz, CMOS-compatible signal. The signal is created through the PLD at U24 from the Am186CC communications controller's PIO40 and PIO41 signals, which correspond to POTS channels 1 and 2, respectively. The PLD takes the 3.3-V, peak-to-peak PIO outputs and converts them to 5-V peak-to-peak to satisfy the requirements for the RSLIC device. Figure 3-12 on page 3-24 (or sheet 8 of the development module schematics included in your kit) show the DSLAC-to-RSLIC circuit interface.

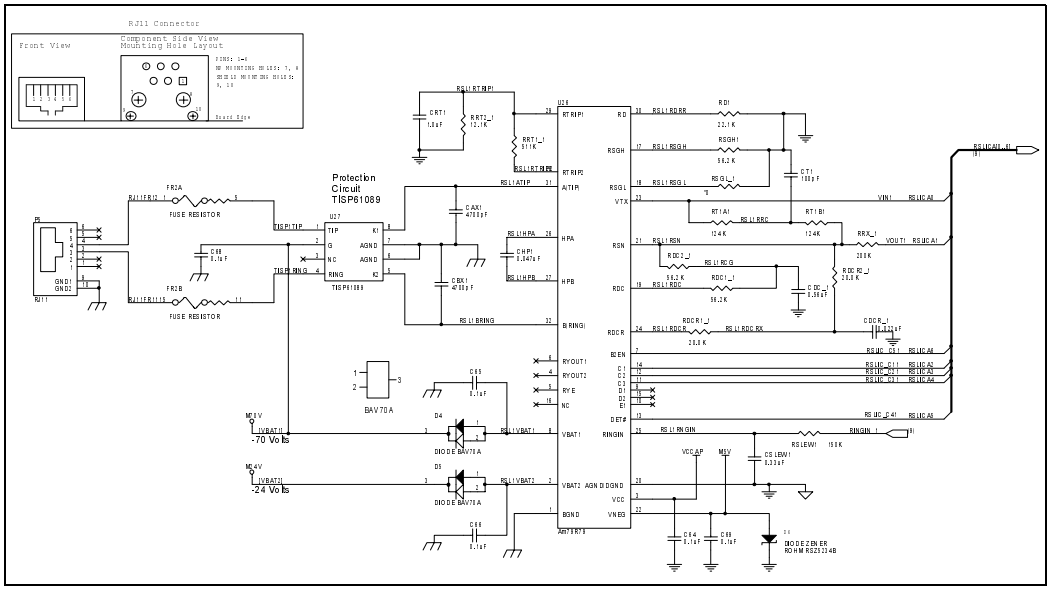


Figure 3-12. DSLAC-to-RSLIC Circuit Interface

Dual Tone Multiple Frequency (DTMF) Interface

The two DTMF receivers are used to detect valid tone pairs from each POTS telephone interface, and then translate them into digital signaling. The digital signaling is used by the Am186CC communications controller to set up and place a call. When a DTMF detects a valid tone pair from the RSLIC device, the DTMF sends an active High interrupt (INT4 for POTS channel 1 and INT5 for POTS channel 2) to the Am186CC communications controller. The DTMF becomes available on the AD3–AD0 after the Am186CC communications controller issues an active High output enable to the corresponding DTMF OE pin. The output enables are generated by inverting $\overline{\text{PCS5}}$ and $\overline{\text{PCS4}}$ for POTS channels 1 and 2, respectively, in the PLD device at U24. Figure 3-13 (or sheet 10 of the development module schematics included in your kit) shows the DTMF circuit.

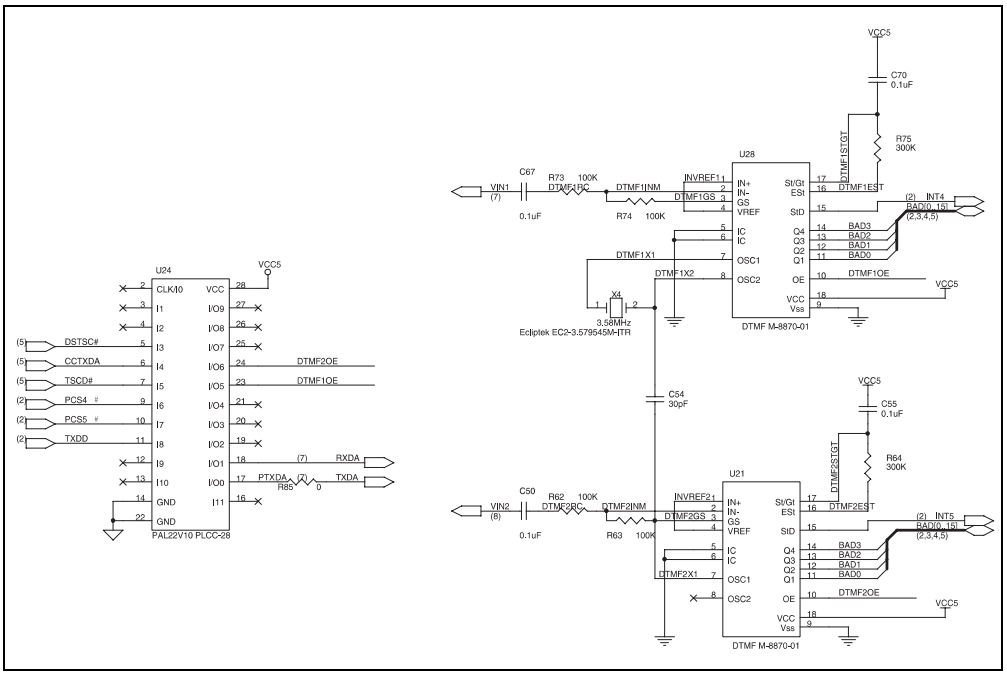


Figure 3-13. DTMF Interface Circuit

Low Noise Board (LNB) Interface

The LNB interface can be used to connect Low Noise Boards developed in AMD's Communication Products Division (CPD). The LNB's are evaluation boards which contain different AMD SLAC and SLIC devices. This feature allows the user to disable the DSLAC and RSLIC used on the development module and use the LNB boards for the POTS interface.

To use the LNB interface, plug the LNB SLAC board into P6. This may be a direct connection if the LNB board contains a DB-25 male connector or may require an adapter cable to interface to the LNB 50-pin male connector. All jumpers from JP3 and R71 must be removed to disable the DSLAC on the development module. In this configuration, the LNB uses the HDLC channel A interface from the development module. The clock and frame sync are driven directly from the PCM or GCI clock master on HDLC channel A and MCLK is driven from the JP3 source.

Appendix A

Default Jumper and Switch Settings

This appendix contains the default jumper and switch settings for the main board and development module.

Table A-1. Main Board Default Jumper and Switch Settings

Part	Number	Position
SW3	1	Off
SW4	1	On
	2	On
SW5	1	Off
SW6	1	Off
SW7	1	Off
SW8	1	Off
	2	Off
	3	Off
	4	Off

Table A-1. Main Board Default Jumper and Switch Settings (Continued)

Part	Number	Position
SW9	1	On
	2	On
	3	On
	4	On
	5	Off
	6	Off
	7	Off
	8	Off
SW10	1	Off
	2	Off
	3	Off
	4	Off
SW11	1	x16
SW12	1	Off
	2	Off
	3	Off
	4	Off
SW13	1	Off
	2	Off
	3	Off
	4	Off
	5	Off
	6	Off
	7	Off
	8	On

Table A-1. Main Board Default Jumper and Switch Settings (Continued)

Part	Number	Position
SW14	1	Off
	2	Off
	3	Off
	4	Off
SW15	1	Off
	2	Off
	3	Off
	4	Off
	5	Off
SW15	6	Off
	7	Off
	8	Off
SW16	1	Off
	2	Off
	3	On
	4	Off
JP1[1]	All	NC
JP2[1]	All	NC
JP3[1]	All	NC
JP4[1]	All	NC
JP5[1]	All	NC
JP6[1]	All	NC
JP7	1-2	$\overline{\text{RTRHU}}$
	5-6	$\overline{\text{CTSHU}}$
JP8	1-2	$\overline{\text{UCS}}$

Table A-1. Main Board Default Jumper and Switch Settings (Continued)

Part	Number	Position
JP9[1]	All	NC
JP10[1]	All	NC
JP11	1-2	NC
	3-4	Connected
	5-6	NC
	7-8	Connected
	9-10	Connected
	11-12	NC

Table A-1. Main Board Default Jumper and Switch Settings (Continued)

Part	Number	Position
JP12	1-2	NC
	3-4	NC
	5-6	Connected
	7-8	NC
	9-10	Connected
	11-12	NC

1. Insert jumper on a signal pin for a no connect (NC).

Table A-2. Router/ISDN Development Module Default Jumper and Switch Settings

Part	Number	Position
SW1	1	$\overline{\text{MCS0}}$
JP2[1]	1-2	NC
	3-4	Connected
	5-6	NC
JP3[1]	1-2	Connected
	3-4	NC
	5-6	NC
	7-8	NC
	9-10	Connected
	11-12	NC

1. Insert jumper on a signal pin for a no connect (NC).

Appendix B

Platform Pin Usage

This appendix provides the Am186CC/CH/CU microcontroller CDP pin usage information in the following tables.

Table B-1. PIO Usage

PIO	Multiplexed Function(s)	Location	Usage	Isolation Method
PIO0	TMRIN1	Main board	Optional $\overline{\text{DCD}}$ hardware flow control for UART or High-Speed UART	Jumper block (**JP5** and **JP3**).
			Am186 processor expansion interface	Do not attach Am186 processor expansion interface card.
PIO1	TMROUT1	Main board	Optional $\overline{\text{DTR}}$ hardware flow control for UART or High-Speed UART	Jumper block (**JP5** and **JP3**).
			Am186 processor expansion interface	Do not attach Am186 processor expansion interface card.
PIO2	$\overline{\text{PCS5}}$	Module	Am186 processor expansion interface	Do not attach 186 local bus expansion interface card.
			Module interface (DTMF1-**U28** OE)	Do not attach module.

Table B-1. PIO Usage (Continued)

PIO	Multiplexed Function(s)	Location	Usage	Isolation Method
PIO3	PCS4 {CLKSEL2}	Module	CPU CLK pinstrap	Pinstrap switch (**SW16**).
			Am186 processor expansion interface	Do not attach Am186 processor expansion interface card.
			Module interface (DTMF2-**U21** OE)	Do not attach module.
PIO4	MCS0 {$\overline{\text{UCSX8}}$}	Module	Flash memory width pinstrap	Pinstrap switch (**SW14**).
			Flash memory chip select	Jumper block (**JP8**).
			SRAM chip select	Jumper block (**JP10**).
			Am186 processor expansion interface	Do not attach Am186 processor expansion interface card.
			Module interface	Do not attach module.
PIO5	MCS3 RAS1	Main board	DRAM bank 1 $\overline{\text{RAS}}$	No bank 1 DRAM (**U18**).
			Am186 processor expansion interface	Do not attach Am186 processor expansion interface card.
			Module interface	Do not attach module.
PIO6	INT8 PWD	Main board	Module interface	Do not attach module.
			TIP interface	Remove R283.
PIO7	INT7	Main board	Module interface	Do not attach module.
			TIP interface	Remove R289.
PIO8	ARDY	Module	Module interface (LED ISDN diagnostics)	Do not attach module.
			TIP interface	PIO isolation switch (**SW4**).

Table B-1. PIO Usage (Continued)

PIO	Multiplexed Function(s)	Location	Usage	Isolation Method
PIO9	DRQ0	None	Am186 processor expansion interface	Do not attach Am186 processor expansion interface card.
			Module interface	Do not attach module.
PIO10	SDEN	Module	Module interface (SSI SLAC chip select)	Do not attach module.
PIO11	SCLK	Module	Module interface (SSI SLAC)	Do not attach module.
PIO12	SDATA	Module	Module interface (SSI SLAC)	Do not attach module.
PIO13	PCS0 {USBSEL1}	Main board	USB CLK pinstrap 186 local bus interface	Pinstrap switch (**SW16**). Do not attach Am186 processor expansion interface card.
			Module interface	Do not attach module.
PIO14	PCS1 {USBSEL2}	Main board and module	USB CLK pinstrap	Pinstrap switch (**SW16**).
			186 local bus interface	Do not attach Am186 processor expansion interface expansion card.
			Module interface (79C32 chip select)	Do not attach module.
PIO15	WR {$\overline{\text{PRODTST}}$}	Main board	DRAM WR	PIO isolation switch (**SW4**).
PIO16	RXD_HU	Main board	High-Speed UART	High-Speed UART transceiver enable switch (**SW9**).
			USB data LED	PIO isolation switch (**SW4**).

Table B-1. PIO Usage (Continued)

PIO	Multiplexed Function(s)	Location	Usage	Isolation Method
PIO17	DCE_CTS_A[1] $\overline{\text{PCM\_TSC\_A}}$[1]	Module	RS422 port A	HDLC A transceiver enable switch (**SW9**).
			Module interface (DSLAC chip select)	Do not attach module.
PIO18	$\overline{\text{DCE\_RTR\_A}}$[1]	Module	RS422 port A	HDLC A transceiver enable switch (**SW9**).
			Module interface (LED ISDN B1-**CR4**)	Do not attach module.
PIO19	INT6	None	Am186 processor expansion interface	Do not attach Am186 processor expansion interface card.
			Module interface	Do not attach module.
PIO20	TXD_U DCE_TXD_D[2] PCM_TXD_D[2]	Main board	UART	UART transceiver enable switch (**SW9**).
			RS422 port D	HDLC D transceiver enable switch (**SW9**).
			Module interface	Do not attach module.
PIO21	UCLK USBSOF[3] USBSCI[3]	Main board	External UART clock	Remove UART clock oscillator (**Y4**).
PIO22	DCE_RCLK_C[2] PCM_CLK_C[2]	Module	RS422 port C	HDLC C transceiver enable switch (**SW9**).
			HDLC clock routing	HDLC clock routing jumper (**JP2**).
			Module interface (DSLAC clock)	Do not attach module.

Table B-1. PIO Usage (Continued)

PIO	Multiplexed Function(s)	Location	Usage	Isolation Method
PIO23	DCE_TCLK_C[2] PCM_FSC_C[2]	Module	RS422 port C	HDLC C transceiver enable switch (**SW9**).
			HDLC clock routing	HDLC clock routing jumper (**JP2**).
			Module interface (DSLAC FSC)	Do not attach module.
PIO24	CTSU DCE_TCLK_D[2] PCM_FSC_D[2]	Main board	UART	UART transceiver enable switch (**SW9**).
			RS422 port D	HDLC D transceiver enable switch (**SW9**).
			HDLC clock routing	HDLC clock routing jumper (**JP1**).
			Module interface	Do not attach module.
PIO25	RTR_U DCE_RCLK_D[2] PCM_CLK_D[2]	Main board	UART	LS UART transceiver enable switch (**SW9**).
			RS422 port D	HDLC D transceiver enable switch (**SW9**).
			HDLC clock routing	HDLC clock routing jumper (**JP1**).
			Module interface	Do not attach module.
PIO26	RXD_U DCE_RXD_D[2] PCM_RXD_D[2]	Main board	UART	UART transceiver enable switch (**SW9**).
			RS422 port D	HDLC D transceiver enable switch (**SW9**).
			Module interface	Do not attach module.

Table B-1. PIO Usage (Continued)

PIO	Multiplexed Function(s)	Location	Usage	Isolation Method
PIO27	TMRIN0	Main board	Optional $\overline{RI}$ hardware flow control for UART or High-Speed UART	Jumper block (**JP3** and **JP5**).
			Am186 processor expansion interface	Do not attach Am186 processor expansion interface card.
PIO28	TMROUT0	Main board	Optional $\overline{DSR}$ hardware flow control for UART or High-Speed UART	Jumper block (**JP3** and **JP5**).
			Am186 processor expansion interface	Do not attach Am186 processor expansion interface card.
PIO29	DT/$\overline{R}$	None	Am186 processor expansion interface	Do not attach Am186 processor expansion interface card.
			Module interface	Do not attach module.
PIO30	DEN DS	None	Am186 processor expansion interface	Do not attach Am186 processor expansion interface card.
			Module interface	Do not attach module.
PIO31	$\overline{PCS7}$	None	Am186 processor expansion interface	Do not attach Am186 processor expansion interface card.
			Module interface	Do not attach module.
PIO32	$\overline{PCS6}$	Module	Am186 processor expansion interface	Do not attach Am186 processor expansion interface card.
			Module interface (LED ISDN D-**CR6**)	Do not attach module.

Table B-1. PIO Usage (Continued)

PIO	Multiplexed Function(s)	Location	Usage	Isolation Method
PIO33	ALE	Main board	Am186 processor expansion interface	Do not attach Am186 processor expansion interface card.
			Module interface	Do not attach module.
PIO34	BHE {$\overline{\text{ADEN}}$}	Main board	Address enable pinstrap	Pinstrap switch (**SW14**).
PIO35	SRDY	None	Flash memory PIO banking	Jumper block (**JP8**).
			Am186 processor expansion interface	Do not attach Am186 processor expansion interface card.
			Module interface	Do not attach module.
PIO36	DCE_RXD_B[1] PCM_RXD_B[1]	Main board	RS422 port B	HDLC B transceiver enable switch (**SW9**).
			Module interface	Do not attach module.
PIO37	DCE_TXD_B[1] PCM_TXD_B[1]	Main board	RS422 port B	HDLC B transceiver enable switch (**SW9**).
			Module interface	Do not attach module.
PIO38	$\overline{\text{DCE\_CTS\_B}}$[1] $\overline{\text{PCM\_TSC\_B}}$[1]	Main board and module	RS422 port B	HDLC B transceiver enable switch (**SW9**).
			Module interface (T77256A SCLK control)	Do not attach module.
PIO39	DCE_RTR_B[1]	Main board and module	RS422 port B	HDLC B transceiver enable switch (**SW9**).
			Module interface (LED ISDN B2-**CR5**)	Do not attach module.

Table B-1. PIO Usage (Continued)

PIO	Multiplexed Function(s)	Location	Usage	Isolation Method
PIO40	DCE_RCLK_B[1] PCM_CLK_B[1]	Main board and module	RS422 port B	HDLC B transceiver enable switch (**SW9**).
			HDLC clock routing	HDLC clock routing jumper.
			Module interface (POTS Ring 1)	Do not attach module.
PIO41	DCE_TCLK_B[1] PCM_FSC_B[1]	Main board and module	RS422 port B	HDLC B transceiver enable switch (**SW9**).
			HDLC clock routing	HDLC clock routing jumper.
			Module interface (POTS ring 2)	Do not attach module.
PIO42	DCE_RXD_C[2] PCM_RXD_C[2]	Main board	USB V_{CC} detect	PIO isolation switch (**SW2**).
			RS422 port C	HDLC C transceiver enable switch (**SW8**).
			Module interface	Do not attach module.
PIO43	DCE_TXD_C[2] PCM_TXD_C[2]	Main board	USB LDO enable	PIO isolation switch (**SW4**).
			RS422 port C	HDLC C transceiver enable switch (**SW9**).
			Module interface	Do not attach module.
PIO44	$\overline{\text{DCE\_CTS\_C}}$[2] $\overline{\text{PCM\_TSC\_C}}$[2]	Main board	Optional hardware flow control for High-Speed UART	HDLC C transceiver enable switch (**SW9**).
			Module interface	Do not attach module.
PIO45	DCE_RTR_C[2]	Main board	Optional hardware flow control for High-Speed UART	HDLC C transceiver enable switch (**SW9**).
			Module interface	Do not attach module.

Table B-1. PIO Usage (Continued)

PIO	Multiplexed Function(s)	Location	Usage	Isolation Method
PIO46	CTS_HU $\overline{\text{DCE\_CTS\_D}}$[2] $\overline{\text{PCM\_TSC\_D}}$[2]	Main board	RS422 port D	HDLC D transceiver enable switch (**SW9**).
			High-Speed UART	High-Speed UART transceiver enable switch (**SW9**).
			Module interface	Do not attach module.
PIO47	RTR_HU $\overline{\text{DCE\_RTR\_D}}$[2]	Main board	RS422 port D	HDLC D transceiver enable switch (**SW8**).
			High-Speed UART	High-Speed UART transceiver enable switch (**SW8**).
			Module interface	Do not attach module.

1. Am186CC and Am186CH microcontrollers only.
2. Am186CC communications controller only.
3. Am186CC and Am186CU microcontrollers only.

Table B-2. Chip Select Usage

Chip Select	Multiplexed Function	Location	Usage
$\overline{\text{LCS}}$	$\overline{\text{RAS0}}$	Main board	DRAM lower bank $\overline{\text{RAS}}$
$\overline{\text{MCS0}}$	PIO4{UCSX8}	Main board	SRAM alternate chip select
$\overline{\text{MCS1}}$	$\overline{\text{CAS1}}$	Main board	DRAM upper $\overline{\text{CAS}}$
$\overline{\text{MCS2}}$	$\overline{\text{CAS0}}$	Main board	DRAM lower $\overline{\text{CAS}}$
$\overline{\text{MCS3}}$	$\overline{\text{RAS1}}$/PIO5	Main board	DRAM upper bank $\overline{\text{RAS}}$
$\overline{\text{PCS0}}$	PIO13{USBSEL1}[1]	None	Not used
$\overline{\text{PCS1}}$	PIO14{USBSEL2}[1]	Module	79C32 chip select
$\overline{\text{PCS2}}$	—	Module	PCnet-ISA chip select
$\overline{\text{PCS3}}$	—	TIP	Ethernet controller chip select
$\overline{\text{PCS4}}$	PIO3{CLKSEL2}	Module	DTMF 1 output enable
$\overline{\text{PCS5}}$	PIO2	Module	DTMF 2 output enable
$\overline{\text{PCS6}}$	PIO32	Module	ISDN D LED PIO
$\overline{\text{PCS7}}$	PIO31	—	
$\overline{\text{UCS}}$	{ONCE}	Main board	Flash memory chip select

1. Am186CC and Am186CU microcontrollers only.

Table B-3. Platform Interrupts Pin Usage

Interrupt	Multiplexed Function(s)	Location	Usage	Polarity
INT0	—	TIP	TIP Ethernet controller	Active High edge
INT2	—	Module	T7256A	Active Low edge
INT3	—	Module	PCnet-ISA	Active High edge
INT4	—	Module	DTMF 1	Active High edge
INT5	—	Module	DTMF 2	Active High edge
INT6	—	Module	Am79C32	Active Low edge
INT6	PIO19	TIP	Parallel port	Active High edge
INT7	PIO7	TIP	Serial 1	Active High edge
INT8	PIO6/PWD	TIP	Serial 0	Active High edge

Appendix C

Main Board Bill of Materials

This appendix provides the Am186CC/CH/CU microcontroller customer development platform bill of materials.

Table C-1. Main Board Bill of Materials

Item	Qty	Reference	Part	Package	Part Spec.
1	7	CR1,CR2,CR3,CR4, CR5,CR6,CR7	LED SOT-23	SOT-23	LUMEX SSL-LX15IGC-RP-TR
2	5	CR8,CR9,CR10, CR11,CR12	LED SMT	SMT-2	LUMEX CCL-CRS10R
3	55	C1,C2,C3,C4,C5,C6, C7,C8,C9,C10,C13, C14,C15,C16,C17, C18,C20,C21,C26, C27,C28,C29,C33, C34,C39,C41,C43, C49,C54,C64,C65, C78,C79,C81,C85, C87,C89,C90,C93, C94,C95,C96,C97, C98,C99,C100, C104,C106,C107, C108,C109,C110, C111,C112,C113, C116, C117	0.1µF	805	+/- 10%, X7R, 50 V
4	12	C11,C12,C22,C23, C24,C31,C32,C36, C53,C55,C63,C71	10µF	C-CASE	Tantalum, C CASE, 16 V
5	1	C19	1.0µF	A-CASE	Tantalum, A CASE, 16 V
6	2	C25,C37	1000pF	805	+/- 10%, X7R, 50 V
7	4	C30,C38,C51,C69	0.01µF	805	+/- 10%, X7R, 50 V

Table C-1. Main Board Bill of Materials (Continued)

Item	Qty	Reference	Part	Package	Part Spec.
8	1	C35	4.7µF	C-CASE	Tantalum, C CASE, 16 V
9	8	C40,C42,C44,C45, C101,C102,C103, C105	22pF	805	+/- 10%, X7R, 50 V
10	6	C46,C47,C56,C57, C58,C70	22µF	E-CASE	AVX TPSE226M035R0300
11	1	C48	220pF	805	AVX 08055C221MATMA
12	1	C50	0.22µF	1206	AVX 12063C224MATMA
13	1	C52	3300pF	1206	AVX 12065C104MATMA
14	2	C59,C60	10µF	1812	+/- 10%, Y5V, 25 V
15	5	C61,C62,C66,C67, C68	330µF	E-CASE	AVX TPSE337M010#100
16	16	C72,C73,C74,C75, C76,C77,C80,C82, C83,C84,C86,C88, C91,C92,C114,C115	220pF	805	+/- 10%, X7R, 50 V
17	1	D1	Diode	SOT-23	ROHM RB400D
18	1	D2	Diode ZENER	SOT-23	ROHM RSZ5228B
19	1	D3	Diode ZENER	DO-214AA	General Semi SMZJ3797B
20	4	D4,D5,D6,D7	Diode	DO-214AA	General Semi ES2D
21	1	D8	Diode	SMA	ROHM RB160L-40
22	1	D9	Schottky Rectifier	SMT-2	International Rectifier 30BQ015
23	3	FB1,FB2,FB4	FB	1206	MURATA BLM31P500SPB
24	2	FB5,FB6	FB	805	MURATA BLM21A121SPB
25	1	F1	2.5A	SMT-2	Bussmann 3216FF-2.5A

Table C-1. Main Board Bill of Materials (Continued)

Item	Qty	Reference	Part	Package	Part Spec.
26	6	GP1,GP2,GP3,GP4, GP5,GP6	GND PT	TH-1	AMP 87224-1
27	7	JP1,JP2,JP3,JP4,JP5, JP6,JP7	Header 4x2	TH-2x4	AMP 103186-4
28	2	JP8,JP9	Header 2x2	TH-2x2	AMP 103186-2
29	1	JP10	Header 3x2	TH-2x3	AMP 103186-3
30	2	JP11,JP12	Header 6x2	TH-2x6	AMP 103186-6
31	1	L1	10µH	SMT	Coiltronics CTX10-2-52
32	1	L2	33µH	SMT-2	Coiltronics UP2B-330
33	4	P1,P2,P3,P4	Connector DB25	TH-25	AMP 787202-1
34	2	P6,P5	Header 5x2	TH-2x5-SHRD	AMP 111949-1
35	2	P15,P7	Connector DB9	TH-9	AMP 787200-1
36	2	P11,P8	DAQ Connector	TH-2x25-SHRD	AMP 1-111949-0
37	8	P9,P10,P13,P14,P16, P17,P20,P21	HP Connector	TH-2x10 SHRD	AMP 103308-5
38	2	P19,P12	COND70	SMT-2x35	AMP 104652-7
39	1	P18	USB Connector	TH-4	AMP 787780-1
40	3	P22,P23,P24	Banana Jack	TH-1	Johnson 105-0851-001
41	2	P25,P28	Banana Jack	TH-1	Johnson 105-0852-001
42	1	P26	Header 32x2	TH-2x32	AMP 3-103186-2
43	1	P27	Header 20x2	TH-2x20	AMP 2-103186-0
44	1	P29	Banana Jack	TH-1	Johnson 105-0853-001
45	1	P30	COND60	SMT-2x30	AMP 104069-7
46	1	P31	Barrel Connector	TH-3	KYCON KLD-0202-BC
47	2	Q2,Q1	TN0200T	SOT-23	Temic TN0200T

Table C-1. Main Board Bill of Materials (Continued)

Item	Qty	Reference	Part	Package	Part Spec.
48	16	R1,R3,R5,R7,R9, R11,R13,R15,R24, R57,R120,R145, R152,R173,R180, R245	100K	805	+/- 5%, 1/10W
49	12	R2,R4,R6,R8,R10, R12,R14,R16,R25, R26,R31,R32	220	805	+/- 5%, 1/10W
50	13	R17,R19,R20,R21,R2 3,R27,R29,R30,R34, R35,R36,R37,R45	47	603	+/- 5%, 1/16W
51	51	R22,R91,R119,R121, R123,R125,R127, R133,R134,R136, R137,R140,R141, R142,R146R149, R154,R156,R159, R164,R172,R175, R176,R179,R181, R182,R186,R187, R201,R202,R207, R208,R213,R214, R246,R248,R249, R255,R257,R258, R259,R260,R264, R267,R269,R271, R278,R280,R282, R288,R291,R295	10K	805	+/- 5%, 1/10W
52	20	R28,R102,R143, R147,R150,R157, R160,R161,R165, R188,R203,R209, R215,R266,R268, R270,R281,R287, R290,R293	1K	805	+/- 5%, 1/10W

Table C-1. Main Board Bill of Materials (Continued)

Item	Qty	Reference	Part	Package	Part Spec.
53	109	R33,R44,R46,R47, R48,R51,R52,R53, R54,R59,R60,R61, R62,R63,R64,R65, R66,R67R68,R69, R70,R71,R72,R73, R74,R75,R76,R77, R79,R80,R81,R82, R83,R84,R85,R86, R87,R88,R138,R158, R162,R163,R166, R168,R169,R170, R171,R174,R177, R178,R183,R184, R185,R189,R190, R191,R192,R193, R194,R195,R196, R197,R198,R199, R200,R204,R205, R206,R212,R216, R217,R218,R219, R220,R221,R222, R223,R224,R225, R226,R227,R228, R229,R230,R231, R235,R236,R237, R238,R239,R240, R241,R242,R250, R251,R252,R253, R254,R261,R262, R263,R272,R273, R274,R275,R276, R284,R285,R286	22	603	"+/- 5%, 1/16W"
54	2	R40,R38	33	603	+/- 5%, 1/16W
55	2	R155,R41	15	603	+/- 5%, 1/16W

Table C-1. Main Board Bill of Materials (Continued)

Item	Qty	Reference	Part	Package	Part Spec.
56	16	R49,R50,R89,R92, R210,R211,R232, R233,R234,R268, R277,R283,R289, R292,R294,R298	0	805	+/- 5%, 1/10W
57	16	R58	1.5K	805	+/- 5%, 1/10W
58	1	R78	56	603	+/- 5%, 1/16W
59	1	R94	3.32K	1206	+/- 1%, 1/4W, 150 V
60	1	R95	487	1206	+/- 1%, 1/4W, 150 V
61	1	R96	10K	1206	+/- 5%, 1/4W, 150 V
62	3	R97,R100,R101	0	1206	KOA RM73Z2B, 5%, 1W
63	2	R98,R99	13.7K	1206	+/- 1%, 1/4W, 150 V
64	17	R103,R104,R105, R106,R107,R108, R109,R110,R111, R112,R113,R114, R115,R116,R117, R118,R167	100	805	+/- 5%, 1/10W
65	16	R122,R124,R126, R128,R129,R130, R131,R132,R135, R139,R144,R148, R151,R153,R296			
66	1	R243	3.9K	2512	KOA RM73B3A, 5%, 1W
67	1	R244	1.5K	2512	KOA RM73B3A, 5%, 1W
68	2	R247,R265	220	1206	+/- 5%, 1/4W, 150 V
69	1	R256	68	1206	+/- 5%, 1/4W, 150 V
70	1	SW1	RESET	SMT-4	C+K KT11P2SM
71	2	SW2,SW11	SW DPDT	TH-6	Grayhill 76SD01
72	4	SW3,SW5,SW6,SW7	DIP 3PST	DIP-6	Grayhill 78G01
73	1	SW4	DIP 4PST DUAL	DIP-16	Grayhill 78H02
74	5	SW8,SW10,SW12, SW14,SW16	SW DIP-4	TH-8	C+K BD04

Table C-1. Main Board Bill of Materials (Continued)

Item	Qty	Reference	Part	Package	Part Spec.
75	3	SW9,SW13,SW15	SW DIP-8	TH-16	C+K BD08
76	3	TP1,TP2,TP3	TESTPT	SMT-1	805 Single Pin
77	1	T1	Flyback Transformer	SMT	Beckman HM00-98519
78	4	U1,U4,U7,U10	DS34C87T SOP	SOP-16	National DS34C87TM
79	4	U2,U3,U8,U9	DS34C86T SOP	SOP-16	National DS34C86TM
80	2	U6,U5	74ACT125	SOIC-14	74ACT125
81	1	U11	M4-128/ 64YC	PQFP-100	Vantis M4-128/64-15YC
82	1	U12	SP2007B	SOIC-28	Sipex SP207BCT
83	1	U13	TLC7733ID	SOIC-8	TI TLC7733ID
84	1	U14	74ACT02	SOIC-14	74ACT02
85	1	U16	Am186CC microcontroller	PQFP-160	
86	1	U17	SP207HB	SOIC-28	Sipex SP207HBCT
87	1	U19	AM29F800 TSOP	TSOP-48	AM29F800BT-55EC
88	1	U20	USB XCVR	SSOP-14	Philips PDIUSBP11DB
89	1	U21	DRAM 256x16 SOJ	SOJ-40	Mosel Vitelic V53C16258HK40
90	1	U22	74ACT04	SOIC-14	74ACT04
91	1	U23	OP Amp	SOT-23-5	Micrel MIC6211BM5
92	1	U24	SLIC Regulator	TO-263	Micrel MIC2171BU
93	2	U25,U28	SRAM	DIP-32	Samsung KM681000CLP-4
94	1	U26	M5V Regulator	TO-263-5	Micrel MIC4575-5.0BU
95	1	U27	MIC4576	TO-263-5	Micrel MIC4576-5.0BT
96	1	U29	LDO-3.3	SOT-223	Micrel MIC5209-3.3BS
97	1	U36	74AC126	SOIC-14	74AC126
98	1	X1	Crystal TH-2	TH-2	Ecliptek EC2-20.000M-CL150

Table C-1. Main Board Bill of Materials (Continued)

Item	Qty	Reference	Part	Package	Part Spec.
99	1	X2	Crystal TH-2	TH-2	Ecliptek EC2-24.000M-CL150
100	1	Y1	OSC4p	SMT-4	Ecliptek EC23-16.384M
101	1	Y2	OSC4p	SMT-4	Ecliptek EC23-20.000M
Miscellaneous Parts					
1	1	SU16	Socket PQFP-160	PQFP-160	YAMAICHI IC149-160-023-S5
2	12	SY5,SY4,SY3	Pin Sockets (4 PER SU)	TH-1	MCKENZIE 185B
3	2	SU28,SU25	Socket DIP-32	DIP-32	AMP 3-382568-2
4	4	SX1,SX2	Pin Sockets (2 PER SU)	TH-1	MCKENZIE 185B
5	18		Berg Jumpers		Open top Berg jumpers
Unpopulated Parts					
1	1	FB3	FB[1]	1206	MURATA BLM31P500SPB
2	6	R42,R43,R55,R56, R93,R279	0[1]	805	+/- 5%, 1/10W
3	1	R90	10K[1]	805	+/- 5%, 1/10W
4	1	SP1	SPARE14[1]	SOIC-14	
5	1	SP2	SPARE20[1]	SOIC-20	
6	1	U15	SRAM 256Kx16 SOJ[1]	SOJ-44	Cypress 7C1041-25VC
7	1	U18	DRAM 256X16 SOJ[1]	SOJ-40	Mosel Vitelic V53C16258HK40
8	1	U20	USB XCVR[1]		
9	3	Y3,Y4,Y5	OSC4p[1]	TH-4	Ecliptek EC1300HS-XX

Table C-1. Main Board Bill of Materials (Continued)

Item	Qty	Reference	Part	Package	Part Spec.
Kit Parts					
1	1		12-V 2.5 A Power Supply		Spectre PS-1225-AP6
2	1		2 Meter USB Cable		Newnex UF2-2002
3	1		RS-232 Cable		Same as 186xx
4	1		6 ft. Male-to Female DB-25 RS-530 Cable		AMP 621796-3

1. Not required for standard kit.

Appendix D

Development Module Bill of Materials

This appendix contains the Am186CC/CH/CU microcontroller customer development platform development module bill of materials.

Table D-1. Router/ISDN Development Module Bill of Materials

Item	Qty	Reference	Part	Package	Part Spec.
1	4	CBX1,CAX1, CBX2,CAX2	4700pF	805	+/- 10%, X7R, 100 V
2	2	CDCR_2,CDCR_1	0.022µF	805	+/- 10%, X7R, 100 V
3	2	CDC_2,CDC_1	0.56µF	1825	+/- 10%, X7R, 100 V
4	2	CHP2,CHP1	0.047µF	1206	+/- 10%, X7R, 100 V
5	2	CRT2,CRT1	1.0µF	2225	+/- 10%, X7R, 100 V
6	7	CR1,CR2,CR3, CR4,CR5,CR6, CR7	LED SOT-23	SOT-23	Lumex SSL-LX15IGC-RP-TR
7	2	CSLEW2, CSLEW1	0.33µF	805	+/- 10%, X7R, 50 V
8	2	CT2,CT1	100pF	805	+/- 10%, X7R, 100 V

Table D-1. Router/ISDN Development Module Bill of Materials (Continued)

Item	Qty	Reference	Part	Package	Part Spec.
9	42	C1,C4,C6,C9,C13, C14,C15,C20,C21, C22,C24,C26,C28, C32,C38,C41,C42, C46,C49,C50,C51, C52,C53,C55,C56, C57,C58,C59,C60, C61,C62,C63,C64, C65,C66,C67,C68, C69,C70,C71,C72, C73	0.1µF	805	+/- 10%, X7R, 100 V
10	4	C2,C3,C29,C30	27pF	805	+/- 10%, COG, 50 V
11	2	C5,C16	22µF	C-CASE	Tantalum, C CASE, 16 V
12	1	C7	10µF	TH-2	Nichicon UVR2A100MEA
13	1	C8	10µF	TH-2	Nichicon UVR1H100MDA
14	4	C10,C11,C12,C17	10µF	C-CASE	Tantalum, C CASE, 16 V
15	2	C27,C19	680pF	805	+/- 10%, X7R, 50 V
16	7	C33,C34,C35,C39, C40,C47,C48	0.01µF	805	+/- 10%, X7R, 50 V
17	1	C36	1.0µF	TH-2	Philips 2222 370 75105
18	1	C37	820pF	805	Kemet C0805C821J5GAC
19	2	C43,C44	3300pF	1206	Kemet C1206C332F5RAC
20	1	C45	1.0µF	TH-2	Philips 2222 373 41105, or Vitramon VJ9253Y105KXPM

Table D-1. Router/ISDN Development Module Bill of Materials (Continued)

Item	Qty	Reference	Part	Package	Part Spec.
21	1	C54	30pF	805	+/- 10%, COG, 50 V
22	4	C74,C75,C76,C77	1000pF	603	+/- 10%, X7R, 16 V
23	4	D1,D2,D4,D5	Diode BAV70A	SOT-23	Philips BAV70A
24	2	D3,D6	Diode ZENER	SOT-23	ROHM RSZ5234B
25	2	FR1,FR2	Fuse Resistor	TH-6	Microelectronic Modules Corp. L11A050AA
26	1	F1	Fuse	TH-2	Raychem TR600-150
27	1	GP1	Ground PostT	TH-1	AMP 87224-1
28	1	JP2	Header 3x2	TH-6	AMP 103186-3
29	1	JP3	Header 6x2	TH-2x6	AMP 103186-6
30	3	P1,P2,P3	RJ45A	TH-12	AMP 555153-1
31	2	P4,P5	RJ11	TH-10	AMP 555154-2
32	1	P6	Connector DB25	TH-25	AMP 787202-1
33	2	P7,P8	COND70	SMT-2x35	AMP 104693-7
34	4	RDCR1_1, RDCR1_2, RDCR2_1, RDCR2_2	20.0K	805	+/- 1%, 1/10W
35	6	RSGH1,RSGH2, RDC1_1,RDC1_2, RDC2_1,RDC2_2	56.2K	805	+/- 1%, 1/10W
36	2	RD2,RD1	22.1K	805	+/- 1%, 1/10W
37	2	RRT1_2,RRT1_1	511K	805	+/- 1%, 1/10W
38	2	RRT2_2,RRT2_1	12.1K	805	+/- 1%, 1/10W
39	2	RRX_2,RRX_1	200K	805	+/- 1%, 1/10W

Table D-1. Router/ISDN Development Module Bill of Materials (Continued)

Item	Qty	Reference	Part	Package	Part Spec.
40	2	RSLEW2, RSLEW1	150K	805	+/- 1%, 1/10W
41	4	RT1B1,RT1A1,RT 2B1,RT2A1	124K	805	+/- 1%, 1/10W
42	27	R1,R2,R3,R4,R8, R9,R10,R13,R14, R15,R16,R17,R18, R19,R21,R22,R23, R24,R25,R27,R28, R58,R67,R70,R77, R83,R86	10K	805	+/- 5%, 1/10W
43	3	R5,R6,R7	270	805	+/- 5%, 1/10W
44	2	R11,R38	1K	805	+/- 5%, 1/10W
45	1	R12	5	1206	+/- 5%, 1/8W
46	6	R20,R26,R62,R63, R73,R74	100K	805	+/- 1%, 1/10W
47	2	R30,R46	100	1206	+/- 1%, 1/8W
48	2	R31,R34	2K	1206	+/- 5%, 1/4W
49	2	R35,R33	3.6K	1206	+/- 5%, 1/4W
50	4	R37,R40,R42,R48	22.6	1210	+/- 1%, 1/2W
51	3	R43,R44,R45	68	805	+/- 5%, 1/10W
52	2	R60,R47	1.1K	SMT-2	Dale WSC-2
53	1	R51	820	805	+/- 5%, 1/10W
54	2	R53,R52	137	1206	Dale CRCW12061370F
55	1	R54	17.8K	1206	Dale CRCW12061783F
56	1	R55	21	1206	+/- 1%, 1/10W

Table D-1. Router/ISDN Development Module Bill of Materials (Continued)

Item	Qty	Reference	Part	Package	Part Spec.
57	1	R56	2.2M	1206	Dale CRCW1206225J
58	1	R57	10K	1206	Dale CRCW1206103J
59	2	R61,R59	16.9	1206	Dale CRCW120616R9FF
60	2	R75,R64	300K	805	+/- 1%, 1/10W
61	2	R71,R85	0	805	+/- 5%, 1/10W
62	1	SW1	SW DPDT	TH-6	Grayhill 76SD01
63	3	U1,U6,U7	74ACT16245	TSSOP-48	TI 74ACT16245DGG
64	1	U2	Serial EPROM DIP	DIP-8	National NM93C56N
65	1	U3	64Kx16 SRAM	TSOP II-44	Samsung KM6161000BLT-5L
66	1	U4	Am79C961A	PQFP-132	Am79C961A KC
67	1	U5	LAN Transformer	SMT-16	Pulse E2003
68	1	U8	AM79C32A PLCC	PLCC-44	Am79C32A JC
69	2	U9,U10	LC03-6	SO-8	Semtech LC03-6
70	1	U11	S Transformer	SMT-16	Pulse PE-65799
71	1	U12	PE65554	TH-8	Pulse PE65554
72	3	U13,U20,U24	PAL22V10 PLCC-28	PLCC-28	Vantis PAL22V10H-5JC
73	1	U14	T7256A PLCC	PLCC-44	Lucent T7256A- -ML-DT
74	1	U15	6N139	DIP-8	Siemens 6N139

Table D-1. Router/ISDN Development Module Bill of Materials (Continued)

Item	Qty	Reference	Part	Package	Part Spec.
75	1	U16	SM6T6V8CA	SMB	SGS-Thomson SM6T6V8CA
76	1	U17	U Transformer	TH-10	Pulse T4008
77	1	U18	LH1465AB	DIP-8	Lucent LH1465AB
78	1	U19	P2300SB	DO-214	Teccor P2300SB, or SGS-Thomson SMP100-200
79	2	U28,U21	DTMF M-8870-01	SOIC-18	Teltone M-8870-01SM
80	2	U22,U26	Am79R79	PLCC-32	Am79R79-1JC
81	2	U23,U27	TISP61089	SOIC-8	Power Innovations TISP61089
82	1	U25	Am79C031	PLCC-32	Am79C031JC
83	1	X1	20.000MHz	HC-49	Ecliptek EC-20.000M-ITR
84	1	X2	12.228MHz	HC-49	Ecliptek EC-12.228M-ITR
85	1	X3	15.36011MHz	HC-49	Saronix SRX5144
86	1	X4	3.58MHz	HC-49	Ecliptek EC2-3.579545M-ITR

Table D-1. Router/ISDN Development Module Bill of Materials (Continued)

Item	Qty	Reference	Part	Package	Part Spec.
Unpopulated Parts					
1	4	C18,C23,C25,C31	0.068µF	1206	+/-10%, X7R, 50 V
2	12	RSGL_1,RSGL_2, R49,R72,R76,R78, R79,R80,R82,R84, R72	0	805	+/- 5%, 1/10W
3	2	R29,R36	121	1210	+/-1%, 1/4W
4	2	R32,R41	309	1210	+/- 1, 1/4W
5	2	R39,R50	10K	1210	+/-1%, 1/4W
6	1	R81	10K	805	+/- 5%, 1/10W
7	1	SP1	SPARE14	SOIC-14	
Miscellaneous Parts					
1	3	SU13,SU20,SU24	PLCC-28 Socket	SMT-28	SMT PLCC-28 Socket
2	1	SU2	DIP-8 Socket	DIP-8	DIP-8
Kit Parts					
1	1				6-Ft. RJ11 Phone Cord
2	2				6-Ft RJ45 CAT5 Cable

Appendix E

PLD Equations

This appendix contains a listing of PLD equations for the PLDs located at U13, U20, and U24 on the Am186CC/CH/CU microcontroller CDP.

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PLD (U13) Equations

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""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""
" U13 PLD code for the Am186CC CDP Development Module Revision 2.1               "
" An AMD PLCC-28 PAL22V10 provides glue logic needed between the Am186CC and the"
" PCNETISAII ethernet controller and ISDN devices.                              "          "
"                                                                                "
"   Written:   Oct. 1998                                                                    "
"    For  :    Advanced Micro Devices - Austin EPD                               "
"    By   :    LDB - System Engineering                                          "
"   Revision 00              10/98        Original Code                           "
"                            11/98        Added DTMF data buffer direction support "
"                            01/99        Added more defined data buffer control  "
""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""
"
"                                      Declarations                                       "
""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""""

INPUT     clkout;                         "PIN 2:  Am186CC CLKOUT
INPUT     /master;                        "PIN 3:  Am79C961A active low MASTER# output
INPUT     resout;                         "PIN 4:  Am186CC Active High Reset output
INPUT     /brd;                           "PIN 6: Am186CC or Am79C961A Active low RD# signal
INPUT     /bwr;                           "PIN 10: Am186CC or Am79C961A Active low WR#
                                          "signal
INPUT     hlda;                           "PIN 7:  Am186CC Active high Hold Acknowledge
INPUT     /pio38;                         "PIN 11: Am186CC Active low PIO38
INPUT     sclk;                           "PIN 12: Am186CC SSI Clock
INPUT     /pcs1;                          "PIN 13: Am186CC Active low PCS1# output
INPUT     /pcs2;                          "PIN 16: Am186CC Active low PCS2# output
INPUT     /pcs4;                          "PIN 5: Am186CC active low chip select

INPUT     /pcs5;                          "PIN 9: Am186CC active low chip select

INPUT     /main;                          "PIN 20: Selects location of packet SRAM (main or
                                          "module)

BIPUT     /bhe ENABLED_BY /master;        "PIN 21: Am186CC Active low BHE# output
BIPUT     /sbhe ENABLED_BY /master;       "PIN 18: Am79C961A Active low SBHE# output
BIPUT     /sramcs ENABLED_BY master;      "PIN 24: Packet SRAM Chip Select
OUTPUT    /reset;                         "PIN 27: Active low RESET used for the U transceiver
OUTPUT    /bhlda;                         "PIN 23: Active low DACK# used for the Am79C961A
OUTPUT    bsclk ENABLED_BY pio38;         "PIN 19: SSI clock used for the U transceiver
OUTPUT    /dbufdir;                       "PIN 17: Active low direction control for the buffers
OUTPUT    /dbufg                          "PIN 25: Active low Gate enable for data buffer

NODE      /dbhe CLOCKED_BY clkout;        "Internal node used to delay SBHE# by a 1/2 clock
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PLD (U13) Equations (continued)

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        “                    Equations                                   “

        ““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““

reset    =  resout;                                “Inverted RESOUT driven to a 5V level for the
                                                   “T7256A (U transceiver)

bhlda    =  hlda + master;                         “Inverted Am186CC HLDA to the Am79C961A
                                                   “DACK# that is latched to the end of the cycle

bsclk    = sclk;                                   “SCLK is transmitted to T7256 U transceiver only
                                                   “when PIO38 is LOW

dbufg    = [pcs1 + pcs2 + pcs4 + pcs5]             “Data buffer is enabled only when data is being
         + [master * sramcs * main]                “transferred between the CDP main and module
         +[/master * sramcs * /main];

dbufdir  = [master * bwr]                          “PCNETISA has bus:Point DATA buffer toward
         + /master * brd;                          “main on writes. Am186CC has bus: Point DATA
                                                   “buffer toward main on reads

sramcs   = 1;                                      “SRAMCS is three-state when Am186CC has the
                                                   bus “and active when Am79C961A has the bus

bhe      = sbhe;                                   “BHE# is three-stated when the Am186CC is
                                                   “master and the Am79C961A SBHE# output when
                                                   “it is master

sbhe     = bhe + dbhe;                             “SBHE# is the Am186CC BHE# extended by 1/2
                                                   “clock to remain active after the deassertion of RD#
                                                   “or WR# to adhere to the ISA spec.

dbhe     = bhe;                                    “Internal node used to delay BHE# by 1/2
                                                   “CLKOUT
```

PLD (U20) Equations (SBP/PCM Mode)

```
““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““
“  U20 PLD code for the Am186CC CDP Development Module Revision 2.1                    “
“  An AMD PLCC-28 PAL22V10 provides synchronization of clocks between the Am79C031 DSLAC “
“  and the Am79C32A when running in SBP/PCM mode.                                       “
“  Written:   Feb. 1999                                                                   “
“   For  :    Advanced Micro Devices - Austin EPD                                         “
“   By   :    LDB - System Engineering                                                    “
“                                                                                         “
“  Revision 00              2/99             Original Code                               “
““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““
“                                    Declarations                  “
““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““

INPUT      mclk_c32;                    “PIN 2:  Am79C32A 12.288 MHz MCLK output
INPUT      bclk_c32;                    “PIN 3:  Am79C32A BCLK output
INPUT      resout;                      “PIN 4:  Am186CC Active High Reset output
INPUT      pclk_c32                     “PIN 5: CLKA output from the Am79C32A

OUTPUT     mclk4;                       “PIN 18: 4.096 MHz Am79C031 MCLK input
OUTPUT     pclk;                        “PIN 25: modified BCLK signal
```

PLD (U20) Equations (continued)

```
““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““
“
“                                   Equations                                   “
““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““
STATE_MACHINE divider CLOCKED_BY mclk_c32 RESET_BY resout;

“ This state machine generates 4.096MHz clock signal for the DSLAC.

STATE one:
    mclk4=0;
    goto two;
STATE two:
    mclk4=0;
    goto three;
STATE three:
    mclk4=1;
    goto one;
END divider;
STATE_MACHINE DPLL CLOCKED_BY mclk_c32 RESET_BY resout;

“ Jitter reduction circuit, implemented as free running up-counter, that counts 15, 16 or 17
“ clock cycles to form a window.  The entire circuit can be viewed as a DPLL

STATE one:
    pclk=1;                 “ set the PCLK output to one
    goto two;               “ on the next rising edge of the CLK signal go to the next
                            “state !
STATE two:
    pclk=1;
    goto three;
STATE three:
    pclk=1;
    goto four;
STATE four:
    pclk=1;
    goto five;
STATE five:
    pclk=1;
    goto six;
```

PLD (U20) Equations (continued)

```
STATE six:
    pclk=1;
    goto seven;
STATE seven:
    pclk=1;
    goto eight;
STATE eight:
    pclk=1;
    goto nine;
STATE nine:
    pclk=1;
    goto ten;
STATE ten:
    pclk=1;
    goto eleven;
STATE eleven:
    pclk=1;
    goto twelve;
STATE twelve:
    pclk=1;
    goto thirteen;
STATE thirteen:
    pclk=1;
    goto fourteen;
STATE fourteen:
    pclk=1;
    goto fifteen;
STATE fifteen:
    pclk=1;
    goto sixteen;
STATE sixteen:
    pclk=1;
    goto seventeen;
```

PLD (U20) Equations (continued)

```
STATE seventeen:
    pclk=0;
    goto eighteen;
STATE eighteen:
    pclk=0;
    goto nineteen;

STATE nineteen:
    pclk=0;
    goto twenty;
STATE twenty:
    pclk=0;
    goto twentyone;

STATE twentyone:
    pclk=0;
    goto twentytwo;
STATE twentytwo:
    pclk=0;
    goto twentythree;

STATE twentythree:
    pclk=0;
    goto twentyfour;
STATE twentyfour:
    pclk=0;
    goto twentyfive;

STATE twentyfive:
    pclk=0;
    goto twentysix;
STATE twentysix:
    pclk=0;
    goto twentyseven;
```

PLD (U20) Equations (continued)

```
STATE twentyseven:
    pclk=0;
    goto twentyeight;
STATE twentyeight:
    pclk=0;
    goto twentynine;

STATE twentynine:
    pclk=0;
    goto thirty;
STATE thirty:
    pclk=0;
    goto thirtyone;

STATE thirtyone:
    pclk=0;
    goto thirtytwo;
STATE thirtytwo:
    pclk=0;
    goto thirtythree;

STATE thirtythree:
    pclk=0;
    goto thirtyfour;
STATE thirtyfour:
    pclk=0;
    goto thirtyfive;

STATE thirtyfive:
    pclk=0;
    goto thirtysix;
STATE thirtysix:
    pclk=0;
    goto thirtyseven;
```

PLD (U20) Equations (continued)

```
STATE thirtyseven:
    pclk=0;
    goto thirtyeight;
STATE thirtyeight:
    pclk=0;
    goto thirtynine;

STATE thirtynine:
    pclk=0;
    goto forty;
STATE forty:
    pclk=0;
    goto fortyone;

STATE fortyone:
    pclk=0;
    goto fortytwo;
STATE fortytwo:
    pclk=0;
    goto fortythree;

STATE fortythree:
    pclk=0;
    goto fortyfour;
STATE fortyfour:
    pclk=0;
    goto fortyfive;

STATE fortyfive:
    pclk=0;
    goto fortysix;
STATE fortysix:
    pclk=0;
    goto fortyseven;
```

PLD (U20) Equations (continued)

```
STATE fortyseven:
    pclk=0;
    goto fortyeight;
STATE fortyeight:
    pclk=0;
    goto fortynine;

STATE fortynine:
    pclk=0;
    goto fifty;
STATE fifty:
    pclk=0;
    goto fiftyone;

STATE fiftyone:
    pclk=0;
    goto fiftytwo;
STATE fiftytwo:
    pclk=0;
    goto fiftythree;

STATE fiftythree:
    pclk=0;
    goto fiftyfour;
STATE fiftyfour:
    pclk=0;
    goto fiftyfive;

STATE fiftyfive:
    pclk=0;
    goto fiftysix;
STATE fiftysix:
    pclk=0;
    goto fiftyseven;
```

PLD (U20) Equations (continued)

```
STATE fiftyseven:
    pclk=0;
    goto fiftyeight;
STATE fiftyeight:
    pclk=0;
    goto fiftynine;
STATE fiftynine:
    pclk=0;
    goto sixty;
STATE sixty:
    pclk=0;
    goto sixtyone;
STATE sixtyone:
    pclk=0;
    goto sixtytwo;
STATE sixtytwo:
    pclk=0;
    goto sixtythree;

" States 63 to 65 form a window to catch the PCLK signal

STATE sixtythree:
" max. frequency
    IF pclk_c32=1 THEN
      pclk=0;
      goto sixtyfour;
    ELSE
     pclk=1;
     goto one;                          " return to state one if BCLK is high
    END IF;
```

PLD (U20) Equations (continued)

```
STATE sixtyfour:
" If the DPLL is synchronized, the state machine is reset to state one in this stage.
    IF pclk_c32=1 THEN
      pclk=0;
      goto sixtyfive;
    ELSE
      pclk=1;
      goto one;
    END IF;
STATE sixtyfive:
" min. frequency
" forces reset to state one
    IF bclk_c32=1 THEN
      pclk=0;
    ELSE
      pclk=1;
    END IF;
    goto one;                                   " force reset to stage one
END DPLL;
```

PLD (20) Equations (IOM-2/GCI Mode)

```
““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““
“ U20 PLD code for the Am186CC CDP Development Module Revision 2.1              “
“ An AMD PLCC-28 PAL22V10 provides clock synchronization between the Am79C031 DSLAC “
“ and the Am79C32A when running in IOM-2/GCI mode                               “
“ Written:   Feb. 1999                                                                    “
“   For  :   Advanced Micro Devices - Austin EPD                                “
“   By   :   LDB - System Engineering                                           “
“                                                                               “
“ Revision 00          2/99          Original Code                              “
““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““
“                              Declarations                 “
““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““
INPUT     mclk_c32;                  “PIN 2:  Am79C32A 12.288 MHz MCLK output
INPUT     bclk_c32;                  “PIN 3:  Am79C32A BCLK output
INPUT     resout;                    “PIN 4:  Am186CC Active High Reset output
INPUT     pclk_c32                   “PIN 5: CLKA output from the Am79C32A

OUTPUT    mclk4;                     “PIN 18: 4.096 MHz Am79C031 MCLK input
OUTPUT    pclk;                      “PIN 25: modified BCLK signal

““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““
“
“                         Equations                                     “
““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““
STATE_MACHINE divider CLOCKED_BY mclk_c32 RESET_BY resout;
“ This state machine generates 4.096MHz clock signal for the DSLAC.
STATE one:
    mclk4=0;
    goto two;
STATE two:
    mclk4=0;
    goto three;
```

PLD (20) Equations (Continued)

```
STATE three:
    mclk4=1;
    goto one;
END divider;

STATE_MACHINE DPLL CLOCKED_BY mclk_c32 RESET_BY resout;

" Jitter reduction circuit, implemented as free running up-counter, that counts 15, 16 or 17
" clock cycles to form a window.  The entire circuit can be viewed as a DPLL

STATE one:
    pclk=1;                 " set the PCLK output to one
    goto two;               " on the next rising edge of the CLK signal go to the next
                            "state !

STATE two:
    pclk=1;
    goto three;
STATE three:
    pclk=1;
    goto four;
STATE four:
    pclk=1;
    goto five;
STATE five:
    pclk=1;
    goto six;
STATE six:
    pclk=1;
    goto seven;
STATE seven:
    pclk=0;
    goto eight;
STATE eight:
    pclk=0;
    goto nine;
```

PLD (20) Equations (Continued)

```
STATE nine:
    pclk=0;
    goto ten;
STATE ten:
    pclk=0;
    goto eleven;
STATE eleven:
    pclk=0;
    goto twelve;
STATE twelve:
    pclk=0;
    goto thirteen;
STATE thirteen:
    pclk=0;
    goto fourteen;
STATE fourteen:
    pclk=0;
    goto fifteen;
" States 15 to 17 form a window to catch the BCLK signal.
STATE fifteen:
" max. frequency
    IF bclk_c32=1 THEN
      pclk=0;
      goto sixteen;
    ELSE
     pclk=1;
     goto one;                          " return to state one if BCLK is high
    END IF;
```

PLD (20) Equations (Continued)

```
STATE sixteen:
"If the DPLL is synchronized, the state machine is reset to state one in this stage.
    IF bclk_c32=1 THEN
      pclk=0;
      goto seventeen;
    ELSE
      pclk=1;
      goto one;                          " return to state one if BCLK is high
    END IF;
STATE seventeen:
"min. frequency
"forces reset to state one
    IF bclk_c32=1 THEN
      pclk=0;
    ELSE
      pclk=1;
      goto one;
    END IF;
   goto one;                             "force reset to stage one
END DPLL;
```

PLD (U24) Equations

```
“““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““
“ U24 PLD code for the Am186CC CDP Development Module Revision 2.1        “
“                                                                          “
“ An AMD PLCC-28 PAL22V10 provides glue logic needed for the POTS interface “
“                                                                          “
“ Written:   Oct. 1998                                                      “
“   For  :   Advanced Micro Devices - Austin EPD                           “
“   By   :   LDB - System Engineering                                       “
“                                                                          “
“ Revision 00        10/98       Original Code                             “
“          01        02/99       Removed SLIC RING-IN Ctrl                 “
“                                                                           “

“““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““
“                               Declarations                  “
“““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““

INPUT   /pcs4;                      “PIN 9:  Am186CC active low PCS4# output
INPUT   /pcs5;                      “PIN 10:  Am186CC active low PCS5# output
INPUT   cctxda;                     “PIN 6:  Am186CC HDLC channel A transmit data output
INPUT   dstsc;                      “PIN 5:  Am79C031 active low time slot control output
INPUT   txdd;                       “PIN 11: Am186CC HDLC channel D transmit data output
INPUT   /tscd;                      “PIN 7:  Am186CC active low time slot control output
OUTPUT  dtmf2oe;                    “PIN 24: Output enable for the DTMF for POTs channel 2
OUTPUT  dtmf1oe;                    “PIN 23: Output enable for the DTMF for POTs channel 2
OUTPUT  txda ENABLED_BY dstsc;      “PIN 17: Am186CC TXDA controlled by DSLAC timeslot
                                    “control
OUTPUT  rxda ENABLED_BY tscd;       “PIN 18: Am186CC TXDD controlled by Am186CC
                                    “timeslot control
```

PLD (U24) Equations (continued)

```
“““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““
“                              Equations                    “
“““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““““

dtmf2oe  = pcs5;                  “Inverted pcs5# to create active high output enable for
                                   “the DTMF on POTS channel 2

dtmf1oe  = pcs4;                  “Inverted pcs4# to create active high output enable for
                                   “the DTMF on POTS channel 1

txda     = cctxda;                “Equals the Am186CC TXDA output when the DSLAC
                                   “is NOT transmitting on the PCM bus.  This is needed
                                   “in case the HDLC TSA’s are configured in muxed mode
                                   “and a POTS line is needed. The Am186CC TXDA
                                   “output will be three-stated when the POTS interface is
                                   “transmitting

rxda     = txdd;                  “Equals the Am186CC TXDD output when PCM
                                   “channel D is transmitting.  This is used if the Am186CC
                                   “is required to transmit data directly to the DSLAC.
```

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