APM883204-X1 | X-Gene™ Multi-Core 64-bit Processor

The AppliedMicro® APM883204-X1 X-Gene™ architecture encompasses a family of computer processors including the Server on a Chip™ processor, the Cloud Processor™, and the Cloud Server™ processor that are optimized for next-generation data center computers, cloud computing, enterprise servers, and embedded communication processors by offering unprecedented improvement in performance per watt per $ against existing solutions in the market. The high level of integration with high-speed peripherals for Storage, PCIe, and 10GE Networking, combined with server class 64-bit ARM™ v8 compliant CPUs and configurable offload capability, result in a solution that dramatically reduces the total cost of ownership for a data center.

Features

- Four X-Gene processor cores operating at up to 2.4 GHz
  - ARM™ v8 compliant 64-bit processor cores
  - Each processor contains a Floating Point Unit (FPU)
  - Each with 32KB L1 Data Cache, 32KB L1 Instruction Cache
- Shared 256KB L2 cache per each pair of processors
- ECC protection on L2 caches, parity protection on L1 caches
- Shared 4MB L3 cache
- Hardware Cache Coherency
- ARM™ Generic Interrupt Controller (GICv2)
- Two DDR3 memory controllers with ECC (72-bit)
- 1MB On-Chip SRAM (OCM)
- QoS capable High-Performance I/O Fabric (IOF)

Offload Features

- Security acceleration for IPSec, SSL/TLS/DTLS, and MACSec protocols
- True Random Number Generator (TRNG)
- Ethernet Classification Engines
- Packet DMA Engine with RAID 5/6 offload
- MSLIM Cluster of Processors
  - Four ARM A5 processors with 32KB I-Cache and 32KB D-Cache
  - Shared 256KB L2 Cache

Queue Manager / Traffic Manager

- Message passing architecture
- Manages Work, Free, and Virtual Queues

High-Speed Interfaces

- Two 10-Gbps Ethernet MACs (XFI/SGMII) and four 1-Gbps Ethernet MACs (SGMII), all with classification and virtualization
- One 1-Gbps Management Interface (RGMII)
- Up to five PCI Express® Gen 3 controllers with internal DMA:
  - 2x 8-lane and 1x 1-lane
  - 1x 8-lane, 2x 4-lane, and 1x 1-lane
  - 4x 4-lane and 1x 1-lane
- Two USB 2.0 Host with integrated PHY
- Six SATA 3.0 ports (four muxed with SGMII)

Other Interfaces

- Two I^2C
- Four UARTs
- GPIOs
- Two SPI
- Two SDIO 3.0
- JTAG / Trace

Power Management:

- Multiple power planes and clock gating

The X-Gene Multi-Core Processor for Performance Applications

The APM883204-X1 X-Gene architecture offers high-end processing performance. For example the innovative Server on a Chip™ subsystem features the Scalable Lightweight Intelligent Management processor (SLIMpro) to enable breakthrough flexibility in power management, resiliency, and end-to-end security for a wide range of applications from data center computers, cloud computing, enterprise servers, embedded communication processors, and other mission-critical systems.

At the heart of the APM883204-X1 are four X-Gene processor cores based on ARM™ v8 Architecture with full SMP/AMP support and individual Floating Point processors. The X-Gene processors are programmable through an industry-standard instruction set architecture (ISA). In addition, these processors are assisted by a rich set of configurable accelerators focused on packet classification, security, packet/data manipulation, and scheduling.

The APM883204-X1 X-Gene architecture provides for a unique congestion-aware and management capability to optimize its available processing resources. This allows for full use control on bandwidth and services.

Designed in 40nm bulk CMOS technology, the APM883204-X1 offers the best-in-class cost versus processing performance in a low-power envelope.

X-Gene Processor Complex Features

The APM883204-X1 incorporates four high performance X-Gene processors. Each X-Gene processor has a 32-KB data cache and a 32-KB instruction cache (which are 8-way set associative), and a floating point unit (FPU) with Single Instruction, Multiple Data (SIMD) execution. Each pair of X-Gene cores has a shared 256KB L2 cache with hardware cache coherency (SMP) and memory resource protection (AMP) that attaches to the high-performance Central Switch (CSW).

A shared 4MB L3 cache is also attached to the CSW.

MSLIM Cluster of Processors

The APM883204-X1 contains an MSLIM Cluster of Processors, which contains four ARM A5 processors with a shared L2 cache. Each processor has its own 32KB I-Cache and 32KB D-Cache and all four processors share a 256KB L2 cache. The MSLIM processors can operate at up to 500 MHz and can be used to provide acceleration to the system.

Classification Engines

The classification engines provide for flow, CoS, and port-based classification of data with 64-byte packet line-rate performance. They are programmable and can support IPv4, IPv6, and AppleTalk, as well as customer proprietary protocols.

Queue Manager / Traffic Manager (QMTM)

The Queue Manager / Traffic Manager allows for the most efficient movement of packets/data between the processors and peripherals using a message passing architecture. This is accomplished through a central communication interface that offloads software from the routing of packets and from transaction synchronization.

The Queue Manager can be used to: centralize management of all transaction traffic, reduce communication overhead between software and hardware, and perform inter-processor message passing and work scheduling.

SLIMpro – Power Management

The APM883204-X1 integrates a dedicated 32-bit SLIMpro acceleration processor that provides advanced capabilities such as dynamic power management and higher layer network acceleration. The SLIMpro processor provides advanced wake up capabilities from Standby.

Specifications

 # Cores / Caches
- Four X-Gene processor cores
  Each processor contains a Floating Point Unit (FPU)
  Each with 32KB L1 Data Cache, 32KB L1 Instruction Cache
- Shared 256 KB L2 cache per each pair of processors
- Shared 4 MB L3 cache

X-Gene Core Frequency
- Up to 2.4 GHz

Junction Temperature Range
- 0ºC to +90ºC

Power Supply
- 0.9V (CPU/SoC logic), 1.35/1.5V (DDR3), 1.8V, 2.5V, and 3.3V

Signal I/Os
- 665

Packaging
1084-pin Heat Spreader Flip Chip Ball Grid Array (HFCBGA)

Advanced Security Engine

The APM883204-X1 can deliver advanced security capabilities with the optional security engine. This security engine utilizes the QMTM for the fastest possible throughput between the processor, memory, and the security engine itself. The security engine supports the following algorithms: DES, 3DES, AES, ARC-4 encryption, MD-5, SHA-1, SHA-2, SHA-224, SHA-256, SHA-384, and SHA-512 hashing with or without HMAC, and also includes acceleration for the following protocols: IPSec, SSL/TLS/DTLS, and MACSec. A true random number generator is also included.

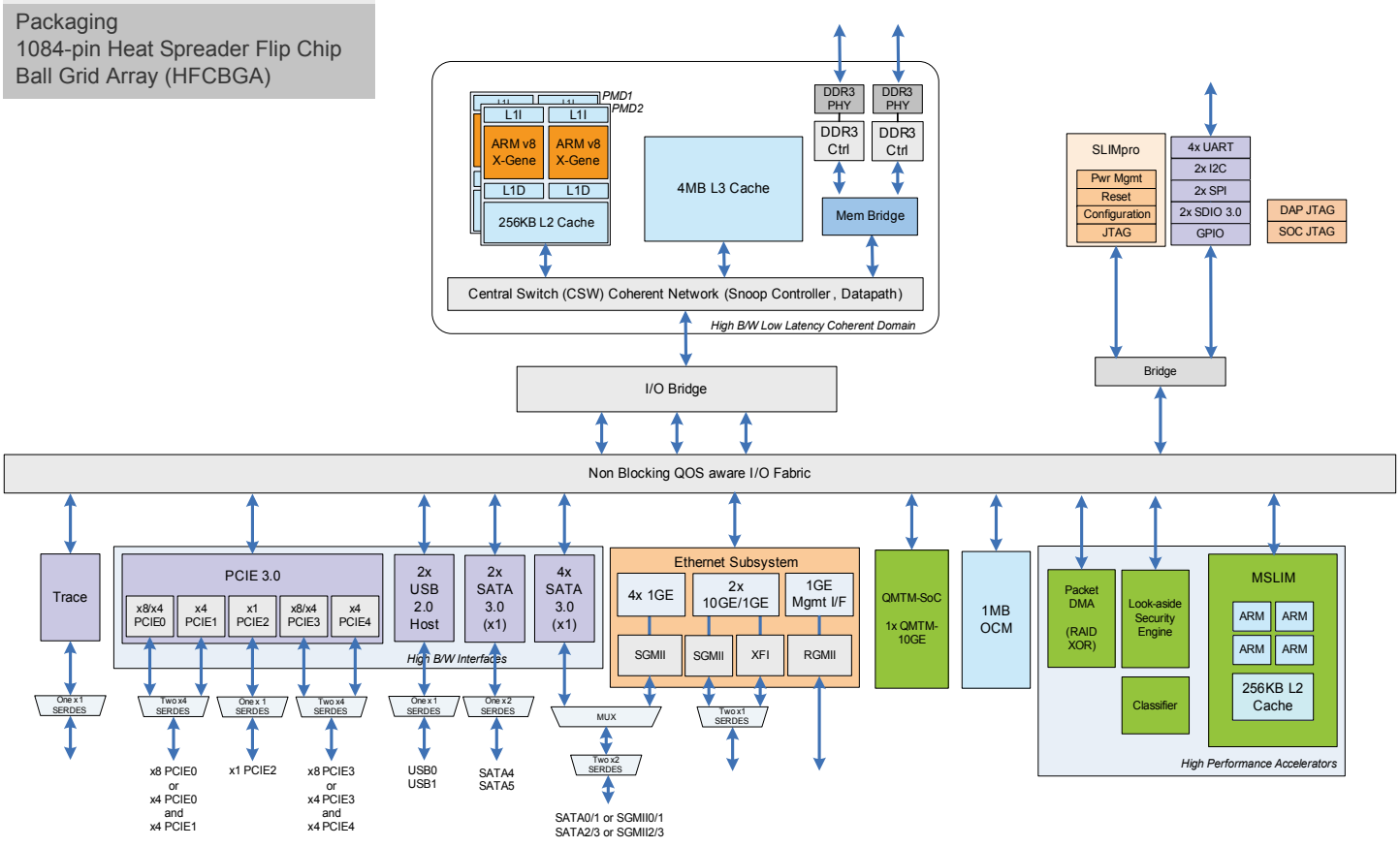
Advanced DMA

The Packet DMA can be used to perform memory-to-memory transfers, which include the SDRAM, SRAM, and PCIe memory spaces. Transfers can also include certain “on-the-fly” data manipulations such as: checksum generation or checking, CRC generation or checking, and XOR. The Packet DMA comprehends data packet delineation, which enables it to perform a comprehensive list of scatter/gather operations for packet assembly and disassembly with minimal software intervention.

AppliedMicro's X-Gene Partner Ecosystem

AppliedMicro's X-Gene processors are supported by an extensive Partner ecosystem of products and services from a wide range of leading suppliers, including industry standard providers of:
- Embedded operating systems
- Hardware and software development tools
- Embedded software products and services
- Board-level products
- System design services
- Technical training

AppliedMicro offers an evaluation kit for product evaluation and for early software development.



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