# 80286

High-Performance Microprocessor with
Memory Management and Protection
PRELIMINARY MILITARY INFORMATION



## DISTINCTIVE CHARACTERISTICS

- High performance processor (up to six times iAPX 86 when using the 8 MHz 80286)
- Large address space
  - 16 megabytes physical
  - 1 gigabyte virtual memory per task
- Integrated memory management, four-level memory protection and support for virtual memory and operating systems
- Military temperature range ($T_C$ = −55 to 125°C)
- Two iAPX 86 upward compatible operating modes
  - iAPX 86 real address mode
  - Protected virtual address mode
- High bandwidth bus interface (16 megabyte/sec)
- Range of clock rates
  - 8 MHz 80286-8

## GENERAL DESCRIPTION

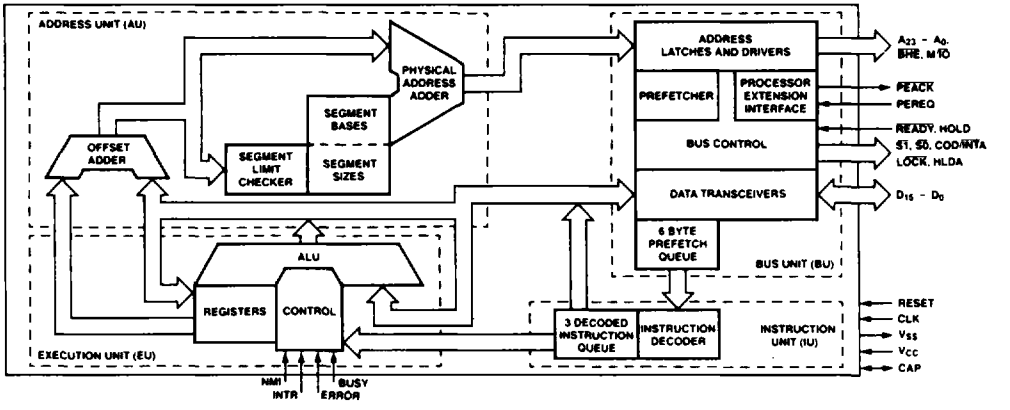
The 80286 is an advanced, high performance microprocessor with specially optimized capabilities for multiple user and multi-tasking systems. The 80286 has built-in memory protection that supports operating system and task isolation as well as program and data privacy within tasks. A 12 MHz 80286 provides up to ten times greater throughput than the standard 5 MHz 8086. The 80286 includes memory management capabilities that map up to $2^{30}$ bytes (one gigabyte) of virtual address space per task into $2^{24}$ bytes (16 megabytes) of physical memory.

The 80286 is upward compatible with iAPX 86 and 88 software. Using iAPX 86 real address mode, the 80286 is object code compatible with existing iAPX 86, 88 software.

In protected virtual address mode, the 80286 is source code compatible with iAPX 86, 88 software and may require upgrading to use virtual addresses supported by the 80286's integrated memory management and protection mechanism. Both modes operate at full 80286 performance and execute a superset of the iAPX 86 and 88 instructions.

The 80286 provides special operations to support the efficient implementation and execution of operating systems. For example, one instruction can end execution of one task, save its state, switch to a new task, load its state, and start execution of the new task. The 80286 also supports virtual memory systems by providing a segment-not-present exception and restartable instructions.

## BLOCK DIAGRAM

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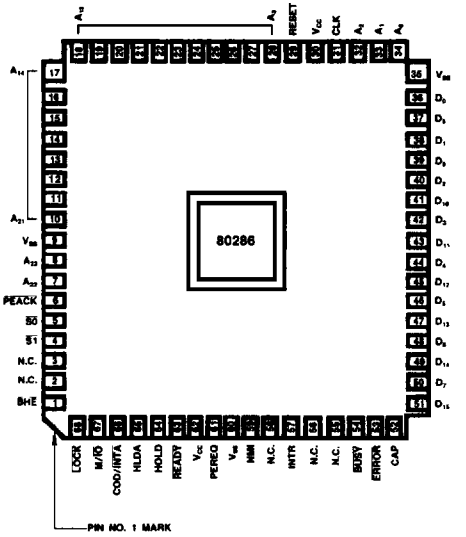
# CONNECTION DIAGRAMS

## LCC

Component Pad Views –
as viewed from underside of component on the P.C. board.

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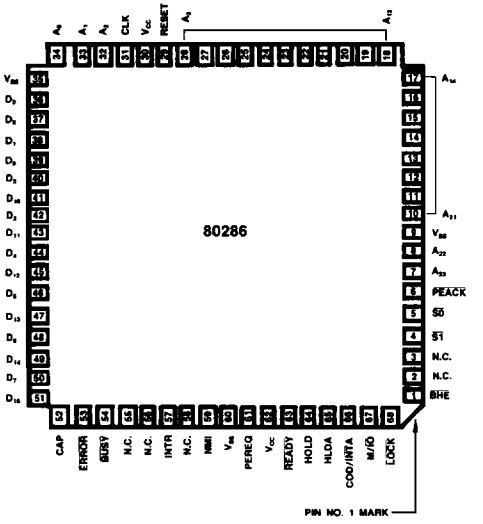
P.C. Board Views –
as viewed from the component side of the P.C. board.

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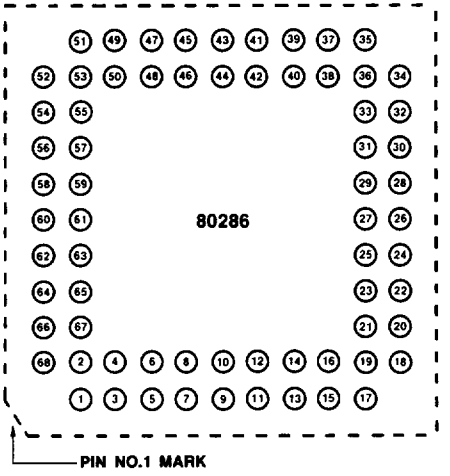
There are no electrical connections on the bottom of this package.

## PGA

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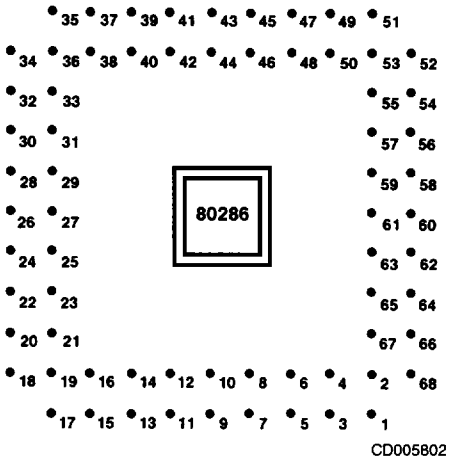
Pins pointing away from viewer

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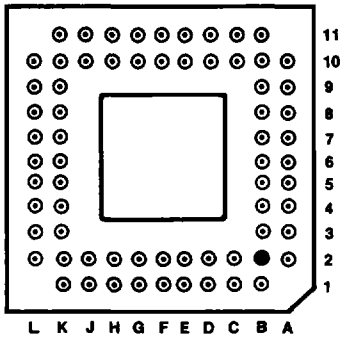
Pins pointing toward viewer

## PGA (continued)

### Bottom View

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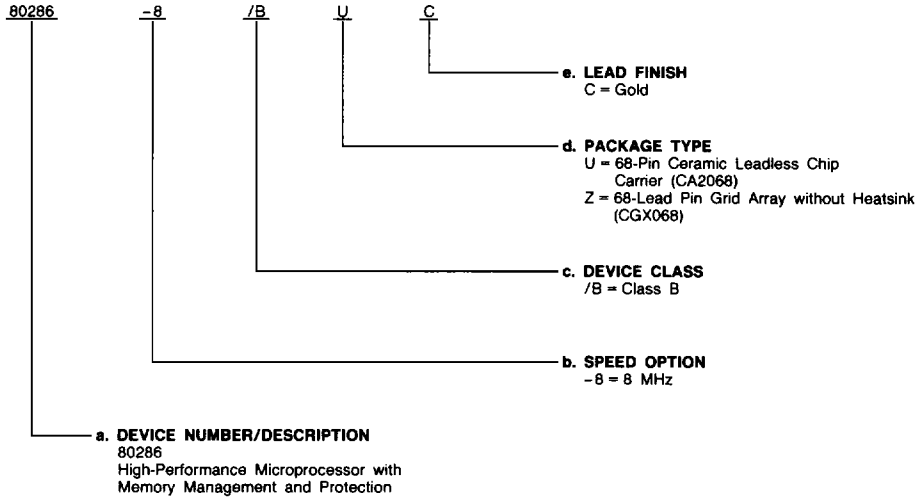
| NAME | PAD | PIN |
|---|---|---|
| $\overline{BHE}$ | 1 | B1 |
| NC | 2 | B2 |
| NC | 3 | C1 |
| $\overline{S1}$ | 4 | C2 |
| $\overline{S0}$ | 5 | D1 |
| $\overline{PEACK}$ | 6 | D2 |
| $A_{23}$ | 7 | E1 |
| $A_{22}$ | 8 | E2 |
| $V_{SS}$ | 9 | F1 |
| $A_{21}$ | 10 | F2 |
| $A_{20}$ | 11 | G1 |
| $A_{19}$ | 12 | G2 |
| $A_{18}$ | 13 | H1 |
| $A_{17}$ | 14 | H2 |
| $A_{16}$ | 15 | J1 |
| $A_{15}$ | 16 | J2 |
| $A_{14}$ | 17 | K1 |
| $A_{13}$ | 18 | L2 |
| $A_{12}$ | 19 | K2 |
| $A_{11}$ | 20 | L3 |
| $A_{10}$ | 21 | K3 |
| $A_9$ | 22 | L4 |
| $A_8$ | 23 | K4 |
| $A_7$ | 24 | L5 |
| $A_6$ | 25 | K5 |
| $A_5$ | 26 | L6 |
| $A_4$ | 27 | K6 |
| $A_3$ | 28 | L7 |
| RESET | 29 | K7 |
| $V_{CC}$ | 30 | L8 |
| CLK | 31 | K8 |
| $A_2$ | 32 | L9 |
| $A_1$ | 33 | K9 |
| $A_0$ | 34 | L10 |

| NAME | PAD | PIN |
|---|---|---|
| $V_{SS}$ | 35 | K11 |
| $D_0$ | 36 | K10 |
| $D_8$ | 37 | J11 |
| $D_1$ | 38 | J10 |
| $D_9$ | 39 | H11 |
| $D_2$ | 40 | H10 |
| $D_{10}$ | 41 | G11 |
| $D_3$ | 42 | G10 |
| $D_{11}$ | 43 | F11 |
| $D_4$ | 44 | F10 |
| $D_{12}$ | 45 | E11 |
| $D_5$ | 46 | E10 |
| $D_{13}$ | 47 | D11 |
| $D_6$ | 48 | D10 |
| $D_{14}$ | 49 | C11 |
| $D_7$ | 50 | C10 |
| $D_{15}$ | 51 | B11 |
| CAP | 52 | A10 |
| $\overline{ERROR}$ | 53 | B10 |
| $\overline{BUSY}$ | 54 | A9 |
| NC | 55 | B9 |
| NC | 56 | A8 |
| INTR | 57 | B8 |
| NC | 58 | A7 |
| NMI | 59 | B7 |
| $V_{SS}$ | 60 | A6 |
| PEREQ | 61 | B6 |
| $V_{CC}$ | 62 | A5 |
| $\overline{READY}$ | 63 | B5 |
| HOLD | 64 | A4 |
| HLDA | 65 | B4 |
| COD/$\overline{INTA}$ | 66 | A3 |
| M/$\overline{IO}$ | 67 | B3 |
| $\overline{LOCK}$ | 68 | A2 |

# MILITARY ORDERING INFORMATION

## APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
**b. Speed Option** (if applicable)
**c. Device Class**
**d. Package Type**
**e. Lead Finish**




| Valid Combinations | |
|---|---|
| 80286-8 | /BUC, /BZC |

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

### Group A Tests

Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Voltage on Any Pin with
Respect to Ground..... −1.0 to +7.0 V
Power Dissipation ..... 3.3 Watts

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Military (M) Devices
Temperature ($T_C$)..... −55 to +125°C
Supply Voltage ($V_{CC}$) ..... 5 V ± 10%

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

**DC CHARACTERISTICS** over operating range (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

| Parameter Symbol | Parameter Description | Test Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{IL}$ | Input LOW Voltage | | −.5 | .8 | V |
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | $V_{CC}$ + .5 | V |
| $V_{ILC}$ | CLK Input LOW Voltage | | −.5 | .6 | V |
| $V_{IHC}$ | CLK Input HIGH Voltage | | 3.8 | $V_{CC}$ + .5 | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 2.0 mA | | .45 | V |
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = −400 µA | 2.4 | | V |
| $I_{LI}$ | Input Leakage Current | 0 V ≤ $V_{IN}$ ≤ $V_{CC}$ | | ±10 | µA |
| $I_{LO}$ | Output Leakage Current | .45 ≤ $V_{OUT}$ ≤ $V_{CC}$ | | ±10 | µA |
| $I_{CC}$ | Supply Current (turn on, 0°C) | [illegible] | | 600 | mA |
| $I_{LO}$ | Output Leakage Current | [illegible] ≤ $V_{OUT}$ ≤ .5 V | | ±1 | mA |
| $I_{IL}$ | Input Sustaining Current on $\overline{BUSY}$ and $\overline{ERROR}$ pins | $V_{in}$ = 0 V | 30 | 500 | µA |

Notes: 1. Low temperature is worst case.



## CAPACITANCE*

| Parameter Symbol | Parameter Description | Test Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $C_{CLK}$ † | CLK Input Capacitance | $f_C$ = 1 MHz | | 20* | pF |
| $C_{IN}$ † | Other Input Capacitance | $f_C$ = 1 MHz | | 10* | pF |
| $C_O$ † | Input/Output Capacitance | $f_C$ = 1 MHz | | 20* | pF |

* Not tested; guaranteed by design.
† Not included in Group A tests.

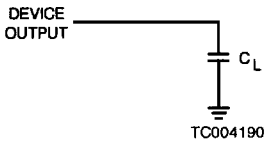
See Section 6 of the MOS Microprocessors and Peripherals Data Book (Order #09067A) for Thermal Characteristics Information.

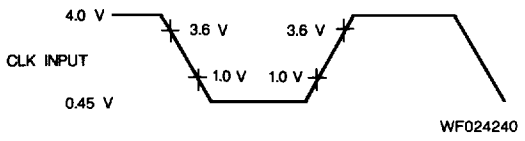
**SWITCHING CHARACTERISTICS** over operating range (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted) ($V_{CC}$ = 5 V ± 10%, $T_C$ = −55 to +125°C); AC timings are referenced to 0.8 V and 2.0 V points of signals as illustrated in datasheet waveforms, unless otherwise noted.

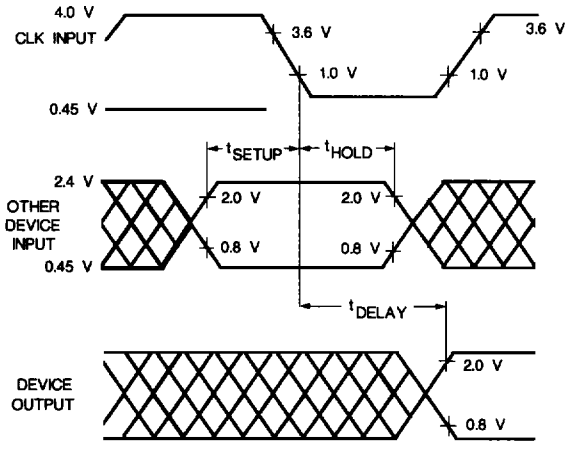
| No. | Parameter Description | Test Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| 1 | System Clock (CLK) Period | | 62 | 250 | ns |
| 2 | System Clock (CLK) LOW Time | at 1.0 V | 15 | 225 | ns |
| 3 | System Clock (CLK) HIGH Time | at 3.6 V | 25 | 235 | ns |
| 17 | System Clock (CLK) Rise Time | 1.0 V to 3.6 V | | 10 | ns |
| 18 | System Clock (CLK) Fall Time | 3.6 V to 1.0 V | | 10 | ns |
| 4 | Asynch. Inputs Set-up Time | Note 1 | 20 | | ns |
| 5 | Asynch. Inputs Hold Time | Note 1 | 20 | | ns |
| 6 | RESET Set-up Time | | 28 | | ns |
| 7 | RESET Hold Time | | 5 | | ns |
| 8 | Read Data Set-up Time | | 10 | | ns |
| 9 | Read Data Hold Time | | 8 | | ns |
| 10 | $\overline{\text{READY}}$ Set-up Time | | 38 | | ns |
| 11 | $\overline{\text{READY}}$ Hold Time | | 25 | | ns |
| 12 | Status/$\overline{\text{PEACK}}$ Valid Delay | Note 2, Note 3 | 1 | 40 | ns |
| 12a | Status/$\overline{\text{PEACK}}$ Active Delay | Note 2, Note 3 | - | - | ns |
| 12b | Status/$\overline{\text{PEACK}}$ Inactive Delay | Note 2, Note 3 | - | - | ns |
| 13 | Address Valid Delay | Note 2, Note 3 | 1 | 60 | ns |
| 14 | Write Data Valid Delay | Note 2, Note 3 | 0 | 50 | ns |
| 15 | Address/Status/Data Float Delay | Note 2, Note 4 | 0 | 50 | ns |
| 16 | HLDA Valid Delay | Note 2, Note 3 | 0 | 50 | ns |
| 19 | Address Valid To Status Valid Setup Time | Note 3, Note 5, Note 6 | 38 | | ns |



Notes:
1. Asynchronous inputs are INTR, NMI, HOLD PEREQ, $\overline{\text{ERROR}}$, and $\overline{\text{BUSY}}$. This specification is given only for testing purposes to assure recognition at a specific CLK edge.
2. Delay from 0.8 V on the CLK to 0.8 V or 2.0 V or float on the output as appropriate for valid or floating condition.
3. Output load: $C_L$ = 100 pF.
4. Float condition occurs when output current is less than $I_{LO}$ in magnitude.
5. Delay measured from address either reaching 0.8 V or 2.0 V (valid) to status going active reaching 2.0 V or status going inactive reaching 0.8 V.
6. For load capacitance of 10 pF on STATUS/$\overline{\text{PEACK}}$ lines, subtract typically 7 ns for 8 MHz spec.



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## 82284 Timing Requirements

| No. | Parameter Description | Test Conditions | 82284-8 Min. | 82284-8 Max. | Unit |
|---|---|---|---|---|---|
| 11 | $\overline{SRDY}/\overline{SRDYEN}$ Set-up Time | | 17 | | ns |
| 12 | $\overline{SRDY}/\overline{SRDYEN}$ Hold Time | | 0 | | ns |
| 13 | $\overline{ARDY}/\overline{ARDYEN}$ Set-up Time | Note 1 | 0 | | ns |
| 14 | $\overline{ARDY}/\overline{ARDYEN}$ Hold Time | Note 1 | 30 | | ns |
| 19 | PCLK Delay | $C_L$ = 75 pF<br>$I_{OL}$ = 5 mA<br>$I_{OH}$ = −1 | 0 | 45 | ns |

Note 1. These times are given for testing purposes to assure a predetermined action.

## 82C288 Timing Requirements

| No. | Parameter Description | Test Conditions | 82C288-8 Min. | 82C288-8 Max. | Unit |
|---|---|---|---|---|---|
| 12 | CMDLY Set-up Time | | 20 | | ns |
| 13 | CMDLT Hold Time | | 1 | | ns |
| 30 | Command Delay from CLK — Command Inactive | $C_L$ = 300 pF Max.<br>$I_{OL}$ = 32 mA Max.<br>$I_{OH}$ = 5 mA Max. | 5 | 25 | ns |
| 29 | Command Delay from CLK — Command Active | | 3 | 25 | |
| 16 | ALE Active Delay | $C_L$ = 150 pF<br>$I_{OL}$ = 16 mA Max.<br>$I_{OH}$ = −1 mA Max. | 3 | 20 | ns |
| 17 | ALE Inactive Delay | | | 25 | ns |
| 19 | DT/$\overline{R}$ Read Active Delay | | | 25 | ns |
| 22 | DT/$\overline{R}$ Read Inactive Delay | | 5 | 35 | ns |
| 20 | DEN Read Active Delay | | 5 | 35 | ns |
| 21 | DEN Read Inactive Delay | | 3 | 35 | ns |
| 23 | DEN Write Active Delay | | | 30 | ns |
| 24 | DEN Write Inactive Delay | | 3 | 30 | ns |