Intel® Core™ Microarchitecture

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Agenda

• Multi-core Update and New Microarchitecture Level Set
• New Intel® Core™ Microarchitecture
• Wrap Up
### Ramping Multi-core Everywhere

<table>
<thead>
<tr>
<th></th>
<th>2005</th>
<th>2006*</th>
<th>2007*</th>
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<tr>
<td><strong>Desktop</strong></td>
<td><strong>Shipping</strong></td>
<td>&gt;70%</td>
<td>&gt;90%</td>
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<td>Mainstream/Performance</td>
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* Data is projected run rate exiting the year. Source: Intel

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**Broadly Delivering Benefits of Parallelism**

All products and dates are preliminary and subject to change without notice.
Refresher: What is Multi-Core?

Two or more independent execution cores in the same processor

Specific implementations will vary over time - driven by product implementation and manufacturing efficiencies

- Best mix of product architecture and volume mfg capabilities
  - Architecture: Shared Caches vs. Independent Caches
  - Mfg capabilities: volume packaging technology
- Designed to deliver performance, OEM and end user experience

**Single die (Monolithic) based processor**
- Example: 90nm Pentium® D Processor (Smithfield)

**Multi-Chip Processor**
- Example: Intel Core™ Duo Processor (Yonah)
- Example: 65nm Pentium D Processor (Presler)

*Not representative of actual die photos or relative size*
Intel® Core™ Micro-architecture

TODAY

+ New innovations

Q3’06

Wide Dynamic Execution
Advanced Digital Media Boost
Smart Memory Access
Advanced Smart Cache
Intelligent Power Capability

*Not representative of actual die photo or relative size
Intel® Core™ Microarchitecture Based Platforms

<table>
<thead>
<tr>
<th>Platform</th>
<th>2006</th>
<th>2007</th>
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<tbody>
<tr>
<td>MP Servers</td>
<td></td>
<td>Caneland Platform (2007)</td>
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<td></td>
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<td>Tigerton (QC) (2007)</td>
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<tr>
<td>DP Servers/</td>
<td>Bensley Platform (Q2’06)/ Glidewell Platform</td>
<td>Woodcrest (Q3’06)</td>
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<tr>
<td>DP Workstation</td>
<td>(Q2’06)</td>
<td>Clovertown (QC) (Q1’07)</td>
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<tr>
<td>UP Servers/</td>
<td>Kaylo Platform (Q3’06)/ Wyloway Platform</td>
<td>Conroe (Q3’06)</td>
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<tr>
<td>UP Workstation</td>
<td>(Q3’06)</td>
<td>Kentsfield (QC) (Q1’07)</td>
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<tr>
<td>Desktop -Home</td>
<td>Bridge Creek Platform (Mid’06)</td>
<td>Conroe (Q3’06)</td>
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<td>Kentsfield (QC) (Q1’07)</td>
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<td>Desktop -Office</td>
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<tr>
<td>Mobile Client</td>
<td>Napa Platform (Q1’06)</td>
<td>Merom (2H’06)</td>
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</tbody>
</table>

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Note: only Intel® Core™ microarchitecture based processors listed

QC refers to Quad-Core
Delivering both industry leading performance and performance/watt

- **Conroe**: >40% improvement in performance¹ & >40% reduction in power²
  - As compared to today’s high-end Pentium® D processor 950 (formerly Presler)

- **Woodcrest**: >80% improvement in performance¹ and >35% reduction in power²
  - As compared to today’s high-end Dual-Core Intel® Xeon® processor 2.8GHz (formerly Paxville DP)

- **Merom**: Extends the already significant performance and performance/watt leadership delivered with today’s Intel® Core™ Duo processor with greater than 20% additional performance¹ improvement
  - As compared to today’s high-end Intel® Core™ Duo processor (formerly Yonah)

¹ - Estimated SPECint*_rate_base2000
² – Expected reduction in TDP
Agenda

• Multi-core Update and New Micro-architecture level set
• New Intel® Core™ Microarchitecture
• Summary
Inside the Intel® Core™ Microarchitecture
Agenda

- Multi-core Update and New Micro-architecture level set
- New Intel® Core™ Microarchitecture
  - Intel Microarchitecture History
  - Intel® Core™ Microarchitecture Design Goals and Roadmap
  - Processor Architecture 101
  - Intel® Core™ Microarchitecture
  - Software Implications
- Wrap Up
New Microarchitecture Coming in 2006

Examples:

EPIC* (Itanium®)  
x86  
IXA* (xScale)

Examples:
P5  
P6  
Intel NetBurst®  
Banias  
Intel® Core™

Examples:
Pentium®  
Pentium® Pro  
Pentium® II/III  
Pentium® 4  
Pentium® D  
Xeon®  
Pentium® M  
Core Duo®  

Controe  
Woodcrest  
Merom
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Intel® Core™ Microarchitecture: Design Goals

• Deliver world class performance combined with superior energy/power efficiency
  – Existing and emerging applications and uses
  – Greater performance and performance/watt
  – Optimized for Intel Multi-core platforms

• Deliver single foundation for optimized processors across each segment and power envelope
  – Optimized for mobile, desktop and server segments

Driving Performance and Performance/Watt Leadership
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Processor Architecture 101

Delivered Performance = Frequency * Instructions Per Cycle (IPC)

Goal is higher performance and lower power

Power \propto C_{\text{dynamic}} \times V \times V \times \text{Frequency}

$C_{\text{dynamic}}$ is roughly a product of area and activity

“how many bits” * “how much do they toggle”
Delivered Performance = Frequency * Instructions Per Cycle (IPC)

Frequency is proportional to voltage, so frequency reduction coupled with voltage reduction results in cubic reduction in power.

Power $\propto C_{\text{dynamic}} \ast V \ast V \ast Frequency$
Processor Architecture 101

Delivered Performance = Frequency * Instructions Per Cycle (IPC)

Higher IPC usually results in wider data paths and/or more speculation:

directly increasing C dynamic

Power \( \propto C_{\text{dynamic}} \times V \times V \times \text{Frequency} \)
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Intel® Core™ Microarchitecture

Block Diagram Walkthrough
Intel® Core™ Microarchitecture

**in order**

instruction fetch
instruction decode
micro-op rename
micro-op allocate
Intel® Core™ Microarchitecture

**out of order**

micro-op schedule
micro-op execute
Intel® Core™ Microarchitecture

**out of order**

memory pipelines

memory order unit maintains architectural ordering requirements
Intel® Core™ Microarchitecture

**in order**

Micro-op retirement fault handling

Retirement Unit maintains illusion of in order instruction retirement
Intel® Core™ Microarchitecture

Wide Dynamic Execution
Advanced Digital Media Boost
Smart Memory Access
Advanced Smart Cache
Intelligent Power Capability

New, State-of-the-Art, Microarchitecture
Wide Dynamic Execution

Start with Instruction Fetch

four(+) instructions / cycle

>33% increase over other x86 processors

Instructions converted to micro-ops (uops)

~1 uop per x86 instruction
Micro-op Reduction (recall Processor 101)

Delivered Performance = Frequency * Instructions Per Cycle (IPC)

Power = $C_{dynamic} \times V \times V \times Frequency$

Fewer uops per instruction allows IPC to be increased while lowering $C_{dynamic}$ (less bits and less toggling)
Techniques for Micro-op Reduction

- **ESP Tracker (Extended Stack Pointer)**
  - Execute Stack Pointer updates in dedicated hardware
  - *Intel® Core™ microarchitecture increases BW by 33%*

- **Micro-Op Micro-Fusion**
  - Single Uop representation of “multi-uop” instruction
  - *Intel® Core™ microarchitecture increase # instructions*

- **Macro-Fusion**
  - New technique in Intel® Core™ microarchitecture (more on next pages)

*Techniques pioneered on Intel® Pentium® M processors*
New: Macro-Fusion

• Represent common x86 instruction pairs in single micro-op
  – CMP or TEST + Conditional Branch (Jcc)

• Enhanced Arithmetic Logic Unit (ALU) for macro-fusion
  – Single dispatch - efficiency
  – Single cycle execution - performance
Without Macro-Fusion

Read four instructions from Instruction Queue

Each instruction gets decoded into separate uops
With Intel’s New Macro-Fusion

Read five Instructions from Instruction Queue

Send fusible pair to single decoder

Single uop represents two instructions

Instruction Queue

- inc ecx
- store [mem3], ebx
- jne targ
- cmp eax, [mem2]
- load eax, [mem1]

Cycle 1

dec0 dec1 dec2 dec3

inc ecx
store [mem3], ebx
cmpjne eax, [mem2], targ
load eax, [mem1]
Macro-Fusion (cont)

- Lower latency
- Increased bandwidth
  “virtually” increase storage

Macro-fusion makes the machine behave as if it is wider and deeper, without the additional cost

Enabling Greater Performance & Efficiency
Wide Dynamic Execution

- 4 wide rename
- 4 wide micro-op execution
- 4 wide retire
- Deeper out of order storage
- 32 discontiguous micro-ops considered for dispatch per cycle

33% Wider Than Previous Generation
Advanced Digital Media Boost

128-bit packed Multiply
plus

128-bit packed Add
plus

128-bit packed Load
plus

128-bit packed Store
plus

(how about a CMPJCC)

2x Compute Throughput / Clock
**Advanced Digital Media Boost**

*Let's scale a vector:*

\[ B[i] := A[i] \times C \]

**Existing Processor**

**Intel® Core™ uarch**

**Advanced Digital Media Boost**

2x Compute Throughput / Clock
Advanced Digital Media Boost

Assume both Microarchitectures have 128-bit path from L1 to Processor

A

Existing Processor

B

Intel® Core™ uarch
Advanced Digital Media Boost

2x Compute Throughput / Clock
Advanced Digital Media Boost

...handles all the memory data

Multiply can't keep up with load bandwidth

Existing Processor

Intel® Core™ uarch
Advanced Digital Media Boost

2x Compute Throughput / Clock

multiplier operates on all data
Advanced Digital Media Boost

Existing implementations eventually stall the load pipe waiting for multiplier

Load eventually stalls waiting for multiplier

Existing Processor

Intel® Core™ uarch
Advanced Digital Media Boost

Load pipe is free to advance

2x Compute Throughput / Clock
Advanced Digital Media Boost

...keeps pipeline free for computations

Load eventually stalls waiting for multiplier

Existing Processor

Intel® Core™ uarch Advanced Digital Media Boost

Load pipe is free to advance

2x Compute Throughput / Clock
**Advanced Digital Media Boost**

*...maintains 2X throughput compared to prior implementations*

Load eventually stalls waiting for multiplier

- **A**
  - Existing Processor
  - Advanced Digital Media Boost

Load pipe is free to advance

- **B**
  - Intel® Core™ uarch
  - 2x Compute Throughput / Clock
Advanced Digital Media Boost

8 Single Precision Flops/cycle

Load eventually stalls waiting for multiplier

Existing Processor

Intel® Core™ uarch Advanced Digital Media Boost

Load pipe is free to advance

2x Compute Throughput / Clock
Advanced Digital Media Boost

4 Double Precision Flops/cycle

**A**

Load eventually stalls waiting for multiplier

**B**

Load pipe is free to advance

**Existing Processor**

**Intel® Core™ uarch**

Advanced Digital Media Boost

2x Compute Throughput / Clock
Advanced Digital Media Boost

Load eventually stalls waiting for multiplier

Existing Processor

Intel® Core™ uarch
Advanced Digital Media Boost

Load pipe is free to advance

2x Compute Throughput / Clock
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Intel® Core™ uarch

Advanced Digital Media Boost

2x Compute Throughput / Clock
Advanced Digital Media Boost

Load eventually stalls waiting for multiplier

Existing Processor

Intel® Core™ uarch Advanced Digital Media Boost

Load pipe is free to advance

A

B

2x Compute Throughput / Clock
Advanced Digital Media Boost

Load eventually stalls waiting for multiplier

Existing Processor

Intel® Core™ uarch
Advanced Digital Media Boost

Load pipe is free to advance

2x Compute Throughput / Clock
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Load eventually stalls waiting for multiplier

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Load pipe is free to advance

Intel® Core™ uarch
Advanced Digital Media Boost

2x Compute Throughput / Clock
Advanced Digital Media Boost

Load eventually stalls waiting for multiplier

Load pipe is free to advance

Existing Processor

Intel® Core™ uarch

Advanced Digital Media Boost

Leading Compute Density
2x Compute Throughput / Clock
Smart Memory Access

- Memory Disambiguation
- Improved Prefetchers
Smart Memory Access – Goal

System Bus

L1 Data Cache → Smart-Shared L2 Cache → L1 Data Cache

CORE1 → Smart-Shared L2 Cache → CORE2

WHEN
Ensure data can be used as **early** as possible

WHERE
Ensure user of data has it as **close** as possible

Hiding Latency to Memory Subsystem
Without Memory Disambiguation

Subsequent Loads Must Wait

Load4 must WAIT until previous stores complete

Waits for Data X before can execute

Intel Developer FORUM
Smart Memory Access

With Intel’s New Memory Disambiguation

Loads can decouple from Stores

Load4 can get its data FIRST

Solving the Problem of When

Data X

Data Y

Data Z

Data W

Load4
Store3
Load2
Store1
Smart Memory Access

**Memory Disambiguation**

- Memory Disambiguation predictor
  - Loads that are predicted NOT to forward from preceding store are allowed to schedule as early as possible
    - increasing the performance of OOO memory pipelines

- Disambiguated loads checked at retirement
  - Extension to existing coherency mechanism
  - Invisible to software and system

Hiding Latency to Memory Subsystem
Smart Memory Access

Prefetchers

L1 Data Cache

Shared L2 Data Cache

Load1
Load2
Load3
Load4

youngest

oldest
Smart Memory Access: Prefetchers

- Memory is too far away

Oldest

- Load1
- Load2
- Load3
- Load4

Youngest

L1 Data Cache

Shared L2 Data Cache
Caches are closer when they have the data.
Smart Memory Access: Prefetchers

Prefetchers detect applications data reference patterns.

Load1
Load2
Load3
Load4

L1 Data Cache
Shared L2 Data Cache

youngest
oldest
Smart Memory Access: Prefetchers

And bring the data closer to data consumer
Smart Memory Access: Prefetchers

Solving the Problem of Minimizing Memory Latency
Prefetchers and Multi-Core
Prefetchers and Multi-Core

Three Individual Prefetchers per Core
Two L2 Prefetchers dynamically shared
Smart Memory Access

- 8 Prefetchers per two-core processor
  - 2 data and 1 instruction prefetcher per core
    - able to handle multiple simultaneous patterns
  - 2 prefetchers in the L2 cache
    - tracking multiple patterns per core

- Prefetchers monitor demand traffic and regulate “aggression”

- Implementation “knobs” allow platform and segment specific settings tailored to applications and usage models

Data Is Where You Need It, When You Need It
Advanced Smart Cache
Multi-core Optimized

All the Smart Cache benefits:
• L2 can adapt to each core’s load
• Fast data sharing
• No replicated data

Plus:
• 2X BW to L1 caches

Shared & Multi-Core Optimized, with 2x Bandwidth
Advanced Smart Cache

Dynamic Cache Allocation

Independent Cache (today)

Shared Cache adapts to mismatched loads. Independent Cache can thrash heavy app even when other cache is under-utilized.

Advanced Smart Cache
Advanced Smart Cache

Efficient Data Sharing

Advanced Smart Cache

- Core1
- Core2
- L2 Cache

Independent Cache

- Core1
- Core2
- L2 Cache
- L2 Cache

FSB

Main memory

2X L2 to L1 Bandwidth
Intelligent Power Capability

Extending the power management architecture
  • Intel® Pentium® M processor innovated a new power management architecture
  • Intel® Core™ Duo extended the Pentium® M processor capability to multi-core

New Power Features within each processor core
  • Ultra fine-grained power control
  • Split Busses
  • Platformization of Power Management Architecture
Intelligent Power Capability

Even during periods of high performance execution, many parts of the chip core can be shut off.

Example could be a SW memory initialization executing from front end with IQ operating as loop cache.
Intelligent Power Capability

Split Busses (core power feature)

Many buses are sized for worst-case data
(x86 instruction of 15 bytes)
(ALU can write-back 128 bits)

Improved Energy Efficiency
Intelligent Power Capability
Split Busses (core power feature)

By splitting buses to deal with varying data widths, we can gain the performance benefit of bus width while maintaining C dynamic closer to thinner buses.

Improved Energy Efficiency
Platformization of Power Management Architecture

- Integrating best features from Server and Mobile products
- Exposing more to the system

- PSI-2 Power Status Indicator (Mobile)
- DTS Digital Thermal Sensors
- PECI Interface Platform Environment Control
Power Status Indicator (Mobile)

- Processor communicates power consumption to external platform components
  - Optimization of voltage regulator efficiency
  - Load line and power delivery efficiency
Enabling Efficient Processor and Platform Thermal Control...

**DTS – Digital Thermal Sensor**

- Several thermal sensors are located within the Processor to cover all possible hot spots.
- Dedicated logic scans the thermal sensors and measures the maximum temperature on the die at any given time.
- Accurately reporting Processor temperature enables advanced thermal control schemes.
• Processor provides its temperature reading over a **multi drop single wire bus** allowing efficient platform thermal control.
33% wider pipes (4 vs. 3) and greater efficiency

2x compute throughput / clock

Minimizing latency – Data Where & When needed

Multi-Core optimized, shared with 2x bandwidth

Improved energy efficient performance

Wide Dynamic Execution

Advanced Digital Media Boost

Smart Memory Access

Advanced Smart Cache

Intelligent Power Capability

New, State-of-the-Art, Microarchitecture
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**Intel® Core™ Microarchitecture and Software**

- **Software consistency across application space**
  - Wide Dynamic Execution will provide generic performance gains
  - Smart Memory Access targets memory intensive apps
  - Advanced Digital Media Boost provides a leap in capability for media and floating point apps
  - Multi-Core and Advanced Smart Cache further improve the growing number of multi-threaded applications

- **Software consistency across markets segments**
  - New apps and optimizations can target single microarchitecture

**Immediate Performance Increase Across Applications and Segments**
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Summary

Continuing to drive aggressive multi-core ramp
- Dual-core ramp in 2006, quad-core starts in early 2007

Intel® Core™ microarchitecture delivers leading performance and performance/watt
- Conroe – >40% performance increase\(^1\) / >40% less power
- Woodcrest - >80% performance increase\(^1\) / >35% less power
- Mobile - Extending leadership delivered with Intel® Core™ Duo with >20% performance increase\(^1\)

On track for product introductions starting in Q3’06
- Based upon new Intel® Core™ microarchitecture

1 - Estimated SPECint* rate