Alpha 21364: A Scalable Single-chip SMP

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Outline

- Alpha Roadmap
- Alpha 21364

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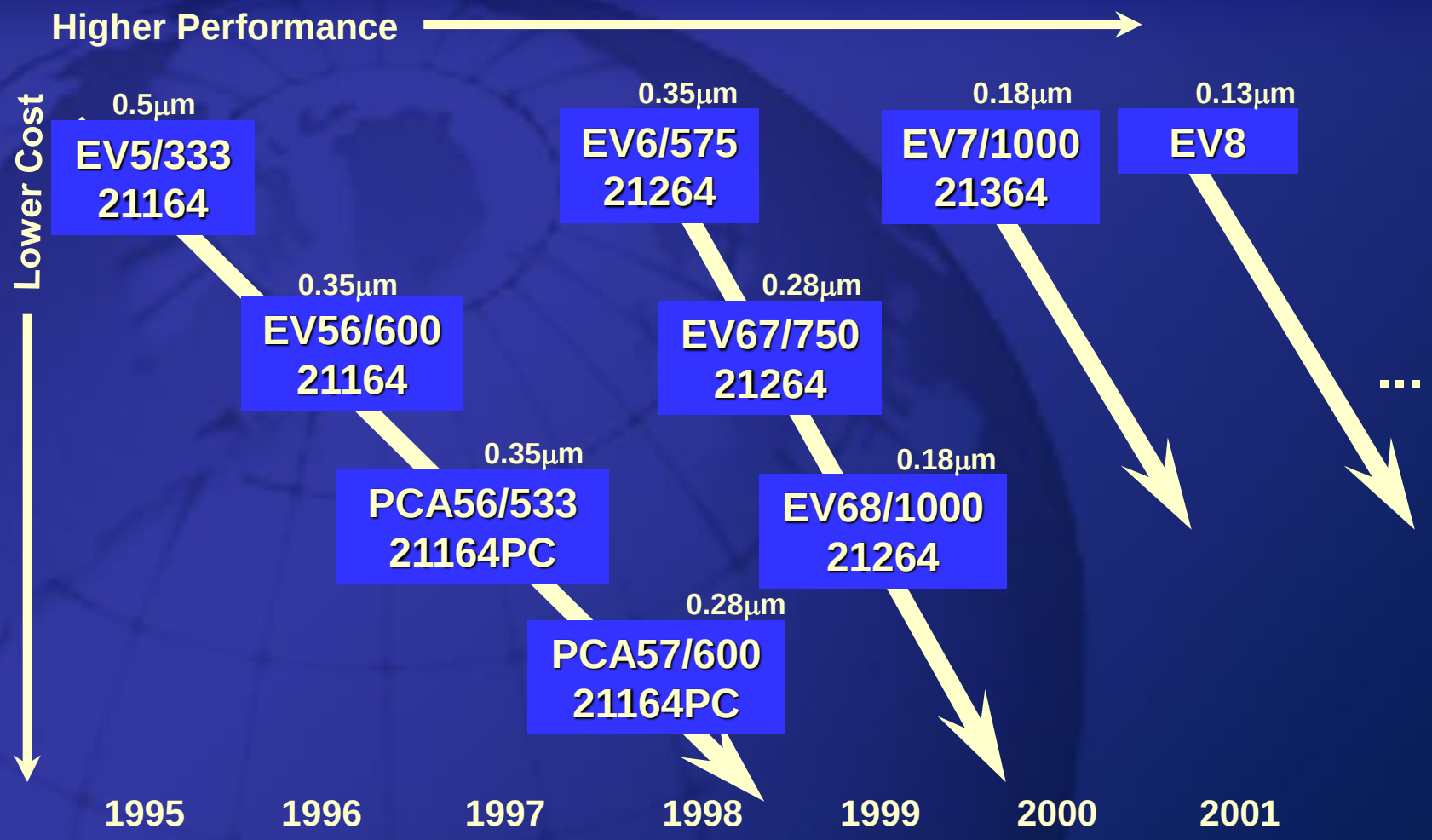
Alpha Roadmap



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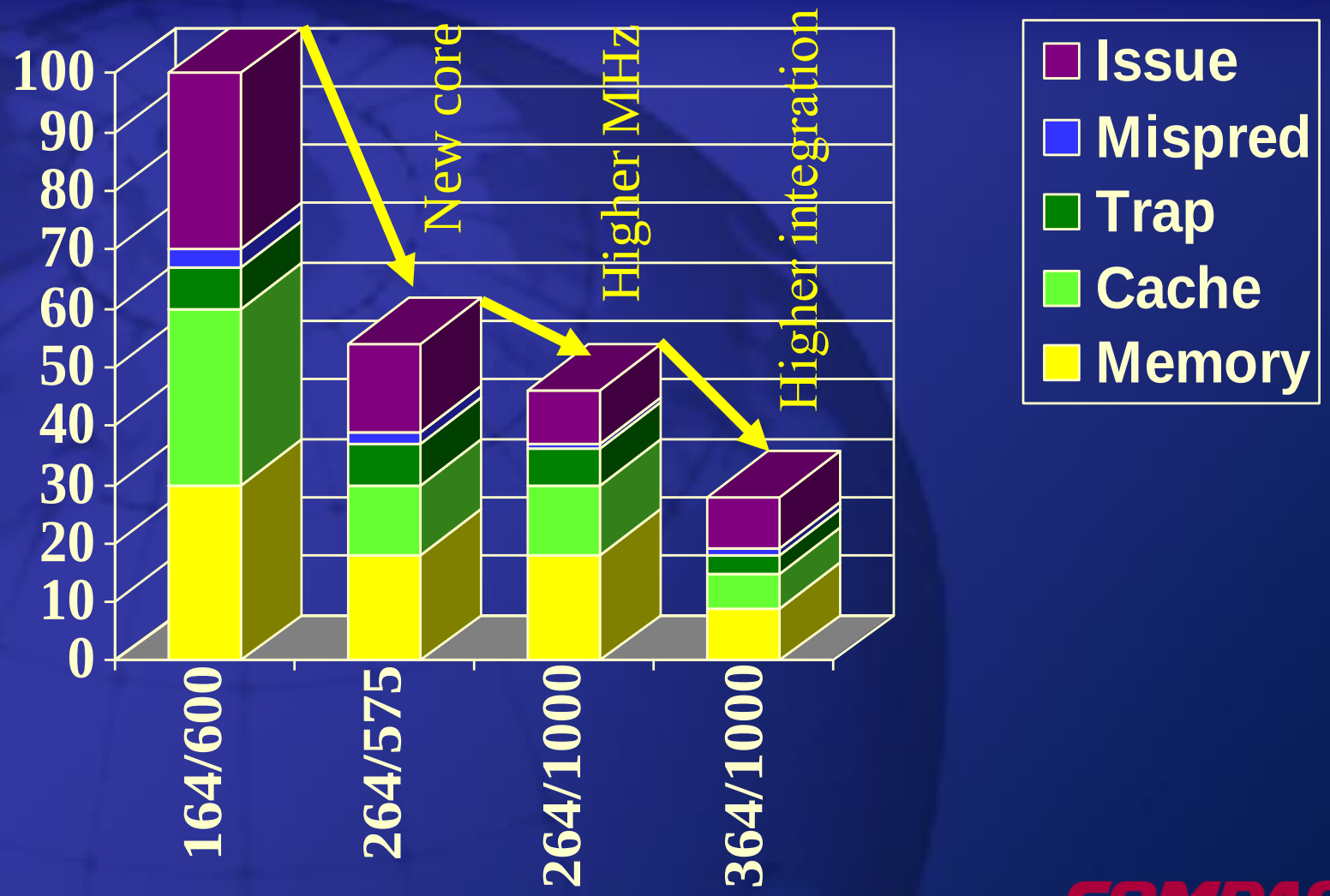
Estimated time for TPC-C



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Alpha 21364 Features

- Alpha 21264 core with enhancements
- Integrated L2 Cache
- Integrated memory controller
- Integrated network interface
- Support for lock-step operation to enable high-availability systems.

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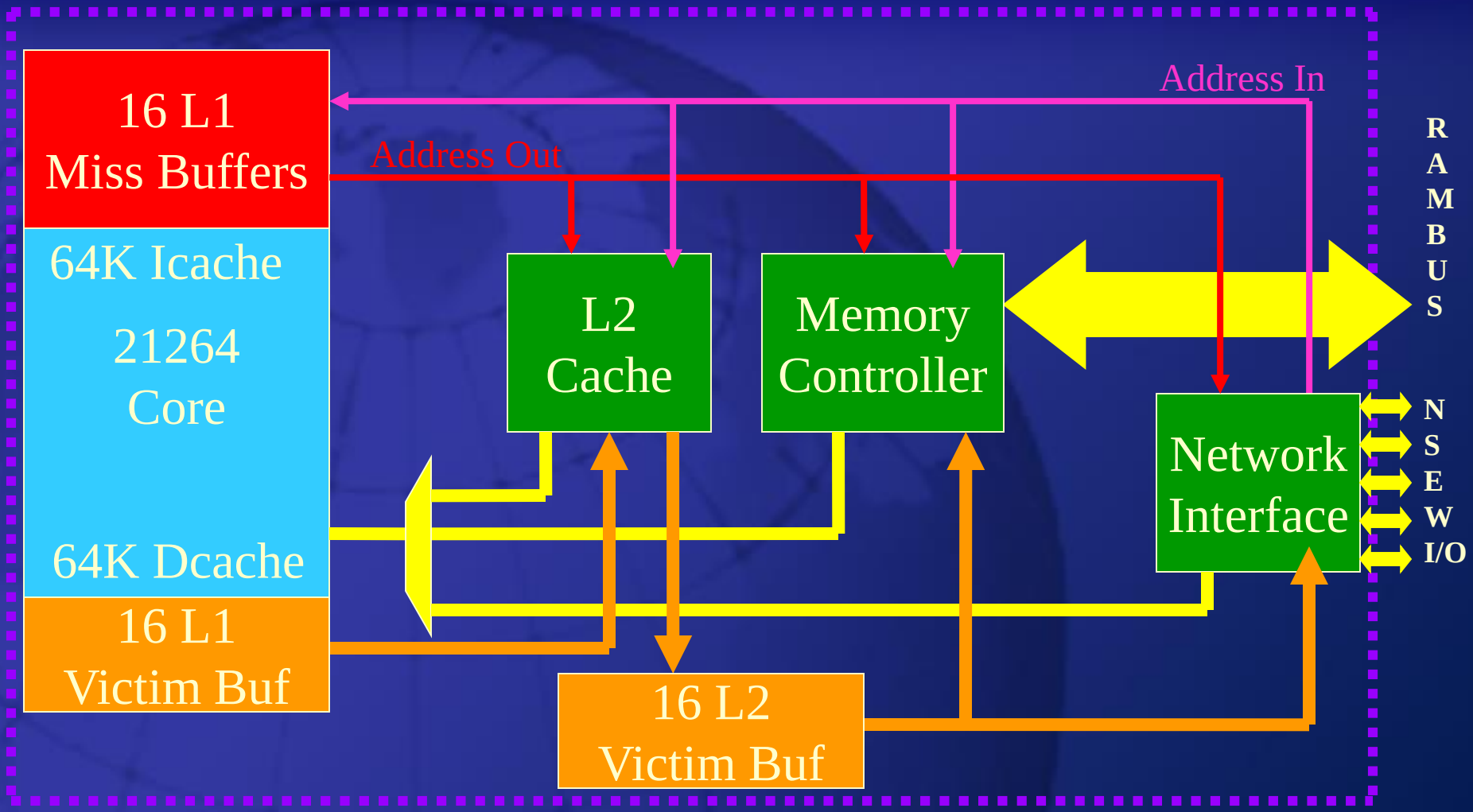
21364 Chip Block Diagram



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Integrated L2 Cache

- 1.5 MB
- 6-way set associative
- 16 GB/s total read/write bandwidth
- 16 Victim buffers for L1 -> L2
- 16 Victim buffers for L2 -> Memory
- ECC SECDED code
- 12ns load to use latency

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Integrated Memory Controller

- Direct RAMbus
  - High data capacity per pin
  - 800 MHz operation
  - 30ns CAS latency pin to pin
- 6 GB/sec read or write bandwidth
- 100s of open pages
- Directory based cache coherence
- ECC SECDED

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Integrated Network Interface

- Direct processor-to-processor interconnect
- 10 GB/second per processor
- 15ns processor-to-processor latency
- Out-of-order network with adaptive routing
- Asynchronous clocking between processors
- 3 GB/second I/O interface per processor

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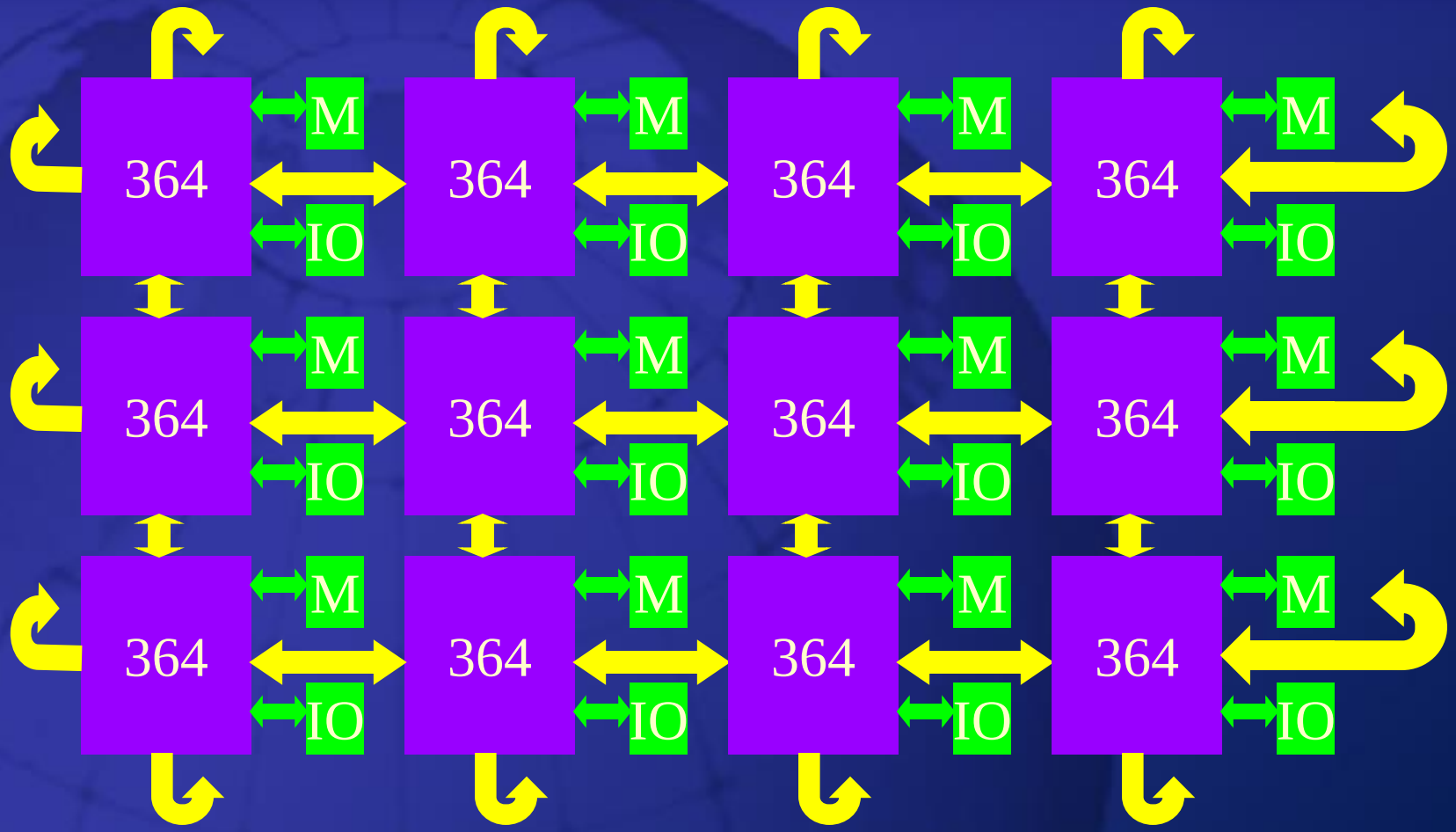
21364 System Block Diagram



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Alpha 21364 Technology

- 0.18 μm CMOS
- 1000+ MHz
- 100 Watts @ 1.5 volts
- 3.5 cm^2
- 6 Layer Metal
- 100 million transistors
  - 8 million logic
  - 92 million RAM

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