The AMD Am286™ZX Microprocessor

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Abstract: The introduction of the IBM Personal Computer created one of the largest industries in the electronics world. Since then, innovative design methodologies have been used to create smaller, faster, and cheaper PCs. The advent of "chip sets" which integrated commonly used peripheral functions, fueled this industry to greater heights, allowing smaller and faster machines to be built. In October 1990, AMD announced the Am286ZX integrated processor taking the integration to a new level. The Am286ZX integrated processor integrates the 80C286 CPU along with all the other logic functions into one piece of silicon, literally making the Am286ZX integrated processor a "PC-AT motherboard on a chip." This paper describes all the functions of the Am286ZX integrated processor and shows how to design a PC-AT motherboard using the Am286ZX integrated processor.

1.0 Introduction

AMD has been a source for the 80C286 microprocessor and most of the peripheral chips that are required to design a PC-AT motherboard for several years. The next logical step was to put all these devices on one piece of silicon and produce the world's first integrated PC-AT motherboard on a chip, the Am286ZX integrated processor.

The following functions have been integrated into the device:

- Static 80C286 microprocessor core
- Counter/Timer (82C54)
- DMA controllers (Am95C17/8237)
- Interrupt controllers (82C59)
- Real Time Clock (RTC) with 114 bytes of static RAM
- Enhanced clock generator
- Enhanced bus controller
- Advanced DRAM controller with full EMS 4.0 support
- DRAM Refresh controller
- Fast Reset and Fast GateA20
- Direct connect interfaces to the Industry Standard Architecture (ISA) system
- Direct 80C287 Co-processor interface
- Bus master mode

The Am286ZX device has a companion part called the Am286LX. Both the parts are identical except for the fact that the power saving features, which include the stop clock (static) modes and staggered and slow refresh for DRAMs, are tested and guaranteed in the Am286LX device.

2.0 Functional Description

Figure 1 shows a block diagram of the Am286ZX integrated processor.

The device has three major functional blocks:

1) 80C286 and standard peripherals
2) System control logic
3) External interfaces

2.1 80C286 and Standard Peripherals

2.1.1 CPU (80C286)

The core of the Am80C286 CPU has been integrated into the Am286ZX device. This includes the full instruction set, addressing space, memory organization, and operating modes of the Am80C286. The device is a completely static design, meaning that the CPU clock can be stopped anytime and the complete state is maintained and restored when the clock is re-started. Since the device is implemented in CMOS, the potential for power savings is substantial.

2.1.2 Counter/Timer

A three-channel, general purpose, 8254-compatible 16-bit counter/timer is integrated into the Am286ZX processor. This timer is programmed to produce features like the system timer tick, speaker output, and refresh request.

2.1.3 DMA Controllers

Two identical 9517/8237-compatible DMA controllers and a page register are integrated into the Am286ZX processor allowing data transfers between memory and I/O to be performed between CPU cycles without CPU participation, reducing data transfer latency.

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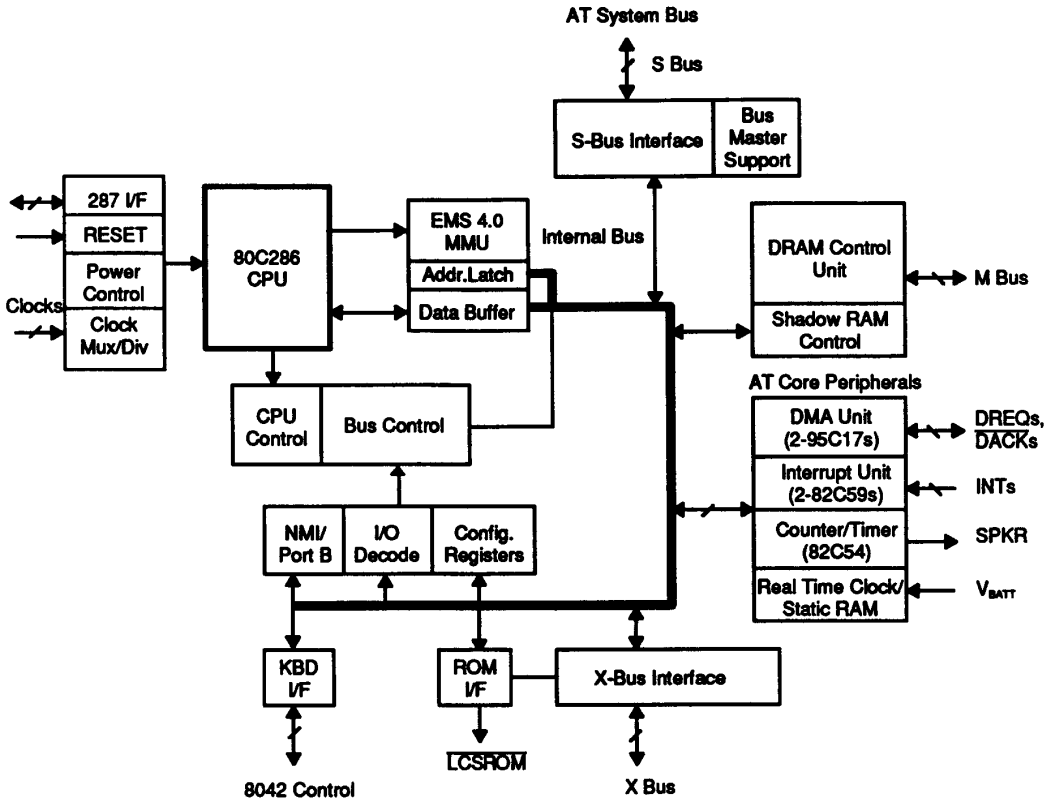


Figure 1: Block Diagram of the Am286ZX Integrated Processor.

2.1.4 Interrupt Controllers

Two 8259-compatible interrupt controllers have been integrated into the Am286ZX processor and are cascaded to prioritize up to 15 completely asynchronous events. Interrupt controllers allow external peripherals to request CPU intervention only when the peripherals require CPU processing, freeing up the CPU from constantly monitoring peripheral events.

2.1.5 RTC and CMOS RAM

The Real Time Clock (RTC) combines a complete time-of-day clock with alarm, a one-hundred-year calendar, a programmable periodic interrupt, and 114 bytes of static RAM. The device not only serves the obvious function of keeping the system time, but also of storing the system's configuration and other non-volatile information when the system is turned off.

2.2 System Control Logic

2.2.1 Enhanced Clock Generator

The Am286ZX processor provides a very flexible clock generator. The CPU, AT Bus, Keyboard controller and the 80C287 clocks can be individually selected by programming a configuration register. Figure 2 shows that each of the clocks has multiple sources and dividers available to it. The configuration register may be changed dynamically to meet a systems constantly changing needs achieving considerable power savings.

2.2.2 Enhanced Bus Controller

Figure 3 provides a block diagram of the bus control circuitry. This circuitry controls the routing of the address and data appropriately through the Am286ZX device. In addition, the device can be programmed to have the peripherals reside on the AT system bus (SBUS) or the local expansion bus (XBUS).

2.2.3 Advanced DRAM Controller and EMS Support

The Am286ZX integrated processor connects directly to DRAM modules, providing zero or near zero waitstate performance, while maintaining low system cost with inexpensive, slower DRAMs.

Four 16-bit (plus parity) banks of DRAM are supported. They can be implemented using 256-Kbit, 1-Mbit, or 4-Mbit DRAMs for a maximum of 8 Mb per bank, with 16 Mb total for all

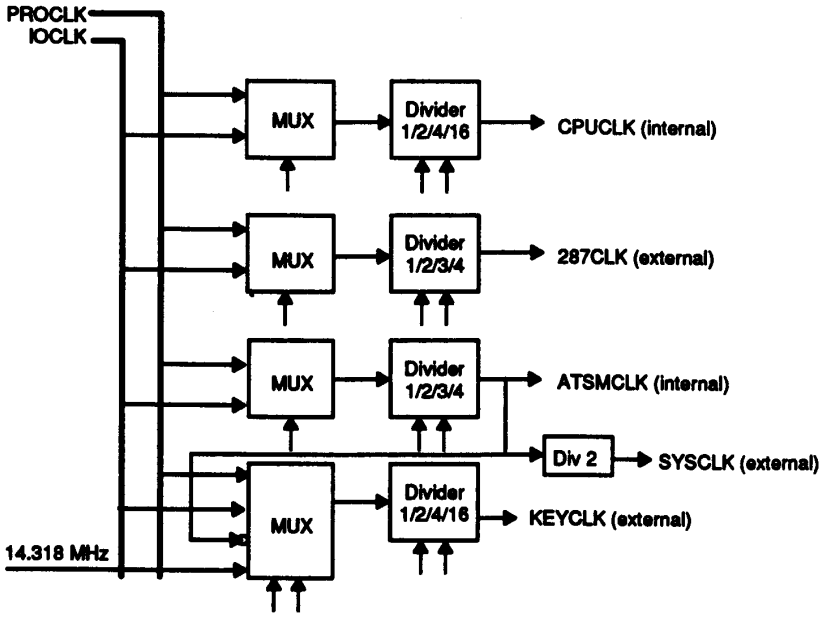


Figure 2: Clock Generator Block Diagram.

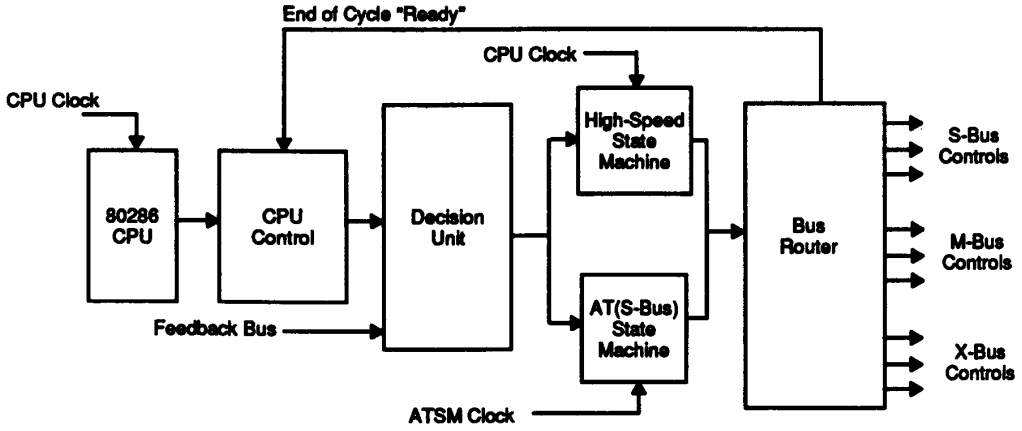


Figure 3: Bus Controller Block Diagram.

banks. Each bank can contain any mix of the above DRAM configurations. If adjacent arrays are populated with the same DRAM size, two and four way interleave access may be selected to increase the page-mode hit ratio.

In the LX version the standard RAS-only-refresh has been implemented and enhanced with both slow and staggered refresh options. These options help reduce the large power requirement associated with the continual recharging ("refreshing") needed by a DRAM to retain its contents.

The device has an Address Translation Memory Manager which allows global memory mapping and relocation. This allows the device to provide full hardware support for LIM EMS 4.0. Two full sets of 64 EMS registers have been provided to allow for quick task switching by multitasking EMS software.

In the DRAM Control Unit separate relocation registers are provided which allows the slow EPROM based BIOS to be "Shadow" mapped into fast DRAM system memory and

executed from the DRAM. The device also allows the 384 kb memory above the 640 kb base memory to be relocated to addresses starting at 1 Mb to provide extended or expanded memory. See Figure 4.

2.2.4 Fast RESET and Fast GATEA20

The Am286ZX processor provides two features which enhance the system's ability to switch from protected to real mode: Fast RESET and Fast GATEA20. In most existing systems this is handled by the slow keyboard controller.

2.2.5 ISA Interface

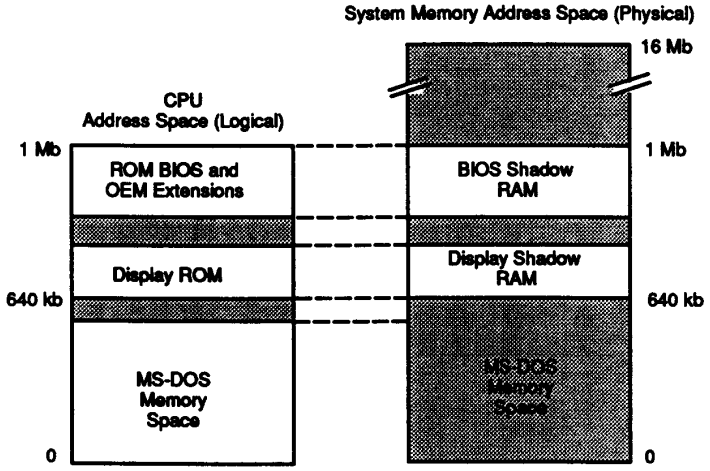
The Am286ZX processor will directly interface to the standard ISA system bus (SBUS) with no additional logic required. The device can be programmed to provide a synchronous SBUS clock or a separate oscillator may be used so that the integrated processor can run at the maximum clock speed while the SBUS runs at a slower asynchronous speed.

2.2.6 Co-processor Interface

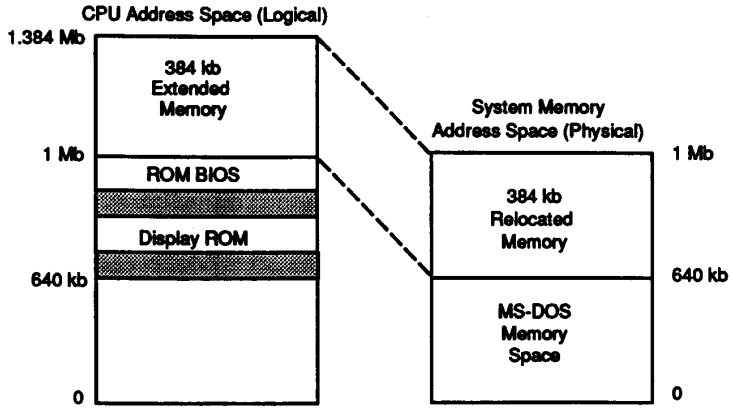
The Am286ZX processor provides all the signals required to connect an 80C287 math co-processor. It also provides the clock required by the 80C287.

2.2.7 Bus Master Mode

The device directly supports ISA bus mastering. In other words, an intelligent bus master adaptor based on the Am286ZX device could have overlapping addresses between its local memory and the host memory. In the Bus master mode, the Am286ZX device will allow the accesses to be routed to the appropriate memory. With external logic, MCA, EISA and other system busses can be supported. Selecting



a. Shadowing the ROM into RAM



b. 384 kb Relocation

Figure 4: Shadow ROM/384 kb Relocation

bus mastering mode changes the operating mode (direction) of some of the ISA expansion bus pins to allow the integrated processor to directly connect to the expansion bus of another system.

2.3 External Interfaces

All the external interfaces of the Am286ZX integrated processor are designed for direct connection. This means that to interface the Am286ZX integrated processor to a standard AT-architecture system, no external "glue logic" is needed. The Am286ZX processor will control the additional devices (DRAM, Keyboard controller, AT expansion bus peripherals, etc...) needed to complete a system without the space consuming driver chips common in today's systems.

The Am286ZX integrated processor provides support for both 8-bit and 16-bit EPROM configurations. This space can be defined by the user to be as large as 256 kb. The ability to write to the EPROM space has been added in order to support the new FLASH type memories.

In addition to the EPROM and keyboard controller, the integrated processor's X Bus can be used to attach other I/O devices. Eight configuration registers are available to map any 8-byte I/O address range onto the X Bus. Sixteen-bit I/O is also supported on the X Bus. Any I/O devices such as serial ports, parallel ports, floppy disk controllers, and hard disk controllers may be attached to the X Bus. Any of the four 8-bit DMA channels (0-3) can be mapped to the X Bus as well.

3.0 Designing with the Am286ZX Integrated Processor

The Am286ZX device is so highly integrated, that the design effort becomes minimal as can be seen in Figure 5. In addition to the Am286ZX processor the basic AT motherboard requires an EPROM, 8042 type keyboard controller, DRAM modules, oscillators and an optional math co-processor. All of these devices connect directly to the Am286ZX device. The only additional device required is a delay line for non CPU memory accesses. The device will also drive two expansion slots directly.

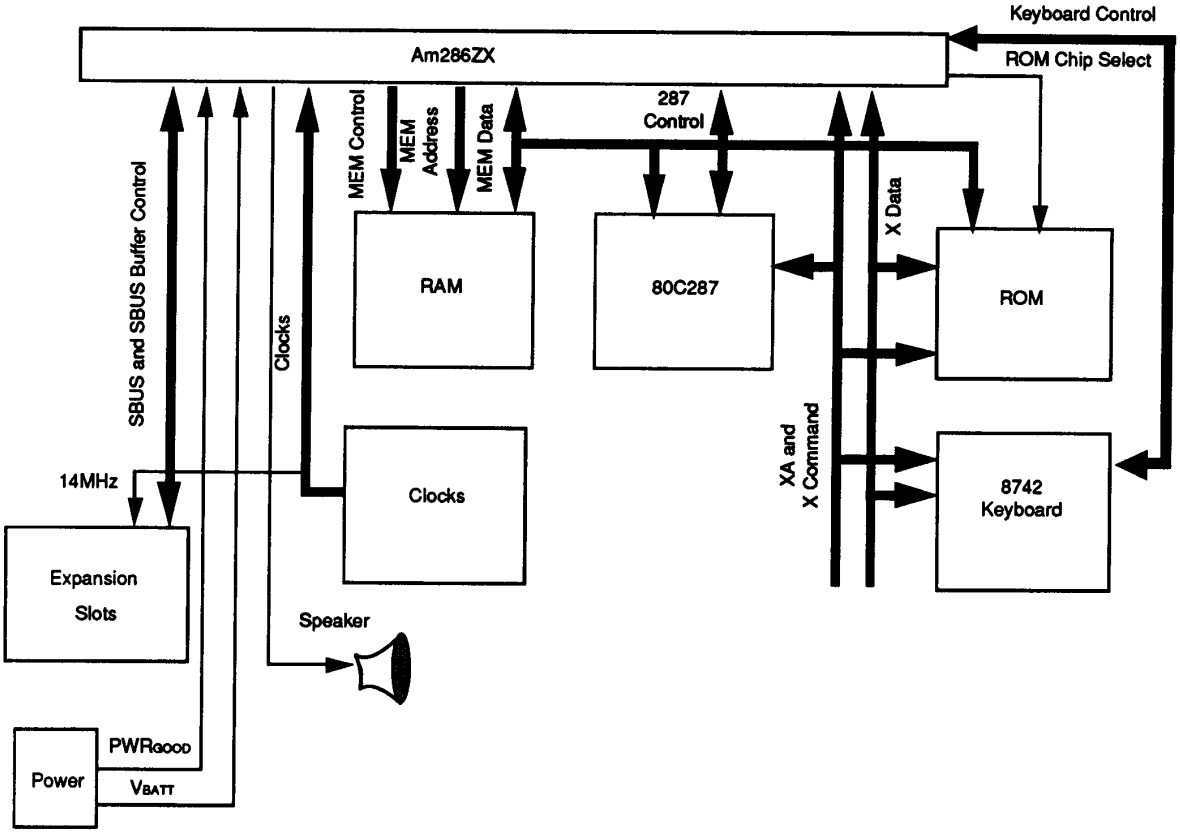


Figure 5: Block Diagram for AT Motherboard

References

[1] Advanced Micro Devices, *Am286ZX* datasheet , Austin Texas

[2] Douglas Gephardt and Mark Klonower, "Destination Laptop: The integrated processor," *Byte* Feb 1991