

μCOM-44 SINGLE CHIP MICROCOMPUTER

DESCRIPTION The μPD651 is a CMOS version of the μCOM-44. It features a single +5 volt power supply, a 2 mA (max), 800 μA (typ) current drain and extended temperature range. As a μCOM-44, it includes 1000 x 8 ROM, 64 x 4 RAM and 35 I/O lines in a 42 pin plastic dual-in-line package.

ABSOLUTE MAXIMUM RATINGS*	Operating Temperature	-30°C to +85°C
	Storage Temperature	-55°C to +125°C
	Supply Voltage	-0.3 to +7.0 Volts
	Input Voltages	-0.3 to +7.0 Volts
	Output Voltages	-0.3 to +7.0 Volts
	Output Current (Each Output Bit)	2.5 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

*T_a = 25°C

DC/AC CHARACTERISTICS

T_a = -30°C to +85°C, V_{CC} = +5V ± 10%.

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input High Voltage	V _{IH}	0.7V _{CC}		V _{CC}	V	Ports A to D, \overline{INT} , RES
Input Low Voltage	V _{IL}	0		0.3V _{CC}	V	Ports A to D, \overline{INT} , RES
Input Leakage Current High	I _{LIH}			+10	μA	Ports A and B, \overline{INT} , RES (V _I = V _{CC})
Input Leakage Current Low	I _{LIL}			-10	μA	Ports A and B, \overline{INT} , RES (V _I = 0V)
I/O Leakage Current High	I _{IOH}			+10	μA	Ports C and D (V _I = V _{CC})
I/O Leakage Current Low	I _{IOL}			-10	μA	Ports C and D (V _O = 0V)
Output High Voltage 1	V _{OH1}	V _{CC} -0.5			V	Ports C and D (I _{OH} = -1 mA)
		V _{CC} -0.5			V	Ports E to I (I _{OH} = -1 mA)
Output High Voltage 2	V _{OH2}	V _{CC} -2.5			V	Ports C to I (I _{OH} = -2 mA)
Output Low Voltage	V _{OL1}			0.6	V	Ports E to I (I _{OL} = 2 mA)
				0.4	V	Ports E to I (I _{OL} = 1.2 mA)
Supply Current	I _{CC}		0.8	2.0	mA	
Clock High Voltage	V _{φH}	0.7V _{CC}		V _{CC}	V	CLO, Ext. Clk.
Clock Low Voltage	V _{φL}	0		0.3V _{CC}	V	CLO, Ext. Clk.
Clock Leakage Current High	I _{LφH}			200	μA	CLO, Ext. Clk. (V _{OH} = V _{CC})
Clock Leakage Current Low	I _{LφL}			-200	μA	CLO, Ext. Clk. (V _{OL} = 0V)
Clock Frequency	f	150		440	KHz	
Clock Rise and Fall Times	tr, tf	0		0.3	μs	Ext. Clk.
Clock Pulse Width	t _{φW}	0.5		5.6	μs	Ext. Clk.

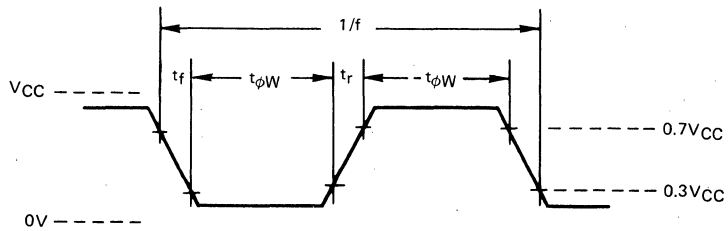
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μ PD651

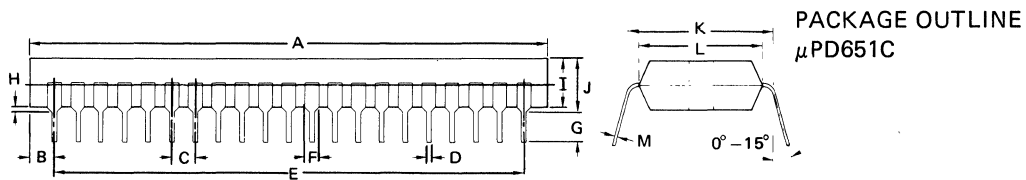
T_a = -30°C to +85°C, V_{CC} = +5V ± 10%.

CAPACITANCE

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance	C _I			15	pf	f = 1 MHz
Output Capacitance	C _O			15	pf	
I/O Capacitance	C _{IO}			15	pf	



CLOCK WAVEFORM



PACKAGE OUTLINE μPD651C

ITEM	MILLIMETERS	INCHES
A	56.0 MAX	2.2 MAX
B	2.6 MAX	0.1 MAX
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	50.8	2.0
F	1.5	0.059
G	3.2 MIN	0.126 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.20 MAX
J	5.72 MAX	0.22 MAX
K	15.24	0.6
L	13.2	0.52
M	0.3 ± 0.1	0.01 ± 0.004