MELPS4MICROCOMPUTERS

4

M58840-XXXP,M58841-XXXSP

SINGLE-CHIP 4-BIT MICROCOMPUTER WITH 8-BIT A/D CONVERTER

DESCRIPTION

The M58840-XXXP and M58841-XXXSP are single chip 4-bit microcomputers developed using p-channel aluminum gate ED-MOS technology and are housed in 42-pin plastic DIL packages. These single-chip microcomputers feature a built-in 8-bit A-D converter.

Differences between the M58840-XXXP and M58841-XXXSP.

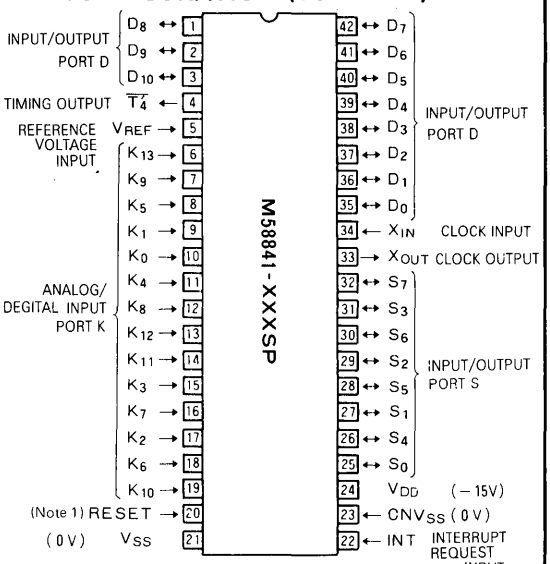
M58840-XXXP	Pin 5 is used as both the V_{REF} input and RESET input
M58841-XXXSP	The V_{REF} input pin and RESET input pin are separate, with pin 20 being used as the RESET input. Therefore, port K is a 14-bit port.

Except for the above differences, unless otherwise noted, the M58840-XXXP is the same as the M58841-XXXSP.

FEATURES

- Basic machine instructions 68
- Basic instruction execution time (1-word instruction at a clock frequency of 600kHz) 10μs
- Memory capacity: ROM ..... 2048 words x 9 bits
  RAM ..... 128 words x 4 bits
- Single −15V power supply
- Built-in A/D converter (14 or 15 analog inputs)
- 2 built-in data pointers
- Analog/digital input (port K):
  M58840-XXXP ..... 15 inputs
  M58841-XXXSP ..... 14 inputs
- Input/output port (ports D and S) ..... 19 lines
- Direct drive for large fluorescent display tubes is possible
- Interrupt function ..... 1 factor 1 level

PIN CONFIGURATION (TOP VIEW)



Outline 42P4B (M58841-XXXSP)
42P1 (M58840-XXXP)

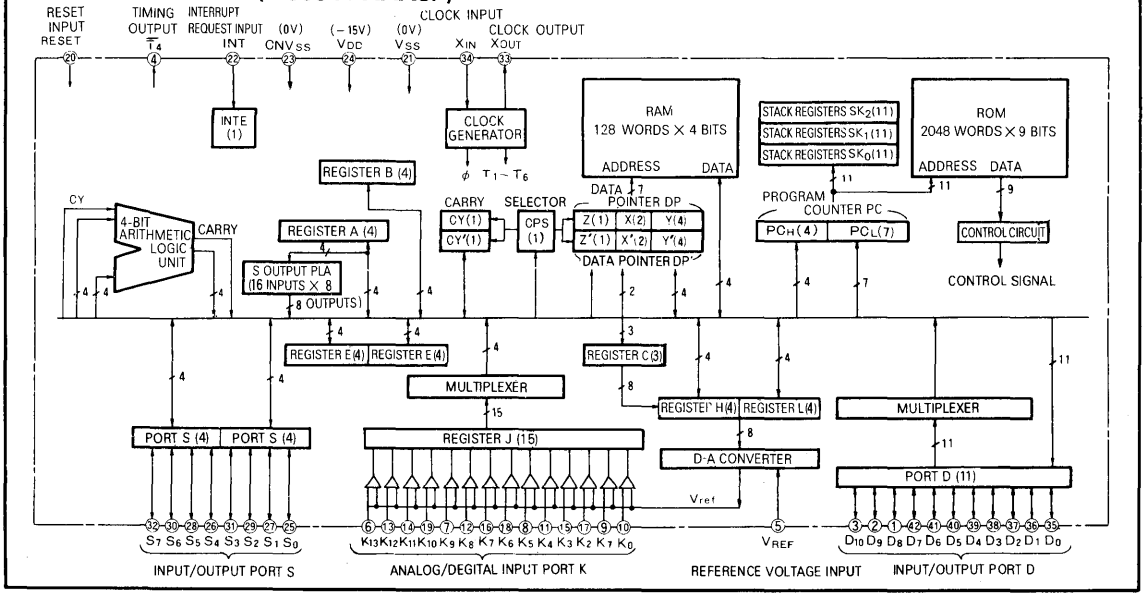
Note 1. Pin 20 is the port K K_{14} pin for the M58840-XXXP.

- Built-in decoder PLA for port S output (mask option)
- On-chip clock generator

APPLICATIONS

- Microwave ovens, air conditioners, heaters, washing machines, home sewing machines
- Office equipment, copying machines, medical equipment

BLOCK DIAGRAM (M58841-XXXSP)



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PERFORMANCE SPECIFICATIONS

Parameter			Performance	
			M58840-XXXP	M58841-XXXSP
Basic machine instructions			68	68
Instruction execution time (1-word instruction)			10μs	10μs
Clock frequency			300～600kHz	300～600kHz
Memory capacity	ROM		2048 words x 9 bits	2048 words x 9 bits
	RAM		128 words x 4 bits	128 words x 4 bits
I/O port	K	Input	1 bit x 15	1 bit x 14
	S	Output	8 bits x 1	8 bits x 1
		Input	4 bits x 2	4 bits x 2
	D	Output	1 bit x 11	1 bit x 11
		Sense input	1 bit x 11	1 bit x 11
A/D conversion circuit			Built-in (accuracy ± 2LSB)	Built-in (accuracy±2LSB)
RESET input			Common with V_{REF} pin	Independent RESET pin
Subroutine nesting			3 levels (including one level of interrupt)	3 levels (including one level of interrupt)
Clock generator			Built-in (externally connected RC circuit or ceramic resonator)	Built-in (externally connected RC circuit or ceramic resonator)
I/O characteristics of ports	I/O withstanding voltage		−33 V	−33V
	Port S output current		−8mA	− 8 mA
	Port D output current		−15mA	−15mA
Supply voltage	V_{DD}		−15V (typ)	−15V (typ)
	V_{SS}		0 V	0 V
Device structure			p-channel aluminum gate ED-MOS	P-channel aluminum gate ED-MOS
Package			42-pin plastic molded DIL	42-pin shrink plastic molded DIL
Power dissipation (exluding ports)			400mW (typ)	400mW (typ)

PIN DESCRIPTION

Pin	Name	Input or output	Function
V_{DD} V_{SS}	Power supplies	In	V_{DD} and V_{SS} are applied as −15V±10% and 0V respectively
K_0 ～ K_{13}	Input port K	In	The input port K consists of 14 (15 for the M58840-XXXP) independent analog input pins. They can be programmed to receive digital quantities as well.
S_0 ～ S_7	Input/output port S	In/out	The I/O port S can be used as either an 8-bit output port or a pair of 4-bit input ports. Since it has open drain circuits, it is suitable for directly driving segments of a large fluorescent display tube. When the output port S is programmed to a low level, it remains in the floating state (high-impedance) so that it can be used as an input port.
D_0 ～ D_{10}	Input/output port D	In/out	The I/O port D is composed of 11 bits that can be used as independent I/O bits. When the port D outputs are programmed to a low level, the output remains in the floating state (high-impedance) and the input signal level is sensed.
X_{IN}	Clock input	In	A clock generator is built into the device so that the clock frequency is determined by connecting an external RC circuit or ceramic resonator between pins X_{IN} and X_{OUT}. When an external clock source is used, it should be connected to the X_{IN} pin, leaving the X_{OUT} pin open.
X_{OUT}	Clock output	Out	This pin is the output of the built-in clock generator circuit. The oscillation frequency is controlled by connecting an RC circuit or ceramic resonator element between this pin and the X_{IN} pin.
INT	Interrupt request input	In	This pin is used to input the interrupt request signal. The level of the interrupt signal can be programmed as either high or low.
$\overline{T_4}$	Timing output	Out	This is the basic timing output. It is used for testing and should be connected to V_{SS} (0V).
V_{REF}	Reference voltage input	In	This is the input for the reference voltage applied to the D-A converter. For the M58840-XXXP it serves as the RESET input pin as well.
CNV_{SS}	CNV_{SS} input	In	This input is connected to V_{SS} and must have a high-level input applied to it (0V).
RESET	Reset input	In	This is the reset input pin for the M58841-XXXSP. The reset state is enabled when it is kept high for at least two machine cycles.

BASIC FUNCTION BLOCKS

Program Memory (ROM)

This 2048-word x 9-bit mask programmable ROM can be programmed with machine instruction codes in accordance with the customer's specifications. It consists of 16 pages, each containing an address range of 0 ~ 127. Fig. 1 shows the address map of this ROM.

Program Counter (PC)

This counter is used to specify ROM addresses and the sequence of read-out of instructions stored in ROM. The program counter (PC) is an 11-bit counter, the upper order 4 bits of each (PC_H) indicate the ROM page, and the lower order 7 bits (PC_L) of which are a pure binary address designation. Each time an instruction is executed, PC_L is incremented by one step. For branching, subroutine call instructions and return instructions, its value is set to the designated address.

When the 127th address is reached for every page, the address value returns to the first address of that page. Therefore, for moving from one page to another page, the page byte itself must be modified. This is done using the BL and BLA instructions.

Page 14 and page 15 are special pages used for subroutine calls. The page 14 subroutine can be called with a one word instruction from any arbitrary page. This instruction is either BM or BMA. When either BM or BMA is executed, subsequent BM or BMA instructions are equivalent to B and BA on page 14. Also, B or BA is equivalent to B or BA on page 15. This condition is cancelled when the RT, RTS, BL, BML, BLA or BMLA instruction is executed. Table 3 shows the instruction codes and corresponding states.

Stack Registers (SK_0, SK_1, SK_2)

These registers are used to temporarily store the contents of the PC while executing subroutines or interrupt programs until the program returns to its main routine. The SK registers are organized in three words of 11 bits each, enabling up to three levels of subroutine nesting. If one level is used for an interrupt routine, the remaining two levels can be used for subroutine calls.

Data Memory (RAM)

This 512-bit (128 words x 4 bits) RAM is used to store both processing and control data. One RAM word consists of 4 bits with bit manipulation possible over the entire storage area. The 128 words are arranged as 2 file groups x 4 files x 16 digits x 4 bits. Fig. 2 shows the RAM address map.

The RAM address specification is made by the combination of data pointer DP (register Z, register X and register Y.) Thus, the selector CPS and data pointer DP must be set. However, as long as the address is not changed this is not necessary.

Data Pointers (DP, DP')

These registers are used to designate RAM address, and bit positions for the I/O port D and register J. Each data pointer is composed of a 7-bit register. Register Z (the most significant bit of DP) designates the RAM file group; register X (the central 2 bits) designates a RAM file; and register Y (the least significant 4 bits) designates the digit position of the RAM file. At the same time, register Y designates bit positions of the I/O port D and register J.

4-bit Arithmetic Logic Unit (ALU)

This unit executes 4-bit arithmetic and logical operations by means of a 4-bit adder and related logic circuitry. The arithmetic logic unit performs subtraction, addition, logical comparisons, arithmetic comparisons, and bit manipulation.

Register A and Carry flag (CY)

Register A is a 4-bit accumulator that constitutes the basis for arithmetic operations. Data processing operations such as arithmetic and logical operations, data transfer, exchange, conversion and data input/output are executed by means of this register. Overflow of register A is stored in the carry flag's CY or CY' after execution of arithmetic or logical operations. The carry flags can also be used as 1-bit flags. Carry flags and data pointer DP selection is done by means of the selector CPS.

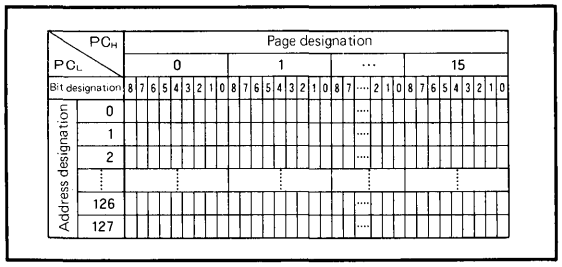

Fig. 1 ROM Address map

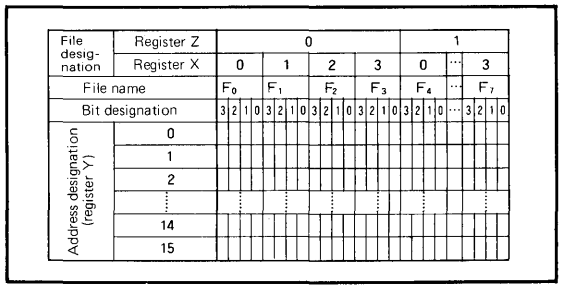

Fig. 2 RAM Address map

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Registers B and E

Register B is composed of 4 bits and can be used as a 4-bit temporary storage register or for 8-bit data transfer in conjunction with register A. Register E is composed of 8 bits and is used not only as an 8-bit temporary storage register, but also as a temporary storage register for I/O port S.

A/D Conversion Circuit

The following A/D conversion functions are controlled by software as described below. Fig. 3 shows the block diagram.

(1) Comparators

These comparators are implemented entirely with PMOS devices and use a chopper-type amplification method. They are capable of determining the difference of the D/A converter output Vref and the port K input signals $V_{K(Y)}$ (where Y=0~13).

(2) Register J

Register J is composed of 14 1-bit registers, each representing the comparison result from the comparators. All register bits are set simultaneously. The value of the register J with respect to the comparison results is as follows.

1 when $|V_{ref}| > |V_{K(Y)}|$

0 when $|V_{ref}| < |V_{K(Y)}|$

In this relationship(Y) represents the bit position in register J which is designated by register Y. The comparison results can be checked for each bit using the SZJ instruction.

(3) Registers H and L

These two 4-bit registers are capable of transferring and exchanging data to and from register A. The 8-bit digital data for the D-A converter is transferred from these registers, the higher order 4 bits from H and lower order 4 bits from L.

(4) Register C

This 3-bit register is used as a counter to designate bit positions in the H and L registers.

(5) D/A Converter

The D/A converter converts the digital values stored in the registers H and L, referencing with the external reference voltage V_{REF} applied at the pin V_{REF}, to the analog value of the internal reference voltage Vref. The theoretical value of the internal reference voltage V_{ref} is defined as follows.

$$V_{ref} = \frac{n - 0.5}{256} \times V_{REF}$$

where n = 1, 2, ... 255

V_{ref}=0 where n=0

In the above relationships n is the value weighted accorded to the contents of registers H and L.

A/D Conversion Algorithms

A/D conversion is controlled by the programming of the previously described functional blocks. Thus, by modifying the program either the successive approximation method or the sequential comparison method may be selected. In addition, a digital input of high or low level may be used to select the method, eliminating software selection of the A/D conversion technique.

(1) Successive Approximation Method

In this method, a constant conversion speed is maintained regardless of the amplitude of the analog signal. The A/D conversion process requires 0.6ms (at 600kHz clock frequency). 12 program words are required.

(2) Sequential Comparison Method

In this method the conversion speed varies in accordance with the rate of change of the analog quantity. When the rate of change is slow, the conversion rate increases. 30 program words are required.

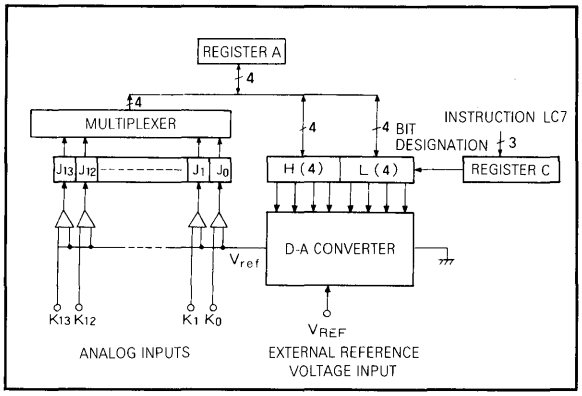

Fig. 3 A/D Conversion circuit block diagram

Interrupt Function

The flag INTE is a 1-bit flip-flop used to control interrupt operation. When an interrupt request signal is applied to the pin INT while the interrupt is enabled, the INTE flag is reset to disable further interrupts, after which the program jumps from the main program to address 0 of page 12. When an interrupt program is used, one level of the three-level stack register is required, the remaining two levels being used for subroutines. After the interrupt program is started, the data pointer DP, register A, carry flag CY, and registers used by the interrupt program must be saved and these must be restored before returning to the main program. The returning may be done by the execution of RTI instruction.

When an interrupt occurs, the microcomputer internal states are as follows.

(1) Program Counter

The current address in the main program is stored in a stack register and the program counter is set to page 12, address 0.

(2) Interrupt Flag INTE

The flag INTE is reset to disable further interrupts. This disabled state will continue even after the program has returned from the interrupt routine to the main program by the execution of the RTI instruction. EI is executed and when the input level of the INT input changes, this state is disabled. Thus, when the INTH instruction is executed the interrupt state is enabled when the INT input goes high. As long as it remains in the high state, further interrupts are prohibited. If the INT input should change to a low level and return to high, the next interrupt will be accepted.

(3) Skip Flags

Skip flags are provided for skip instructions and consecutively described instructions and these skip flags discriminate the skip and non skip conditions. Each flag has its own stack within which the skip state is saved.

As a mask option, the interrupt pin may be provided with Schmitt input circuits.

Input/Output Pins

(1) Input port K

The input port K consists of 14 pins (15 pins for the M58840-XXXP). The voltage level input at these pins is compared with the D-A converter output voltage Vref by a comparator and the results stored in register J. As a mask option, it is possible to build into the input port K load resistors. These are implemented using an enhancement-type (M58840-XXXP) or depletion-type (M58841-XXXSP) MOS transistors. In addition, to enable the use of capacitive touch-type keys, it is possible to provide these inputs with the required discharge transistors.

(2) Input/Output Port S

The input/output port S consists of 8 bits, each bit with an output latch. These latches are used to store data transferred by means of a PLA from register A, or data transferred from register A or register B directly. 4 bits at a time of the 8 input bits of port S may be transferred to register A.

Because port S outputs are provided with a built-in PLA, it is possible to output any arbitrarily settable 8-bit code from 4 input bits specified by register A. These PLA output codes can be specified arbitrarily as a masked option.

(3) Input/Output Port D

The input/output port D consists of 11 bits. Each bit can be individually designated as either input or output and is provided with its own latch. The contents of the data pointer register Y can be used to designate a single bit of port D for output or sensing.

When port S or port D is used as an input port, the output should first be cleared to the low state.

Reset Function

For the M58840-XXXP, when a power source satisfying the conditions shown in Fig. 4 is applied, an internal power-on reset function operates to reset the microcomputer. Cancelling of the reset state also is performed automatically, the program being started at page 0, address 0.

If the power-on reset function does not operate properly because of the trailing edge characteristics of the power supply, reset can be enabled by inputting a high level at the V_{REF} pin. Setting this V_{REF} pin to low starts the program at page 0, address 0.

For the M58841-XXXSP, if the RESET input is kept high for at least two machine cycles, the reset state is enabled. Because the M58841-XXXSP is provided with an internal charging transistor it requires only an external diode and capacitor as shown in Fig. 5.

For this configuration, when the supply voltage falls below −13.5V, the circuit design should ensure that the RESET input is above −4V.

When the reset state is enabled, the following operations are performed.

(1) The program counter is set to page 0, address 0 (PC) ← 0

(2) The interrupt mode is in the interrupt disabled state (INTE) ← 0

This is the same state as when the instruction DI is executed.

(3) By setting the interrupt request signal INT to high, the interrupt enabled state is entered. This is the same state as when the instruction INTH is executed.

(4) All outputs of port S are cleared to low (S) ← 0

(5) All outputs of port D are cleared to low (D) ← 0

(6) The carry and data pointer selector CPS is cleared to low to designate DP and CY (CPS) ← 0

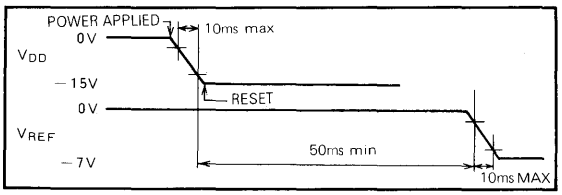

Fig.4 M58840-XXXP Power on reset

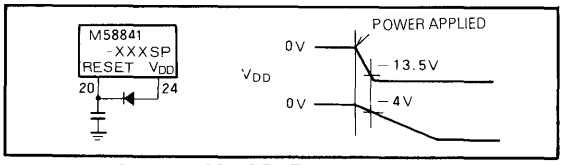

Fig.5 M58841-XXXSP Power on reset

Clock Generator Circuit

A clock generator circuit has been built-in to the M58840-XXXP and M58841-XXXSP, allowing control of the frequency by means of an externally connected RC circuit or ceramic resonator. In addition, an external clock signal may be applied at the X_{IN} pin, leaving the X_{OUT} pin open. Circuit examples are shown in Fig. 6 to Fig. 8.

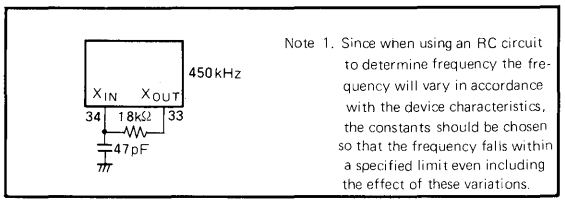

Fig. 6 External RC circuit

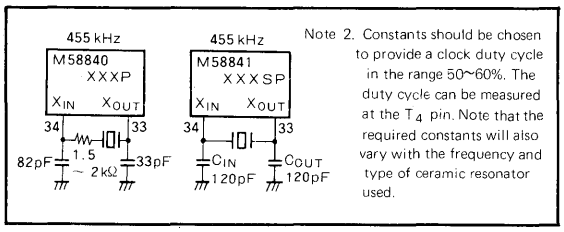

Fig. 7 Externally connected ceramic resonator

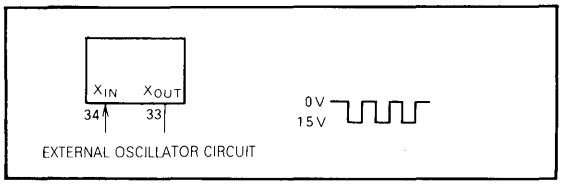

Fig. 8 External clock input circuit

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MACHINE INSTRUCTIONS

Type of instruction	Mnemonic	Instruction code D_8 $D_7D_6D_5D_4$ $D_3D_2D_1D_0$	16 mal notation	Skip conditions	No. of cycles	Functions	Skip conditions	Flag CY	Description of operation
RAM addresses	LXY x,y	0 11xx yyyy	0 C(y)+(x)	1	1	(X)←x, where, x=0~3 (Y)←y, where, y=0~15	Written successively	X	Loads value of "x" into register X, and of "y" into Y. When LXY is written successively, the first is executed and successive ones are skipped
	LZ z	0 0100 101z	0 4A+(z)	1	1	(Z)←z, where, z=0, 1		X	Loads value of "z" into register Z.
	INY	0 0000 0010	0 02	1	1	(Y)←(Y)+1	(Y)=0	X	Increments contents of register Y by 1. Skips next instruction when new contents of register Y are "0".
	DEY	0 0000 0011	0 03	1	1	(Y)←(Y)−1	(Y)=15	X	Decrements contents of register Y by 1. Skips next instruction when new contents of register Y are "15".
	LCPS i	0 0100 000i	0 4i	1	1	(CPS)←i, where, i=0, 1	–	X	DP and CY are active when i=0, DP' and CY', when i=1.
Register-to-register transfers	TAB	0 0001 1110	0 1E	1	1	(A)←(B)	–	X	Transfers contents of register B to register A.
	TBA	0 0001 1100	0 1C	1	1	(B)←(A)	–	X	Transfers contents of register A to register B.
	TAY	0 0001 1101	0 1D	1	1	(A)←(Y)	–	X	Transfers contents of register Y to register A.
	TYA	0 0000 1100	0 0C	1	1	(Y)←(A)	–	X	Transfers contents of register A to register Y.
	TLA	0 0001 1001	0 19	1	1	(L)←(A)	–	X	Transfers contents of register A to register L.
	THA	0 0101 1001	0 59	1	1	(H)←(A)	–	X	Transfers contents of register A to register H.
	TEAB	0 0001 1010	0 1A	1	1	(E_7~E_4)←(B), (E_3~E_0)←(A)	–	X	Transfers contents of registers A and B to register E.
	TEPA	0 0001 0110	0 16	1	1	(E_7~E_0)←through PLA←(A)	–	X	Decodes contents of register A in the PLA and transfers result to register E.
	TAJ	0 0000 1101	0 0D	1	1	(A)←($J_3J_2J_1J_0$) when, (Y_1Y_0)=0 (A)←($J_7J_6J_5J_4$) when, (Y_1Y_0)=1 (A)←($J_{11}J_{10}J_9J_8$) when, (Y_1Y_0)=2 (A)←(0 $J_{14}J_{13}J_{12}$) when, (Y_1Y_0)=3	–	X	Transfers designated contents of register J to register A.
	XAL	0 0001 1000	0 18	1	1	(A)↔(L)	–	X	Exchanges contents of register A with contents of register L.
	XAH	0 0101 1000	0 58	1	1	(A)↔(H)	–	X	Exchanges contents of register A with contents of register H.
RAM-accumulator transfers	TAM j	0 0110 01jj	0 64+j	1	1	(A)←(M(DP)) (X)←(X)∀j, where, j=0~3	–	X	Transfers the RAM contents addressed by the active DP to register A. Register X is then "exclusive OR-ed" with the value j in the instruction, and the result stored in register X.
	XAM j	0 0110 00jj	0 6j	1	1	(A)↔(M(DP)) (X)←(X)∀j, where, j=0~3	–	X	Exchanges the contents of the RAM and register A. Contents of X are then "exclusive OR-ed" with the value j, and the result stored in register X.
	XAMD j	0 0110 10jj	0 68+j	1	1	(A)↔(M(DP)), (Y)←(Y)−1 (X)←(X)∀j, where, j=0~3	(Y)=15	X	Exchanges the contents of the RAM and register A. Contents of X are then "exclusive OR-ed" with the value j in the instruction, and the result stored in register X. The contents of register Y are decremented by 1, and when the result is 15, the next instruction is skipped.
	XAMI j	0 0110 11jj	0 6C+j	1	1	(A)↔(M(DP)), (Y)←(Y)+1 (X)←(X)∀j where, j=0~3	(Y)=masked skip condition	X	Exchanges the contents of the RAM and register A. Contents of X are then "exclusive OR-ed" with the value j in the instruction and result stored in register X. The contents of register Y are incremented by 1, and when the result meets with the marked skip condition the next instruction is skipped.
Arithmetic operations	LA n	0 1011 nnnn	0 Bn	1	1	(A)←n, where, n=0~15	Written successively	X	Loads the value n into register A. When LA is written consecutively the first is executed, and successive ones are skipped.
	AM	0 0000 1010	0 0A	1	1	(A)←(A)+(M(DP))	–	X	Adds the contents of the RAM to register A. The result is retained in register A, and the contents of flag CY are unaffected.
	AMC	0 0000 1110	0 0E	1	1	(A)←(A)+(M(DP))+(CY) (CY)←carry	–	0/1	Adds the RAM contents addressed by the active DP and contents of flag CY to register A. The result is stored in register A and the carry in the active flag CY.
	AMCS	0 0000 1111	0 0F	1	1	(A)←(A)+(M(DP))+(CY) (CY)←carry	(CY)=1	0/1	Adds the contents of the RAM and flag CY to register A. The result is stored in register A and the carry in the CY, but the next instruction is skipped when a carry is produced.
	A n	0 1010 nnnn	0 An	1	1	(A)←(A)+n, where, n=0~15	A carry ≠0 but n≠6	X	Adds value n in the instruction to register A. The contents of flag CY are unaffected and their next instruction is skipped if a carry is not produced, except when n=6.
	SC	0 0100 1001	0 49	1	1	(CY)←1	–	1	Sets active flag CY
	RC	0 0100 1000	0 48	1	1	(CY)←0	–	0	Resets active flag CY
	SZC	0 0010 1111	0 2F	1	1		(CY)=0	X	Skips next instruction when contents of the active flag CY are 0.
	CMA	0 1000 1111	0 8F	1	1	(A)←$\overline{(A)}$	–	X	Stores complement of register A in register A.
Bit operations	SB j	0 0100 11jj	0 4C+j	1	1	(Mj(DP))←1, where, j=0~3	–	X	Set the jth bit of the RAM addressed by the active DP (the bit designated by the value j in the instruction).
	RB j	0 0101 11jj	0 5C+j	1	1	(Mj(DP))←0, where, j=0~3		X	Resets the jth bit of the RAM addressed by the active DP (the bit designated by the value j in the instruction)
	SZB j	0 0010 00jj	0 2j	1	1		(Mj(DP))=0 where, j=0~3	X	Skips next instruction when the contents of the jth bit of the RAM addressed by the active DP (the bit which is designated by the value y in the instruction) are 0.
Compares	SEAM	0 0010 0110	0 26	1	1		(M(DP))=(A)	X	Skips next instruction when contents of register A are equal to the RAM contents addressed by the active DP.
	SEY y	0 0011 yyyy	0 3y	1	1		(Y)=y where, y=0~15		Skips next instruction when the contents of register Y are equal to the value j in the instruction.
A/D converter operations	LC7	0 0101 0111	0 57	1	1	(C)←7		X	Loads 7 to register C.
	DEC	0 0000 1001	0 09	1	1	(C)←(C)−1	(C)=7	X	Decrements contents of register C by 1, when result is 7, skips next instruction.
	SHL	0 0100 0010	0 42	1	1	(H(C1 C0))←1 when, (C_2)=1 (L(C1 C0))←1 when, (C_2)=0	–	X	Sets the bit in register L or H designated by register C. The box instruction shows the relationship between register C and bit position. (C) 7 6 5 4 3 2 1 0 / Bit H_3 H_2 H_1 H_0 L_3 L_2 L_1 L_0
	RHL	0 0101 0010	0 52	1	1	(H(C1 C0))←0 when, (C_2)=1 (L(C1 C0))←0 when, (C_2)=0	–	X	Resets the bit in register L or H that is designated by register C.
	CPA	0 0000 1000	0 08	1	1 (2)	(J(i))←1 when, $\|V_{ref}\| > \|V_{K(i)}\|$ (J(i))←0 when, $\|V_{ref}\| < \|V_{K(i)}\|$ i=0~14		X	Reads all analog values from input port K for comparison with D-A converter output V_{ref}, and either sets the respective bit of register J to the next instruction cycle, whenever $V_{ref} < V_{K(i)}$ is true, or resets it, whenever $V_{ref} < V_{K(i)}$ is true.
	CPAS	0 0101 0001	0 51	1	1	(J(i))←1 when, $\|V_{ref}\| > \|V_{K(i)}\|$ (J(i))←0 when, $\|V_{ref}\| < \|V_{K(i)}\|$ i=0~14	–	X	Reads and stores temporarily all analog values from the input port K, which are the unaffected by changes in port K inputs. These values are compared with the D-A converter output V_{ref} calculated from contents of registers H and L and respective bits of register J are set/reset.
	CPAE	0 0101 0000	0 50	1	1	Execution of the instruction CPAS is over, and no more changes will made in (J(Y)).		X	Terminates execution of instruction CPAS. Contents of register J remain unaffected, maintaining the value immediately before termination, and input port K is again ready to receive inputs.
	SZJ	0 0010 1001	0 29	1	1		(J(Y))=0 (Y)=15	X	Skips next instruction when the bit in register J, designated by register Y, is 0. The next instruction is unconditionally skipped when the contents of register Y are 15.

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Type of instruction	Mnemonic	Instruction code D8 D7D6D5D4 D3D2D1D0	16mal notation	Skip conditions	No. of cycles	Functions	Skip conditions	Flag CY	Description of operation
Jumps	B xy	1 1xxx yyyy	1 8y + x	1	1	(PCL)←16x+y	–	X	Jumps to address xy of the current page.
						(PCH)←15, (PCL)←16x+y			Jumps to address xy on page 15 when executed, provided that none of instructions RT, RTS, BL, BML or BMLA was executed after execution of instruction BM or BMA.
	BL pxy	0 0111 pppp 1 1xxx yyyy	0 7p 1 8y + x	2	2	(PCH)←p (PCL)←16x+y	–	X	Jumps to address xy of page p.
	BA xX	0 0000 0001 1 1xxx XXXX	0 01 1 8X + x	2	2	(PCL)←16x+(A)	–	X	Jumps to address x(A) of the current page.
						(PCH)←15, (PCL)←16x+(A)			Jumps to the address x(A) of page 15 provided that none of instructions RT, RTS, BL, BML, BLA or BMLA was executed after execution of instruction BM or BMA.
	BLA pxX	0 0000 0001 0 0111 pppp 1 1xxx XXXX	0 01 0 7p 1 8x + x	3	3	(PCH)←p (PCL)←16x+(A)	–	X	Jumps to the address x(A) of page p.
Subroutine calls	BM xy	1 0xxx yyyy	1 xy	1	1	(SK2)←(SK1)←(SK0)←(PC) (PCH)←14, (PCL)←16x+y	–	X	Calls for the subroutine starting at address xX on page 14.
						(PCH)←14, (PCL)←16x+y			Jumps to address xy of page 14 provided that none of instructions RT, RTS, BL, BML, BLA or BMLA was executed after the execution of instructions BM or BMA.
	BML pxy	0 0111 pppp 1 0xxx yyyy	0 7p 1 xy	2	2	(SK2)←(SK1)←(SK0)←(PC) (PCH)←p, (PCL)←16x+y	–	X	Calls for the subroutine starting at address xx of page P.
	BMA xX	0 0000 0001 1 0xxx XXXX	0 01 1 xX	2	2	(SK2)←(SK1)←(SK0)←(PC) (PCH)←14, (PCL)←16x+(A)	–	X	Calls for the subroutine starting at address x(A) of page 14.
						(PCH)←14, (PCL)←16x+(A)			Jumps to address x(A) of page 14 provided that none of instructions RT, RTS, BL, BML, BLA or BMLA was executed after the execution of instructions BM or BMA.
	BMLA pxX	0 0000 0001 0 0111 pppp 1 0xxx XXXX	0 01 0 7p 1 XX	3	3	(SK2)←(SK1)←(SK0)←(PC) (PCH)←p, (PCL)←16x+(A)	–	X	Calls for the subroutine starting at address x(A) of page p.
Program returns	RTI	0 0100 0110	0 46	1	1	(PC)←(SK0)←(SK1)←(SK2) Resets interrupt flip-flop	–	X	Returns from interrupt routine to main routin. The internal flip-flops is restored
	RT	0 0100 0100	0 44	1	1	(PC)←(SK0)←(SK1)←(SK2)	–	X	Returns to the main routine from the subroutine.
	RTS	0 0100 0101	0 45	1	2	(PC)←(SK0)←(SK1)←(SK2)	Unconditional skip	X	Returns to the main routine from the subroutine, and unconditionally skips the next instruction.
Input/output	SD	0 0001 0101	0 15	1	1	(D(Y))←1, where, (Z)=1, 0≦(Y)≦10	–	X	Sets the bit of port D that is designated by register Y, when the contents of register Z are 1.
	RD	0 0001 0100	0 14	1	1	(D(Y))←0, where, (Z)=1, 0≦(Y)≦10	–	X	Resets the bit of port D that is designated by register Y, when the contents of register Z are 1.
	SZD	0 0010 1011	0 2B	1	1	··· where, (Z)=1, 0≦(Y)≦10	(D(Y))=0	X	Skips the next instruction if the contents of the bit of port D that is designated by register Y are 0 and the contents of register Z are 1.
	OSAB	0 0001 1011	0 1B	1	1	(S7~S4)←(B), (S3~S0)←(A)		X	Outputs contents of register A and B to port S.
	OSPA	0 0001 0111	0 17	1	1	(S7~S0)←through PLA←(A)		X	Decodes contents of register A by PLA and the result is output to port.
	OSE	0 0000 1011	0 0B	1	1	(S)←(E)		X	Outputs contents of register E to port S.
	IAS i	0 0101 010i	0 54 + i	1	1	i=0 : (A)←(S7~S4) i=1 : (A)←(S3~S0)		X	Transfers from port S to register A. The high-order four bits of port S are transferred when the value of i in the instruction is 0 or the low-order four bits are transferred when the value of i is 1.
	CLD	0 0001 0011	0 13	1	1	(D)←0		X	Clears port D.
	CLS	0 0001 0000	0 10	1	1	(S)←0		X	Clears port S.
	CLDS	0 0001 0001	0 11	1	1	(D)←0, (S)←0		X	Clears ports S and D.
Interrupts	EI	0 0000 0101	0 05	1	1	(INTE)←1		X	Sets interrupt flag INTE to enable interrupts.
	DI	0 0000 0100	0 04	1	1	(INTE)←0		X	Resets interrupt flag INTE to disable interrupts.
	INTH	0 0000 0110	0 06	1	1	(INTP)←1		X	Sets interrupt polarity flag INTP to enable interrupts when the interrupt request signal is turned high.
	INTL	0 0000 0111	0 07	1	1	(INTP)←0		X	Resets interrupt polarity flag INTP to enable interrupts when the interrupt request signal is turned low.
Misc	NOP	0 0000 0000	0 00	1	1	(PC)←(PC)+1		X	No operation

Symbol	Contents
A	4-bit register (aacumulator)
B	4-bit register
C	3-bit register
E	8-bit register
H	4-bit register
J	15-bit register
L	4-bit register
X	2-bit register
Y	4-bit register
Z	1-bit register
DP	7-bit data pointer, combination of registers, Z, X and Y
PC_H	The high-order four bits of the program counter.
PC_L	The low-order seven bits of the program counter.
PC	11-bit program counter, combination of PC_H and PC_L.

Symbol	Contents
SK0	11-bit stack register
SK1	11-bit stack register
SK2	11-bit stack register
CY	1-bit carry flag
xx	2-bit binary variable
yyyy	4-bit binary variable
z	1-bit binary variable
nnnn	4-bit binary constant
i	1-bit binary constant
jj	2-bit binary constant
XXXX	4-bit unknown binary number
D	11-bit port
K	15-bit port
S	8-bit port

Symbol	Contents
INTE	Interrupt enable flag
INTP	Interrupt polarity flag
INT	Interrupt request signal.
←	Shows direction of data flow.
( )	Indicates contents of the register, memory, etc.
∀	Exclusive OR.
—	Negation.
X	Indicates flag is unaffected by instruction execution.
xy	Label used to indicate the address xxyyyy.
pxy	Label used to indicate the address xxyyyy of page pppp.
CPS	Indicates which data pointer and carry are active.
C + x	Hexadecimal number C + binary number x.

LIST OF INSTRUCTION CODES

D_8-D_4 / D_3-D_0 (Hexadecimal notation)		0 0000	0 0001	0 0010	0 0011	0 0100	0 0101	0 0110	0 0111	0 1000	0 1001	0 1010	0 1011	0 1100	0 1101	0 1110	0 1111	1 0000 ~ 1 0111	1 1000 ~ 1 1111
		0 0	0 1	0 2	0 3	0 4	0 5	0 6	0 7	0 8	0 9	0 A	0 B	0 C	0 D	0 E	0 F	10~17	18~1F
0000	0	NOP	CLS	SZB 0	SEY 0	LCPS 0	CPAE	XAM 0	BL BML	—	—	A 0	LA 0	LXY 0,0	LXY 1,0	LXY 2,0	LXY 3,0	BM	B
0001	1	BA BMA BLA BMLA	CLDS	SZB 1	SEY 1	LCPS 1	CPAS	XAM 1	BL BML	—	—	A 1	LA 1	LXY 0,1	LXY 1,1	LXY 2,1	LXY 3,1	BM	B
0010	2	INY	—	SZB 2	SEY 2	SHL	RHL	XAM 2	BL BML	—	—	A 2	LA 2	LXY 0,2	LXY 1,2	LXY 2,2	LXY 3,2	BM	B
0011	3	DEY	CLD	SZB 3	SEY 3	—	—	XAM 3	BL BML	—	—	A 3	LA 3	LXY 0,3	LXY 1,3	LXY 2,3	LXY 3,3	BM	B
0100	4	DI	RD	—	SEY 4	RT	IAS 0	TAM 0	BL BML	—	—	A 4	LA 4	LXY 0,4	LXY 1,4	LXY 2,4	LXY 3,4	BM	B
0101	5	EI	SD	—	SEY 5	RTS	IAS 1	TAM 1	BL BML	—	—	A 5	LA 5	LXY 0,5	LXY 1,5	LXY 2,5	LXY 3,5	BM	B
0110	6	INTH	TEPA	SEAM	SEY 6	RTI	—	TAM 2	BL BML	—	—	A 6	LA 6	LXY 0,6	LXY 1,6	LXY 2,6	LXY 3,6	BM	B
0111	7	INTL	OSPA	—	SEY 7	—	LC7	TAM 3	BL BML	—	—	A 7	LA 7	LXY 0,7	LXY 1,7	LXY 2,7	LXY 3,7	BM	B
1000	8	CPA	XAL	—	SEY 8	RC	XAH	XAMD 0	BL BML	—	—	A 8	LA 8	LXY 0,8	LXY 1,8	LXY 2,8	LXY 3,8	BM	B
1001	9	DEC	TLA	SZJ	SEY 9	SC	THA	XAMD 1	BL BML	—	—	A 9	LA 9	LXY 0,9	LXY 1,9	LXY 2,9	LXY 3,9	BM	B
1010	A	AM	TEAB	—	SEY 10	LZ 0	—	XAMD 2	BL BML	—	—	A 10	LA 10	LXY 0,10	LXY 1,10	LXY 2,10	LXY 3,10	BM	B
1011	B	OSE	OSAB	SZD	SEY 11	LZ 1	—	XAMD 3	BL BML	—	—	A 11	LA 11	LXY 0,11	LXY 1,11	LXY 2,11	LXY 3,11	BM	B
1100	C	TYA	TBA	—	SEY 12	SB 0	RB 0	XAMI 0	BL BML	—	—	A 12	LA 12	LXY 0,12	LXY 1,12	LXY 2,12	LXY 3,12	BM	B
1101	D	TAJ	TAY	—	SEY 13	SB 1	RB 1	XAMI 1	BL BML	—	—	A 13	LA 13	LXY 0,13	LXY 1,13	LXY 2,13	LXY 3,13	BM	B
1110	E	AMC	TAB	—	SEY 14	SB 2	RB 2	XAMI 2	BL BML	—	—	A 14	LA 14	LXY 0,14	LXY 1,14	LXY 2,14	LXY 3,14	BM	B
1111	F	AMCS	—	SZC	SEY 15	SB 3	RB 3	XAMI 3	BL BML	CMA	—	A 15	LA 15	LXY 0,15	LXY 1,15	LXY 2,15	LXY 3,15	BM	B

Note 1. The list shows the machine codes and corresponding machine instructions. D3~D0 indicate the low-order 4 bits of the machine code and D8~D4 indicate the high-order 5 bits. The hexadecimal values are also shown that represent these codes. An instruction may consist of 1, 2, or 3 words, but only the first word is listed. Codes indicated with bar (—) must not be used.

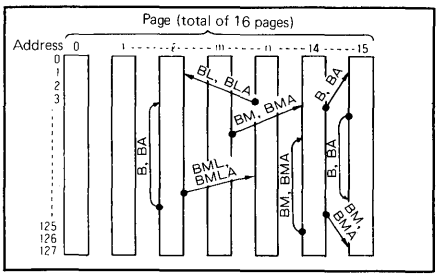
Note 2. Two-Word Instructions

	Second word
BL	1 1xxx yyy
BML	1 0xxx yyyy
BA	1 1xxx XXXX
BMA	1 0xxx XXXX

Three-Word Instructions

	Second word	Third word
BLA	0 0111 pppp	1 1xxx XXXX
BMLA	0 0111 pppp	1 0xxx XXXX

Note 3. Relationships of Branching and Paging for Branching, and Sub-Routine Call Instructions



MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{DD}	Supply voltage	With respect to V_{SS}	0.3 ~ −20	V
V_I	Input voltage, port S and D inputs		0.3 ~ −35	V
V_I	Input voltage, inputs other than port S and D		0.3 ~ −20	V
V_O	Output voltage, port S and D outputs		0.3 ~ −35	V
V_O	Output voltage, outputs other than port S and D		0.3 ~ −20	V
P_d	Power dissipation	Ta = 25°C	1100	mW
Topr	Operating temperature		−10 ~ 70	°C
Tstg	Storage temperature		−40 ~ 125	°C

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RECOMMENDED OPERATING CONDITIONS (T_a=−10~70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{DD}	Supply voltage	−13.5	−15	−16.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	−1.5		0	V
$V_{IH(\phi)}$	High-level clock input voltage	−1.5		0	V
V_{IL}	Low-level input voltage, inputs other than port D and S	V_{DD}		−4.2	V
V_{IL}	Low-level input voltage, port D and S inputs	−33		−4.2	V
$V_{IL(\phi)}$	Low-level clock input voltage	V_{DD}		V_{DD} + 2	V
$V_{I(K)}$	Analog input voltage, port K input	V_{REF}		0	V
V_{REF}	Reference voltage	−5		−7	V
V_{OL}	Low-level output voltage, port D and S outputs	−33		0	V
$f_{(\phi)}$	Internal clock oscillation frequency	300		600	kHz

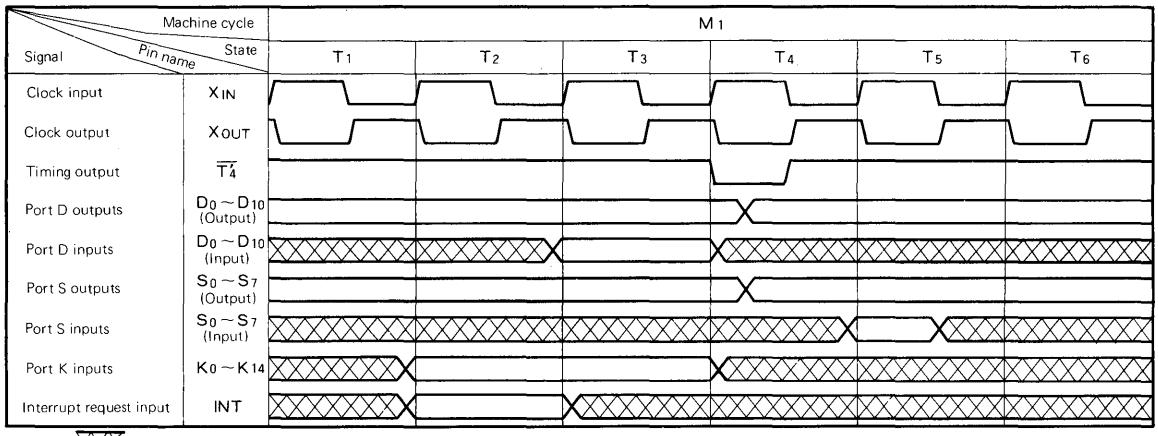
Note 1. $V_{IL(\phi)}$ is specified with respect to the maximum value of V_{DD}. The maximum allowable value is −33V when using a ceramic resonator with the M58841-XXXSP. This maximum allowable value is 1.1V for $V_{IH(\phi)}$ when using the M58841-XXXSP.

ELECTRICAL CHARACTERISTICS (T_a=−10~70°C, V_{DD}=−15V±10%, V_{SS}=0V, f(φ)=300~600kHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{T-}	Negative threshold voltage, RESET input	V_{DD} = −15V, Ta = 25°C	−4		−7	V
$V_{T+} - V_{T-}$	RESET input hysteresis	V_{DD} = −15V, Ta = 25°C	2		3.5	V
V_{OH}	High-level output voltage, port D outputs	V_{DD} = −15V, I_{OH} = −15mA, Ta = 25°C	−2.5			V
V_{OH}	High-level output voltage, port S outputs	V_{DD} = −15V, I_{OH} = −8mA, Ta = 25°C	−2.5			V
I_{IH}	High-level input current, port K (depletion load)	V_{DD} = −15V, V_{IH} = 0V, Ta = 25°C	100		370	μA
I_{IH}	High-level input current, port K (enhancement load)	V_{DD} = −15V, V_{IH} = 0V, Ta = 25°C	40		200	μA
I_{IH}	High-level input current, RESET	V_{DD} = −15V, V_{IH} = 0V, Ta = 25°C	30		100	μA
I_I	Input current, port K inputs	To be measured when the instruction CPAS or CPA is not being executed. V_I = −7V			−7	μA
$I_{I(\phi)}$	Clock input current	$V_{I(\phi)}$ = −15V, Ta = 25°C		−20	−40	μA
I_{OH}	High-level output current, port D outputs	V_{DD} = −15V, V_{OH} = −2.5V, Ta = 25°C			−15	mA
I_{OH}	High-level output current, port S outputs	V_{DD} = −15V, V_{OH} = −2.5V, Ta = −25°C			−8	mA
I_{OL}	Low-level output current, port D and port S outputs	V_{OL} = −33V, Ta = 25°C			−33	μA
I_{DD}	Supply current from V_{DD}	V_{DD} = −15V, Ta = 25°C			−41	mA
I_{REF}	Current from V_{REF}	V_{REF} = −7V, Ta = 25°C			−0.7	mA
C_I	Input capacitance, port K inputs	V_{DD} = V_I = V_O = V_{SS}, f = 1MHz 25mVrms		7	10	pF
$C_{I(\phi)}$	Clock input capacitance	V_{DD} = X_{OUT} = V_{SS}, f = 1MHz 25mVrms		7	10	pF
	A-D conversion linearity error	V_{REF} = −7V	Overall	±2	±3	LSB
	A-D conversion zero error	V_{REF} = −7V				
	A-D conversion fullscale error	V_{REF} = −7V				

Note 2. Currents are taken as positive when flowing into the IC (No sign), with the minimum and maximum values as absolute values.
3. The overall sum of the port D high-level output currents should be kept below 75mA.
4. The negative threshold voltage, hysteresis, high-level input current (depletion load), and high-level input current. For reset refer to the M58841-XXXSP.
5. The high-level input current (enhancement load), refer to the M58840-XXXP.

TIMING DIAGRAM



Note 1. The crosshatched area indicates invalid input.

DOCUMENTATION REQUIRED UPON ORDERING

The following information should be provided when ordering a custom mask.

(1) M58840-XXXP, M58841-XXXSP mask confirmation sheet.
(2) ROM data — 3 EPROM sets
(3) S output PLA coding — On confirmation sheets
(4) Interrupt input Schmitt circuits — On confirmation sheets
(5) M58840-XXXP reset circuits — On confirmation sheets
(6) Port K pulldown transistors — On confirmation sheets
(7) Pork K input discharge transistors — On confirmation sheets

MASK OPTIONS

The following type of mask options are available, specifiable at the time of ordering

(1) S output PLA data
(2) Interrupt input Schmitt circuit
(3) M58840-XXXP reset circuit
(4) Port K input pulldown resistors
(5) Port K input discharge transistors

DESCRIPTION

The M58842S MELPS 4 system evaluation device is designed to emulate the M58840-XXXP, M58841-XXXSP, M58843-XXXP and M58844-XXXP single-chip 4-bit microcomputer. It has been developed using P-channel aluminum-gate ED-MOS technology, and has a 64-pin ceramic DIL package. The M58842S facilitates fast development of new systems by using a program memory ROM external to the M58842S.

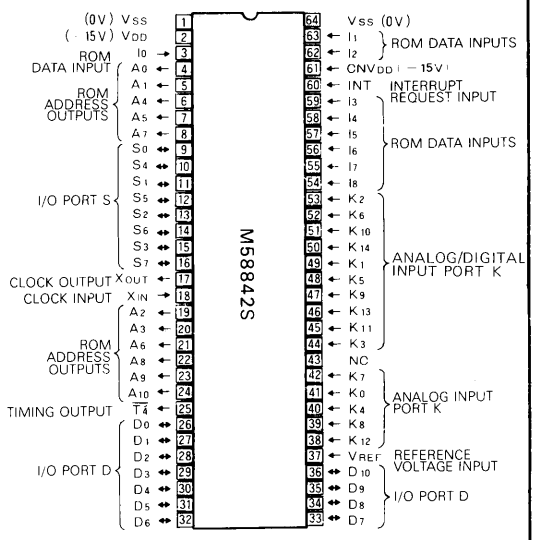
FEATURES

- Except for the mask ROM, all functions are equivalent to the M58840-XXXP.
- RAM capacity ..... 128-word x 4-bit
- Single – 15V power supply
- Built-in A/D converter/(15 analog inputs)
- Two data pointers
- Subroutine nesting ..... 3 levels
- Analog/digital input ports (K ports) 15
- I/O ports (ports D, S) 19
- Capable of direct drive of large fluorescent display tubes
- Interrupt ..... 1 level
- Internal PLA (mask option) for port S
- Internal clock generator

APPLICATION

- System development and prototyping of equipment using the M58840-XXXP, M58841-XXXSP, M58843-XXXP, and M58844-XXXP single-chip 4-bit microcomputers.

PIN CONFIGURATION (TOP VIEW)



Outline 64S1

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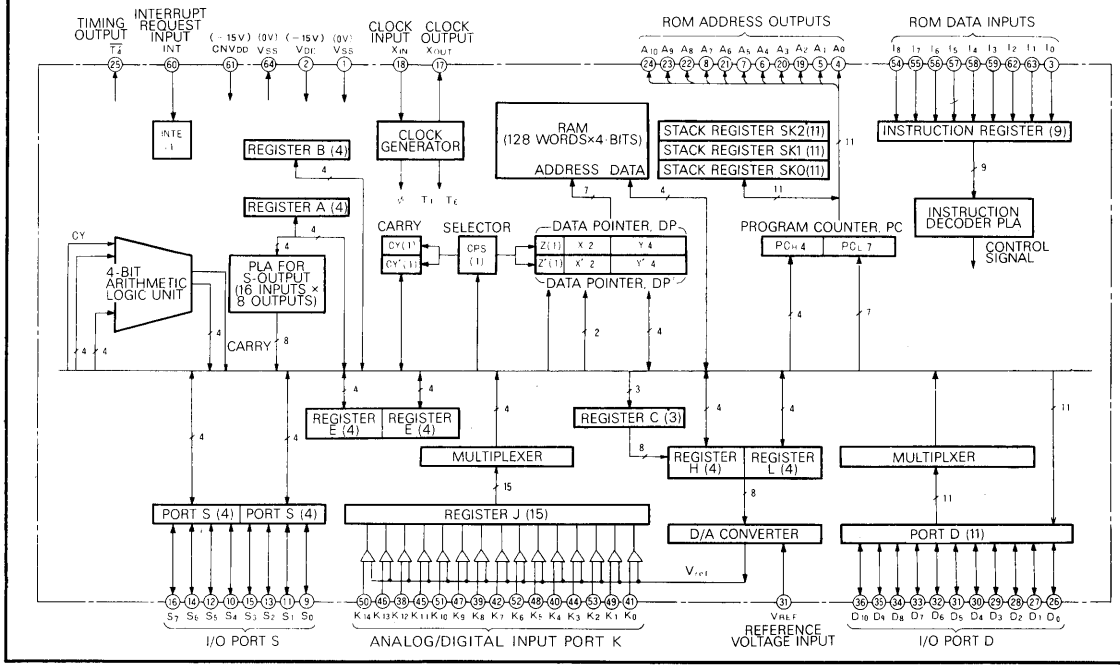
BLOCK DIAGRAM



FUNCTION

The M58842S MELPS 4 system evaluation device has the same functions as the M58840-XXXP single-chip 4-bit microcomputer except for the program memory ROM, which must be provided for from an external source connected through the address output pins ($A_0 \sim A_{10}$) and instruction input pins ($I_0 \sim I_8$).

In using the single-chip 4-bit microcomputer to control the operations of equipment, the operational procedures have to be put in a program and stored in the program memory (ROM). It may, however, consume a lot of time and effort, not to mention the cost, when a program correction is needed. This would naturally call for simulation of the application program before masking it into a ROM. In order to satisfy such a requirement, the M58842S has been prepared for evaluating a trial program before programming it into a mask-programmable ROM.

When using the M58842S for evaluating the M58841-XXXSP, M58843-XXXP and M58844-XXXP which are partially different from the M58840-XXXP (e.g. in the number of I/O ports), use the appropriate pins only. For example, since the M58843-XXXP is provided with a IK-word ROM, use the last IK words of the M58842S. Also since only the K_0 to K_3 ports are available, use K_0 through K_3 of the M58842S.

DESCRIPTION OF OPERATION

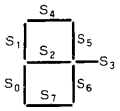
Programmable Logic Array (PLA) for the S-Output

The standard code listed below is stored in the PLA for the S-output. This code is used for numerical indication on 7-segment display units.

Input of ROM Data

Machine instructions can be executed by the M58842S if input from an external source. During the state T_2, the ROM address signal appears on the ROM address output pins $A_0 \sim A_{10}$. Then ROM data corresponding to this address should be applied to the ROM data input pins $I_0 \sim I_8$ during state T_6. For further details, refer to the instruction fetch timing diagram. During this application the input pin CNV_{DD} should be connected to V_{DD}.

LIST OF S-OUTPUT PLA CODES



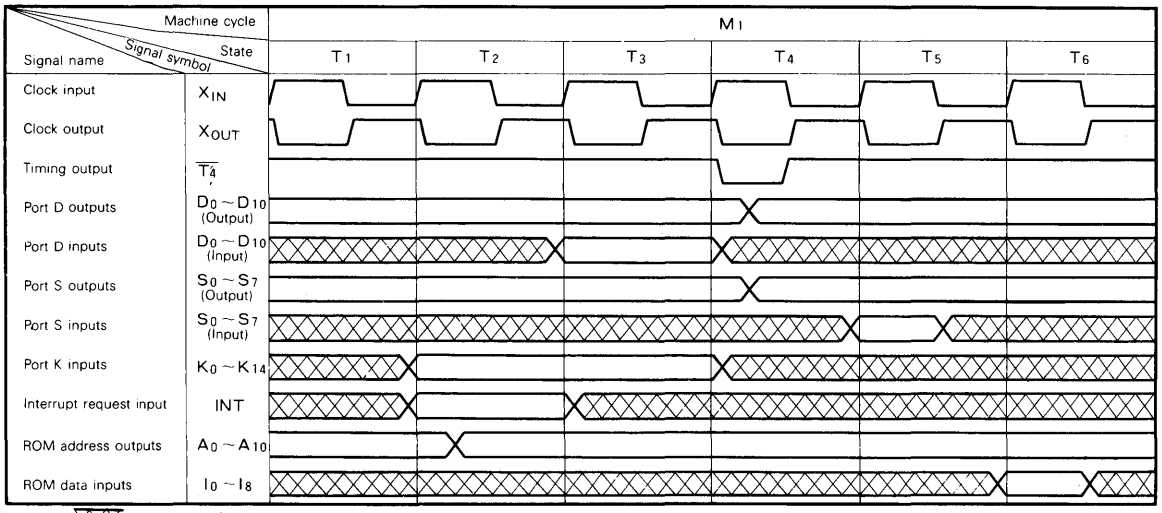
Register A					Port S output								Display
Hexadecimal notation	A_3	A_2	A_1	A_0	S_0	S_1	S_2	S_3	S_4	S_5	S_6	S_7	
0	0	0	0	0	H	H	L	L	H	H	H	H	0
1	0	0	0	1	L	L	L	L	L	H	H	L	1
2	0	0	1	0	H	L	H	L	H	H	L	H	2
3	0	0	1	1	L	L	H	L	H	H	H	H	3
4	0	1	0	0	L	H	H	L	L	H	H	L	4
5	0	1	0	1	L	H	H	L	H	L	H	H	5
6	0	1	1	0	H	H	H	L	H	L	H	H	6
7	0	1	1	1	L	H	L	L	H	H	H	L	7
8	1	0	0	0	H	H	H	L	H	H	H	H	8
9	1	0	0	1	L	H	H	L	H	H	H	H	9
A	1	0	1	0	H	L	H	L	L	L	H	H	0
B	1	0	1	1	L	L	L	H	L	L	L	L	–
C	1	1	0	0	H	H	H	L	H	L	L	H	E
D	1	1	0	1	H	H	L	L	H	L	L	H	C
E	1	1	1	0	L	L	H	L	L	L	L	L	–
F	1	1	1	1	L	L	L	L	L	L	L	L	Blank

PIN CONFIGURATION

Pin	Name	Input or output	Function
K_0 \ K_{14}	Analog input port K	In	Analog port K has 15 independent analog input terminals. All signals applied to the 15 input lines of port K are simultaneously compared with the V_{ref} generated by the D-A converter. Corresponding bits of register J are set when the condition, $\|V_{ref}\| > \|V_{K(Y)}\|$ is met. This port is utilized for receiving input signals from the touch panel or receiving analog inputs from temperature and other sensing devices. It can also be used as a value threshold digital signal input port when the V_{ref} is properly selected.
S_0 \ S_7	I/O port S	In/out	The I/O port S can be used as either an 8-bit output port or a pair of 4-bit input ports. Since it has open-drain circuits, it is suitable for directly driving segments of a large fluorescent display tube. It has an 8-bit output latch and can perform to drive 8 bits simultaneously. When the output of port S is programmed to low-level, it remains in the floating (high-impedance) state so that it can be used as an input port.
D_0 \ D_{10}	I/O port D	In/out	The I/O port D is composed of 11 bits that can be used as discrete I/O units. Latches are provided on the output side to maintain individual output signals. When port D output is programmed to low-level, to keep it in floating (high-impedance) state, it can be used as a sense input port. The level of the input signal is sensed at the input terminal and is tested to determine if it is high or low by executing a skip instruction.
A_0 \ A_{10}	ROM address output	Out	The address output is composed of 11 bits that output the contents of the program counter PC to the external program memory (ROM).
I_0 \ I_8	ROM data input	In	The data input is composed of 9 bits that are used to fetch the instruction code for the CPU from the external program memory (ROM).
X_{IN}	Clock input	In	As the clock generator is contained internally, clock frequency is determined by connecting an external CR circuit or an IF ceramic resonator between the pins X_{IN} and X_{OUT}. In case an external clock source is to be used, it should be connected to the pin X_{IN}, leaving the pin X_{OUT} open.
X_{OUT}	Clock output	Out	This pin generates the clock frequency from the internal clock oscillation circuit. The oscillation frequency is controlled by connecting the CR circuit or IF ceramic resonator between this pin and the pin X_{IN}.
INT	Interrupt request input	In	This signal is used for requesting interrupts. Whether high or low-level interrupt signals are in used for requests is selected by means of the program. When the instruction INTH is executed, interrupt is accepted with a high-level signal, and accepted with a low-level signal when the instruction INTL is executed. When an interrupt is requested and accepted, program execution is jumped to address 0 of page 12. The instruction RTI is used for the return instruction.
V_{REF}	External reference voltage input	In	A reference voltage input is applied to the D-A converter from the external terminal. Its nominal value is V_{REF} = −7V. The value (n-0.5) $V_{REF}/256$ is generated by the D-A converter, and is compared with the analog signals from the input port K; where n represents the contents of the register H-L, but when n = 0, the output voltage is treated as 0V. It can also be used as an automatic reset signal input. When a high-level is applied to the V_{REF} input, it actuates the automatic reset circuit, and then the V_{REF} input is changed to low-level ready to start the program from address 0 of page 0.
$\overline{T_4}$	Timing output	Out	This pin generates a part of the basic timing pulse. This signal is used for testing other devices incorporated in the system.
CNV_{DD}	CNV_{DD} input	In	This input terminal should be conected with the V_{DD} and have a low-level input (−15V) applied.

4

BASIC TIMING CHART



Note 1: XXX indicates invalid signal input.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{DD}	Supply voltage	With respect to V_{SS}	0.3 ~ −20	V
V_I	Input voltage, port S and D inputs		0.3 ~ −35	V
V_I	Input voltage, other than port S and D inputs		0.3 ~ −20	V
V_O	Output voltage, port S and D outputs		0.3 ~ −35	V
V_O	Output voltage, other than port S and D outputs		0.3 ~ −20	V
P_d	Power dissipation	Ta = 25°C	1100	mW
Topr	Operating temperature		0 ~ 70	°C
Tstg	Storage temperature		−40 ~ 125	°C

RECOMMENDED OPERATING CONDITIONS (Ta = 0 ~ 70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{DD}	Supply voltage	−13.5	−15	−16.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	−1.5		0	V
$V_{IH(\phi)}$	High-level clock input voltage	−1.5		0	V
V_{IL}	Low-level input voltage, other than port D, port S and INT inputs	V_{DD}		−4.2	V
V_{IL}	Low-level input voltage, INT input	V_{DD}		−7	V
V_{IL}	Low-level input voltage, port D and S inputs	−33		−4.2	V
$V_{IL(\phi)}$	Low-level clock input voltage	V_{DD}		$V_{DD}+2$	V
$V_{I(K)}$	Analog input voltage, port K input	V_{REF}		0	V
V_{REF}	Reference voltage	−5		−7	V
V_{OL}	Low-level output voltage, port D and S outputs	−33		0	V
V_{OL}	Low-level output voltage, ROM address output	V_{DD}		0	V
$f(\phi)$	Internal clock oscillation frequency	300		600	kHz

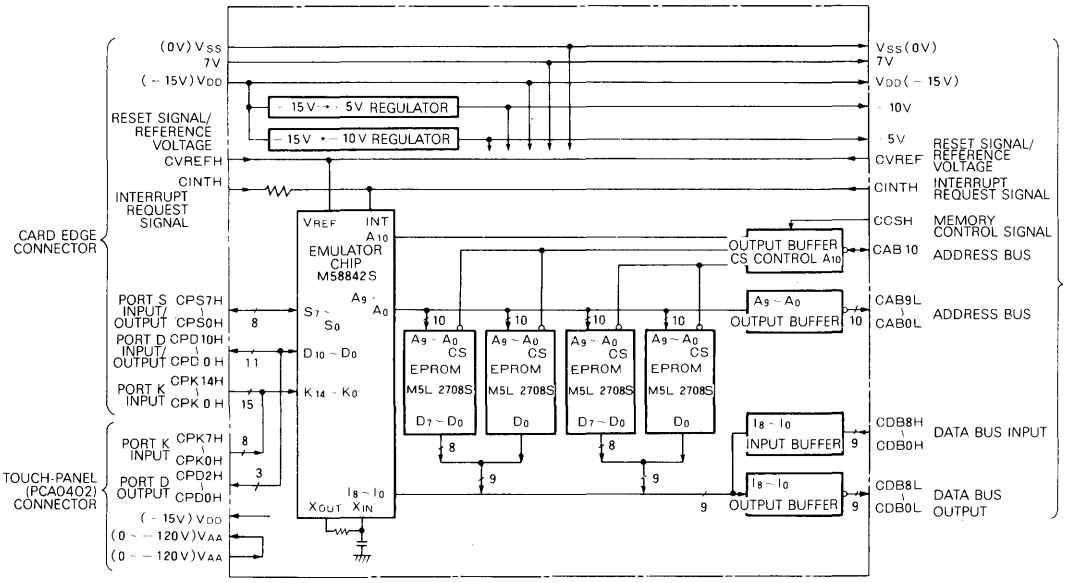
Note 1: The standard $V_{IL}(\phi)$ is with respect to the maximum V_{DD}.

ELECTRICAL CHARACTERISTICS (T_a = 0 ~ 70°C, V_{DD} = −15V ± 10%, V_{SS} = 0V, f(φ) = 300 ~ 600kHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage, port D and S inputs		−1.5		0	V
V_{IH}	High-level input voltage, ROM data inputs		−1.5		0	V
V_{IL}	Low-level input voltage, port D and S inputs		−33		−4.2	V
V_{IL}	Low-level input voltage, ROM data inputs		V_{DD}		−4.2	V
V_{OH}	High-level output voltage, port D outputs	V_{DD} = −15V, I_{OH} = −15mA, T_a = 25°C	−2.5			V
V_{OH}	High-level output voltage, port S outputs	V_{DD} = −15V, I_{OH} = −8mA, T_a = 25°C	−2.5			V
V_{OH}	High-level output voltage, ROM address outputs	V_{DD} = −15V, I_{OH} = −2mA, T_a = 25°C	−2			V
I_I	Input current, port K inputs	To be measured when the instruction CPAS or CPA is not being executed. V_I = −7V			−7	μA
$I_{I(\phi)}$	Clock input current	$V_{I(\phi)}$ = −15V, T_a = 25°C		−20	−40	μA
I_{OH}	High-level output current, port D outputs	V_{DD} = −15V, V_{OH} = −2.5V, T_a = 25°C			−15	mA
I_{OH}	High-level output current, port S outputs	V_{DD} = −15V, V_{OH} = −2.5V, T_a = 25°C			−8	mA
I_{OL}	Low-level output current, ports D and S outputs	V_{OL} = −33V, T_a = 25°C			−33	μA
I_{OL}	Low-level output current, ROM address outputs	V_{OL} = −17V, T_a = 25°C			−17	μA
C_I	Input capacitance, port K inputs	V_{DD} = V_I = V_O = V_{SS}, f = 1MHz 25mVrms		7	10	pF
$C_{I(\phi)}$	Clock input capacitance	V_{DD} = X_{OUT} = V_{SS}, f = 1MHz 25mVrms		7	10	pF
	A-D conversion linearity error	V_{REF} = −7V	Total	±2	±3	LSB
	A-D conversion zero error	V_{REF} = −7V				
	A-D conversion full-scale error	V_{REF} = −7V				

Note 2 : Current flowing into an IC is positive; out is negative.
3 : The sum of high-level output current from port D must be 75mA (max).

APPLICATION EXAMPLE



M58843-XXXP,M58844-XXXSP

SINGLE-CHIP 4-BIT MICROCOMPUTER WITH 8-BIT A/D CONVERTER

DESCRIPTION

The M58843-XXXP and M58844-XXXSP are single-chip 4-bit microcomputers fabricated using p-channel aluminum gate ED-MOS technology. They include an on-chip 8-bit A-D converter. The M58843-XXXP is housed in a 28-pin plastic moulded DIL package while the M58844-XXXSP is housed in a 40-pin shrink plastic molded DIL package.

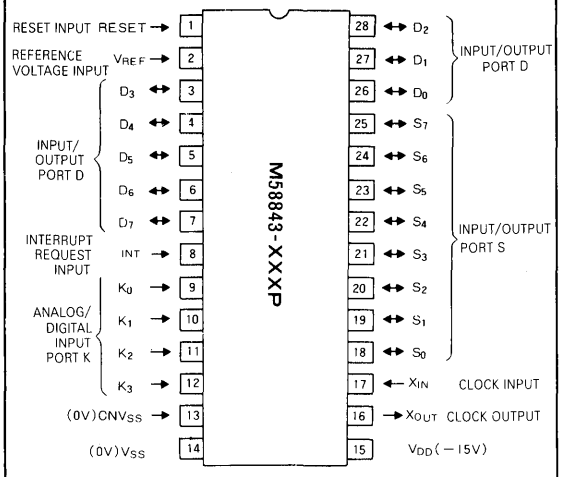
FEATURES

- Basic machine instructions 67
- Basic instruction execution time (for single-word instructions using a 600kHz clock frequency) 10μs
- Memory capacity ROM ..... 1024 words x 9 bits
  RAM ..... 64 words x 4 bits
- Single −15V power supply
- Built-in 8-bit A-D converter
- Two built-in data pointers
- Subroutine nesting ..... 3 levels
- Analog/digital inputs (port K)
  M58843-XXXP ..... 4 lines
  M58844-XXXSP ..... 11 lines
- Input/output (ports D and S)
  M58843-XXXP ..... 16 lines
  M58844-XXXSP ..... 19 lines
- Capable of driving large fluorescent tube displays
- Interrupt function ..... 1 factor, 1 level
- Built-in port S output decoder PLA (mask option)
- Built-in pull-down transistors (ports D, K, and S, mask option)
- Built-in clock generator circuit

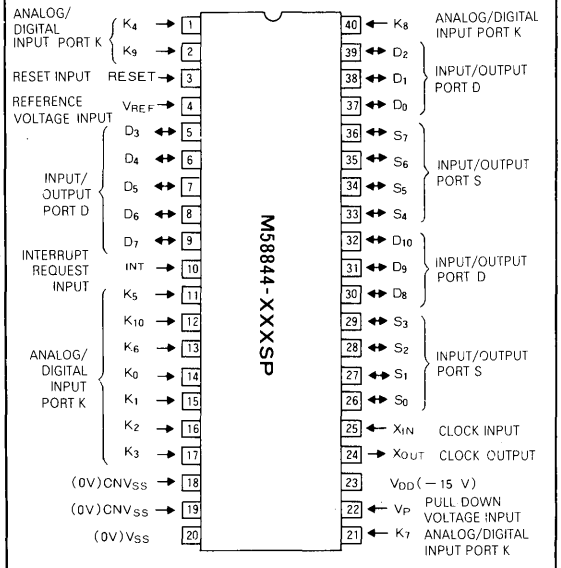
APPLICATIONS

- Electronic ranges, air conditioners, heaters, washing machines, rice cookers
- Office equipment, copying machines

PIN CONFIGURATIONS (TOP VIEW)



Outline 28P4



Outline 40P4B

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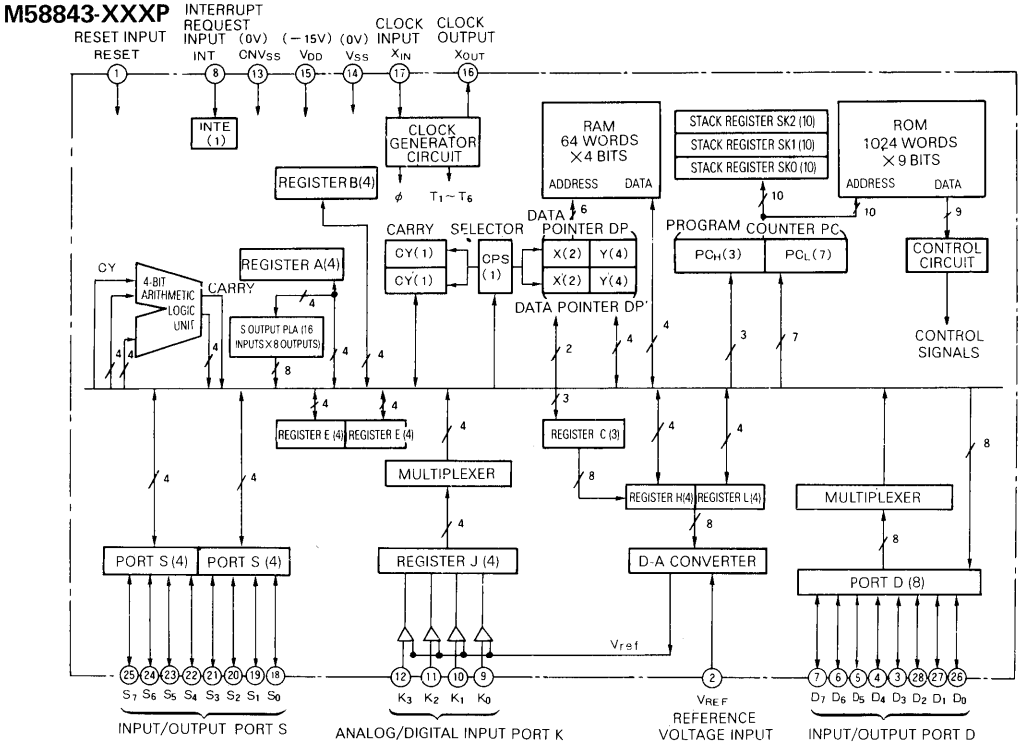
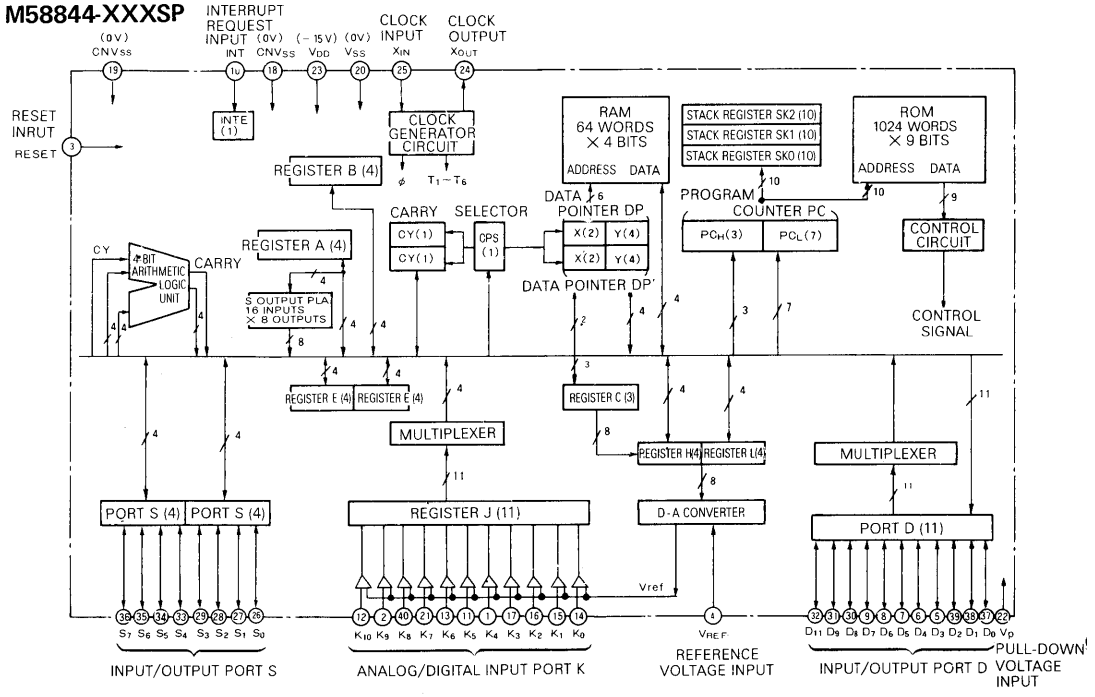
BLOCK DIAGRAMS

M58843-XXXP



M58844-XXXSP



PERFORMANCE SPECIFICATIONS

Parameter			Performance	
			M58843-XXXP	M58844-XXXSP
Basic machine instructions			67	67
Instruction execution time(1-word instruction)			10μs (with a clock frequency of 600kHz)	10μs (with a clock frequency of 600kHz)
Clock frequency			300～600kHz	300～600kHz
Memory capacity	ROM		1024 words x 9 bits	1024 words x 9 bits
	RAM		64 words x 4 bits	64 words x 4 bits
I/O port	K	Input	4 bits x 4	11 bits x 1
	S	Output	8 bits x 1	8 bits x 1
		Input	4 bits x 2	4 bits x 2
	D	Output	8 bits x 1	11 bits x 1
		Sense input	8 bits x 1	11 bits x 1
A-D conversion circuit			Built in (accuracy ± 2LSB, typ)	Built-in (accuracy ± 2LSB, typ)
RESET input			1 pin	1 pin
Subroutine nesting			3 levels (including one level of interrupt)	3 levels (including one level of interrupt)
Clock generator			Built-in (externally connected RC circuit or ceramic resonator)	Built-in (externally connected RC circuit or ceramic resonator)
I/O characteristics of ports	I/O withstanding voltage		-33V (max)	-33V (max)
	Port S output current		-8mA (max)	-8mA (max)
	Port D output current		-15mA (max)	-15mA (max)
Supply voltage	V_{DD}		-15V (typ)	-15V (typ)
	V_{SS}		0 V	0 V
Device structure			p-channel aluminum gate ED-MOS	P-channel aluminum gate ED-MOS
Package			28-pin plastic molded DIL package	40-pin shrink plastic molded DIL package
Power dissipation (excluding ports)			400mW (typ)	400mW (typ)

PIN DESCRIPTIONS

Pin	Name	Input or output	Function
V_{DD} V_{SS}	Power supplies	In	V_{DD} and V_{SS} are applied as -15V ±10% and 0V respectively
$K_0 \sim K_3$ (M58843-XXXP) $K_0 \sim K_{10}$ (M58844-XXXSP)	Analog/digital input port K	In	The input port K consists of 4 (11 for the M58844-XXXP) independent analog input pins. They can be programmed to receive digital quantities as well.
$S_0 \sim S_7$	Input/output port S	In/out	The I/O port S can be used as either an 8-bit output port or a pair of 4-bit input ports. Since it has open drain circuits, it is suitable for directly driving segments of a large fluorescent display tube. When the output port S is programmed to a low level, it remains in the floating state (high-impedance) so that it can be used as an input port.
$D_0 \sim D_7$ (M58843-XXXP) $D_0 \sim D_{10}$ (M58844-XXXSP)	Input/output port D	In/out	Port D consists of 8 bits for the M58843-XXXP and 11 bits for the M58844-XXXSP, all bits operating individually for input and output functions. When a port D output is programmed to low, the output floats (goes to high, impedance state) and the input signal can be sensed.
X_{IN}	Clock input	In	A clock generator is built into the device so that the clock frequency is determined by connecting an external RC circuit or ceramic resonator between pins X_{IN} and X_{OUT}. When an external clock source is used, it should be connected to the X_{IN} pin, leaving the X_{OUT} pin open.
X_{OUT}	Clock output	Out	This pin is the output of the built-in clock generator circuit. The oscillation frequency is controlled by connecting an RC circuit or ceramic resonator element between this pin and the X_{IN} pin.
INT	Interrupt request input	In	This pin is used to input the interrupt request signal. The level of the interrupt signal can be programmed as either high or low.
V_{REF}	Reference voltage input	In	This is the input for the reference voltage applied to the D-A converter.
CNV_{SS}	CNV_{SS} input	In	This input is connected to V_{SS} and must have a high-level input applied to it (0V).
RESET	Reset input	In	When this input is kept high for at least two machine cycles, the reset state is enabled.
V_P (M58844-XXXSP only)	Pull-down voltage input	In	This pin is used to supply the pull-down voltage for port D outputs and port S outputs.

BASIC FUNCTION BLOCKS

Program Memory (ROM)

This 1024-word x 9-bit mask programmable ROM can be programmed with machine instruction codes in accordance with the customer's specifications. It consists of 8 pages, each containing an address range of 0 ~ 127. Fig. 1 shows the address map of this ROM.

Program Counter (PC)

This counter is used to specify ROM addresses and the sequence of read-out of instructions stored in ROM. The program counter (PC) is an 10-bit binary counter, the upper order 3 bits of which (PC_H) indicate the ROM page, and the lower order 7 bits of which (PC_L) are a pure binary address designation. Each time an instruction is executed, PC_L is incremented by one step. For branching, and subroutine call instructions, its value is set to the designated address.

When the 127th address is reached for every page, the address value returns to the first address of that page. Therefore, for moving from one page to another page, the page byte itself must be modified. This is done using the BL and BLA instructions.

Page 14 and page 15 are special pages used for subroutine calls. The page 14 subroutine can be called with a one word instruction from any arbitrary page. This instruction is either BM or BMA. When either BM or BMA is executed, subsequent BM or BMA instructions are equivalent to B and BA on page 14. Also, B or BA is equivalent to B or BA on page 15. This condition is cancelled when the RT, RTS, BL, BML, BLA or BMLA instruction is executed. Note 3 under the instruction codes shows corresponding states.

Stack Registers (SK_0, SK_1, SK_2)

These registers are used to temporarily store the contents of the PC while executing subroutines or interrupt programs until the program returns to its original routine. The SK registers are organized in three words of 10 bits each, enabling up to three levels of subroutine nesting. If one word is used for an interrupt routine, the remaining two levels can be used for subroutine calls.

Data Memory (RAM)

This 256-bit (64 words x 4 bits) RAM is used to store both processing and control data. One RAM word consists of 4 bits with bit manipulation possible over the entire storage area. The 64 words are arranged as 4 files x 16 digits x 4 bits. Fig. 2 shows the RAM address map.

The RAM address specification is made by the combination of data pointer DP register X, and register Y. Thus, the selector CPS and data pointer DP must be set. However, as long as the address is not changed this is not necessary.

Data Pointers (DP, DP')

These registers are used to designate RAM address, and bit position for the I/O port D and register J. Each data pointer is composed of a 6-bit register group. Register X (the upper order 2 bits of DP) designates a RAM file; and register Y (the lower order 4 bits of DP) designates the digit position of the RAM file. At the same time, register Y designates bit positions of the I/O port D and register J.

4-bit Arithmetic Logic Unit (ALU)

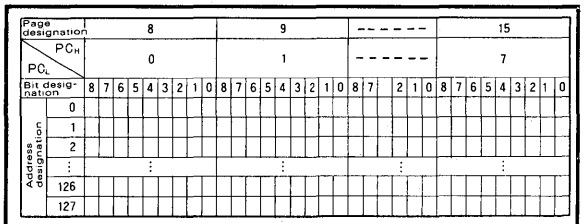
This unit executes 4-bit arithmetic and logical operations by means of a 4-bit adder and related logic circuitry. The arithmetic logic unit performs addition, logical comparisons, arithmetic comparisons, and bit manipulation.

Register A and Carry flag (CY)

Register A is a 4-bit accumulator that constitutes the basis for arithmetic operations. Data processing operations such as arithmetic and logical operations, data transfer, exchange, conversion and data input/output are executed by means of this register. Carry or borrow from register is stored in the carry flag's CY and CY' after execution of arithmetic or logical operations. The carry flags CY and CY' can also be used as 1-bit flags. Carry flags and data pointer DP selection is done by means of the selector CPS.

Registers B and E

Register B is composed of 4 bits and can be used as a 4-bit temporary storage register or for 8-bit data transfer in conjunction with register A. Register E is composed of 8 bits and is used not only as an 8-bit temporary storage register, but also as a temporary storage register for I/O port S.



Note : The M58843-XXXP and M58844-XXXSP programs are developed using a support system having a 2048 word x 9-bit ROM memory. When using such a system pages 8 through 15 of the 2048 words (pages 0 through 15) are used so that the program counter PC_H = 0 ~ 7 is defined as pages 8 through 15.

Fig. 1 ROM Address map

File designation	Register X	0				1				2				3			
File name		F_0				F_1				F_2				F_3			
Bit designation		3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0
Digit designation (register Y)	0																
	1																
	2																
	⋮																
	14																
	15																

Fig. 2 RAM Address map

A/D Conversion Circuit

The following A/D conversion functions are controlled by software as described below. Fig. 3 shows the block diagram.

(1) Comparators

These comparators are implemented entirely with PMOS devices and use a chopper-type amplification method. They are capable of determining the larger of the D-A converter output Vref and the port K input signals $V_{K(Y)}$ (where(Y) = 0 ~ 10).

(2) Register J

Register J is composed of 11 1-bit registers, each representing the comparison result from the comparators. All register bits are set simultaneously. The value of the register J with respect to the comparison results is as follows.

1 when $|Vref| > |V_{K(Y)}|$

0 when $|Vref| < |V_{K(Y)}|$

In this relationship (Y) represents the bit position in register J which is designated by register Y. The comparison results can be checked for each bit using the SZJ instruction.

(3) Registers H – L

These two 4-bit registers are capable of transferring and exchanging data to and from register A.

The 8-bit digital data for the D-A converter is transferred from these registers, the higher order 4 bits from H and lower order 4 bits from L.

(4) Register C

This 3-bit register is used as a counter to designate bit positions in the H and L registers.

(5) D-A Converter

The D-A converter converts the digital values stored in the registers H and L, referencing with the external reference voltage V_{REF} applied at the pin V_{REF}, to the analog value of the internal reference voltage Vref.

The theoretical value of the internal reference voltage Vref is defined as follows.

$$Vref = \frac{n-0.5}{256} \times V_{REF}, \text{ where, } n = 1, 2, \ldots\ldots 255$$

$$Vref = 0 \quad , \text{where, } n = 0$$

In the above relationships n is the value weighted according to the contents of registers H and L.

A-D Conversion Algorithms

A-D conversion is controlled by the programming of the previously described functional blocks. Thus, by modifying the program, either the successive approximation method or the sequential comparison method may be selected. In addition, a digital input of high or low level may be used to select the method, eliminating software selection of the A-D conversion technique.

(1) Successive Approximation

In this method, the conversion speed is maintained constant regardless of the amplitude of the analog signal. The A-D conversion process requires 0.6ms (at 600KHz clock frequency). 12 programs words are required.

(2) Sequential Comparison

In this method the conversion speed varies in accordance with the rate of change of the analog quantity. When the rate of change is slow, the conversion rate increases. 30 program words are required.

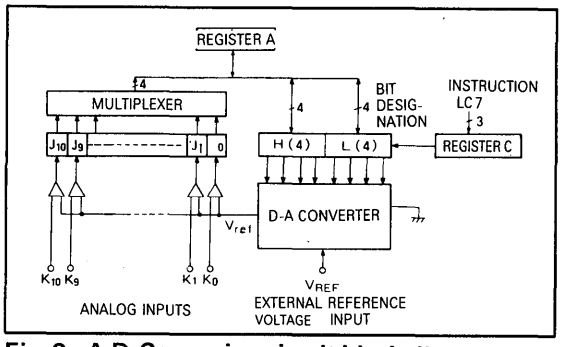


Fig. 3 A-D Conversion circuit block diagram

Interrupt

The flag INTE is a 1-bit flip-flop used to control interrupt operation. When an interrupt request signal is applied to the pin INT while the interrupt is enabled, the INTE flag is reset to disable further interrupts, after which the program jumps from the main program to address 0 of page 12. When an interrupt program is used, one level of the three-level stack register is required, the remaining two levels being used for subroutines. After the interrupt program is started, the data pointer DP, register A, carry flag CY, and registers used by the interrupt program are saved. It is necessary to restore these before returning to the main program by using the instruction RTI.

When an interrupt occurs, the microcomputer internal states are as follows.

(1) Program Counter
The current address in the main program is stored in a stack register and the program counter is set to page 12, address 0.

(2) Interrupt Flag INTE
The flag INTE is reset to disable further interrupts. This disable state will continue even after the program has returned from the interrupt routine to the main program by the execution of the RTI instruction. EI is executed and when the input level of the INT input changes, this state is disabled. Thus, when the INTH instruction is executed the interrupt state is enabled when the INT input goes high. As long as it remains in the high state, further interrupts are prohibited. If the INT input should change to a low level and return to high, the next interrupt will be accepted.

(3) Skip Flags
Skip flags are provided to discriminate skip instructions and consecutively described skip instructions. Each flag has its own stack within which the skip state is saved.

As a mask option, the interrupt pins may be provided with Schmitt input circuits.

Input/Output Pins

(1) Input port K
The input port K consists of 4 bits for the M58843-XXXP and 11 bits for the M58844-XXXSP. The voltage level input at these pins is compared with the D-A converter voltage output Vref by a comparator and the results stored in register J. As a mask option, it is possible to build load resistors into the input port K. These are implemented using depletion-type MOS transistors. In addition, to enable the use of capacitive touch-type keys, it is possible to provide these inputs with the required discharge transistors.

(2) Input/Output Port S
The input/output port S consists of 8 bits, each bit with an output latch. These latches are used to store data transferred by means of a PLA from register A, or data transferred from register A and register B directly, or data transferred from register E directly. 4 bits at a time of the 8 input bits of port S may be transferred to register A.

Because port S outputs are provided with a built-in PLA, it is possible to output any arbitrarily settable 8-bit code from an input specified by register A. These PLA output codes can be specified arbitrarily as a mask option.

In addition, as a mask option, it is possible to build-in load resistors at the input/output port S. The load resistors are implemented with depletion-type MOS transistors.

(3) Input/Output Port D
The input/output port D consists of 8 bits for the M58843-XXXP and 11 bits for the M58844-XXXSP. Each bit can be individually designated as either input or output and is provided with its own latch. The contents of the data pointer register Y can be used to designate a single bit of port D for output or sensing.

In addition, as a mask option load resistors may be built-in at the input/output port D. These resistors are implemented by means of depletion-type MOS transistors.

When port S or port D is used as an input port, the output should first be cleared to the low state.

Reset Function

When the RESET input is kept high for at least two machine cycles, the reset state is enabled. As shown in Fig. 4, it is possible to implement a power-on reset circuit using an externally connected capacitor, resistor and diode. For this configuration, when the supply voltage falls below −13.5V, the circuit design should insure that the RESET input is above −4V.

When the reset state is enabled, the following operations are performed.

(1) The program counter is set to page 8, address 0
(PC) ← 0

Note 1: The M58843-XXXP and M58844-XXXSP programs are developed using a support system having a 2048 word x 9-bit ROM memory. When using such a system pages 8 through 15 of the 2048 words (pages 0 through 15) are used so that the program counter $PC_H = 0 \sim 7$ is defined as pages 8 through 15.

(2) The interrupt mode is in the interrupt disabled state
(INTE) ← 0
This is the same state as when the instruction DI is executed.

(3) By setting the interrupt request signal INT to high, the interrupt enabled state is entered. This is the same state

as when the instruction INTH is executed.

(4) All outputs of port S are cleared to low (S) ← 0
(5) All outputs of port D are cleared to low (D) ← 0
(6) The carry and data pointer selector CPS is cleared to low to designate DP and CY (CPS) ← 0

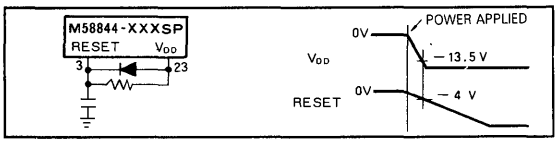


Fig. 4 Power-on reset

Clock Generator Circuit

A clock generator circuit has been built-in, to allow control of the frequency by means of an externally connected RC circuit or ceramic resonator. In addition, an external clock signal may be applied at the X_{IN} pin, leaving the X_{OUT} pin open. Circuit examples are shown in Fig. 5 to Fig. 7.

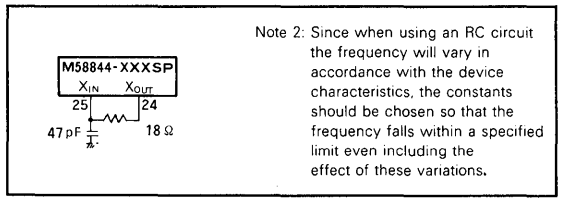


Fig. 5 External RC circuit

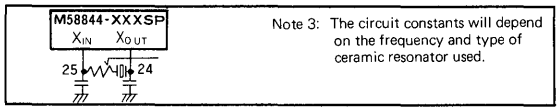


Fig. 6 Externally connected ceramic resonator

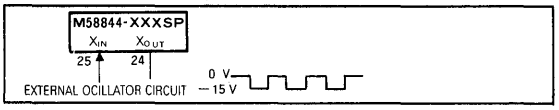


Fig. 7 External clock input circuit

MASK OPTIONS

The following mask options are available, specifiable at the time of initial ordering.

(1) S output PLA data
(2) Interrupt input Schmitt circuit
(3) Port Kinput pull-down resistors
(4) Port K input discharge transistors
(5) Port S input/output pull-down resistors
(6) Port D input/output pull-down resistors

DOCUMENTATION REQUIRED UPON ORDERING

The following information should be provided when ordering a custom mask.

(1) M58843-XXXP, M58844-XXXSP mask confirmation sheet
(2) ROM data 3 EPROM sets
(3) S output PLA coding On confirmation sheets
(4) Interrupt input Schmitt circuits On confirmation sheets
(5) Port K input pull-down resistors On confirmation sheets
(6) Port K input discharge transistors On confirmation sheets
(7) Port S input/output pull-down resistors On confirmation sheets
(8) Port D input/output pull-down resistors On confirmation sheets

LIST OF INSTRUCTION CODES

$D_8 \sim D_4$ / Hexadecimal notation / $D_3 \sim D_0$		0 0000	0 0001	0 0010	0 0011	0 0100	0 0101	0 0110	0 0111	0 1000	0 1001	0 1010	0 1011	0 1100	0 1101	0 1110	0 1111	1 0000 ~ 1 0111	1 1000 ~ 1 1111
		0 0	0 1	0 2	0 3	0 4	0 5	0 6	0 7	0 8	0 9	0 A	0 B	0 C	0 D	0 E	0 F	10 ~ 17	18 ~ 1F
0000	0	NOP	CLS	S Z B 0	SEY 0	LCPS 0	CPAE	XAM 0	BL BML	—	—	A 0	LA 0	LXY 0, 0	LXY 1, 0	LXY 2, 0	LXY 3, 0	BM	B
0001	1	BA BMA BLA BMLA	CLDS	S Z B 1	SEY 1	LCPS 1	CPAS	XAM 1	BL BML	—	—	A 1	LA 1	LXY 0, 1	LXY 1, 1	LXY 2, 1	LXY 3, 1	BM	B
0010	2	INY	—	S Z B 2	SEY 2	SHL	RHL	XAM 2	BL BML	—	—	A 2	LA 2	LXY 0, 2	LXY 1, 2	LXY 2, 2	LXY 3, 2	BM	B
0011	3	DEY	CLD	S Z B 3	SEY 3	—	—	XAM 3	BL BML	—	—	A 3	LA 3	LXY 0, 3	LXY 1, 3	LXY 2, 3	LXY 3, 3	BM	B
0100	4	DI	RD	—	SEY 4	RT	IAS 0	TAM 0	BL BML	—	—	A 4	LA 4	LXY 0, 4	LXY 1, 4	LXY 2, 4	LXY 3, 4	BM	B
0101	5	EI	SD	—	SEY 5	RTS	IAS 1	TAM 1	BL BML	—	—	A 5	LA 5	LXY 0, 5	LXY 1, 5	LXY 2, 5	LXY 3, 5	BM	B
0110	6	INTH	TEPA	SEAM	SEY 6	RTI	—	TAM 2	BL BML	—	—	A 6	LA 6	LXY 0, 6	LXY 1, 6	LXY 2, 6	LXY 3, 6	BM	B
0111	7	INTL	OSPA	—	SEY 7	—	LC7	TAM 3	BL BML	—	—	A 7	LA 7	LXY 0, 7	LXY 1, 7	LXY 2, 7	LXY 3, 7	BM	B
1000	8	CPA	XAL	—	SEY 8	RC	XAH	XAMD 0	BL BML	—	—	A 8	LA 8	LXY 0, 8	LXY 1, 8	LXY 2, 8	LXY 3, 8	BM	B
1001	9	DEC	TLA	S Z J	SEY 9	SC	THA	XAMD 1	BL BML	—	—	A 9	LA 9	LXY 0, 9	LXY 1, 9	LXY 2, 9	LXY 3, 9	BM	B
1010	A	AM	TEAB	—	SEY 10	—	—	XAMD 2	BL BML	—	—	A 10	LA 10	LXY 0, 10	LXY 1, 10	LXY 2, 10	LXY 3, 10	BM	B
1011	B	OSE	OSAB	S Z D	SEY 11	—	—	XAMD 3	BL BML	—	—	A 11	LA 11	LXY 0, 11	LXY 1, 11	LXY 2, 11	LXY 3, 11	BM	B
1100	C	TYA	TBA	—	SEY 12	SB 0	RB 0	XAMI 0	BL BML	—	—	A 12	LA 12	LXY 0, 12	LXY 1, 12	LXY 2, 12	LXY 3, 12	BM	B
1101	D	TAJ	TAY	—	SEY 13	SB 1	RB 1	XAMI 1	BL BML	—	—	A 13	LA 13	LXY 0, 13	LXY 1, 13	LXY 2, 13	LXY 3, 13	BM	B
1110	E	AMC	TAB	—	SEY 14	SB 2	RB 2	XAMI 2	BL BML	—	—	A 14	LA 14	LXY 0, 14	LXY 1, 14	LXY 2, 14	LXY 3, 14	BM	B
1111	F	AMCS	—	S Z C	SEY 15	SB 3	RB 3	XAMI 3	BL BML	CMA	—	A 15	LA 15	LXY 0, 15	LXY 1, 15	LXY 2, 15	LXY 3, 15	BM	B

Note 1: This list shows the machine codes and corresponding machine instructions. $D_3 \sim D_0$ indicate the low-order 4 bits of the machine code and $D_8 \sim D_4$ indicate the high-order 5 bits. Hexadecimal numbers are also shown that represent the codes.
An instruction may consist of one, two, or three words, but only the first word is listed. Code combination indicated with a bar (–) must not be used.

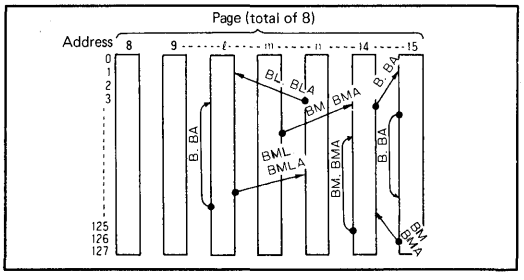
Note 2: Two-word instruction

	Second word
BL	1 1xxx yyyy
BML	1 0xxx yyyy
BA	1 1xxx XXXX
BMA	1 0xxx XXXX

Three-word instruction

	Second word	Third word
BLA	0 0111 pppp	1 1xxx XXXX
BMLA	0 0111 pppp	1 0xxx XXXX

Note 3: Page relationships for branching by means of branching instructions and subroutine calling instructions.



MACHINE INSTRUCTIONS

Type of instruction	Mnemonic	Instruction code $D_8\ D_7D_6D_5D_4\ D_3D_2D_1D_0$	16 mal notation	No. of words	No. of cycles	Functions	Skip conditions	Flag CY	Description of operation
Register-to-register transfers	**TAB**	0 0001 1110	0 1E	1	1	(A)←(B)	—	x	Transfers contents of register B to register A.
	TBA	0 0001 1100	0 1C	1	1	(B)←(A)	—	x	Transfers contents of register A to register B.
	TAY	0 0001 1101	0 1D	1	1	(A)←(Y)	—	x	Transfers contents of register Y to register A.
	TYA	0 0000 1100	0 0C	1	1	(Y)←(A)	—	x	Transfers contents of register A to register Y.
	TEAB	0 0001 1010	0 1A	1	1	$(E_7\sim E_4)\leftarrow(B)$, $(E_3\sim E_0)\leftarrow(A)$	—	x	Transfers contents of registers A and B to register E.
	TEPA	0 0001 0110	0 16	1	1	$(E_7\sim E_0)\leftarrow$ through PLA$\leftarrow(A)$	—	x	Docodes contents of register A in the PLA and trasfers result to register E.
RAM addresses	**LXY x,y**	0 11xx yyyy	0 Cy + x	1	1	(X)←x, where x=0~3 (Y)←y, where, y=0~15	Written successively	x	Loads value of "x" into register X and of "y" into Y. When LXY is written successively, the first is executed and successive ones are skipped
	INY	0 0000 0010	0 02	1	1	(Y)←(Y)+1	(Y)=0	x	Increments contents of register Y by 1. Skips next instruction when new contents of register Y are "0"
	DEY	0 0000 0011	0 03	1	1	(Y)←(Y)−1	(Y)=15	x	Decrements contents of register Y by 1. Skips next instruction when new contents of register Y are "15".
	LCPS i	0 0100 000i	0 4i	1	1	(CPS)←i, where, i=0, 1	—	x	DP and CY are active when i=O, DP' and CY' when i=1.
RAM-accumulator transfers	**TAM j**	0 0110 01jj	0 64 + j	1	1	(A)←(M(DP)) (X)←(X)$\forall$i, where, i=0~3	—	x	Transfer the RAM contents addressed by the active DP to register A. Register X is then "exclusive OR-ed" with the value j in the instruction, and the result stored in register X.
	XAM j	0 0110 00jj	0 6j	1	1	(A)↔(M(DP)) (X)←(X)$\forall$j, where, j=0~3	—	x	Exchanges the contents of the RAM DP and register A. Contents of X are then "exclusive OR-ed" with the valuej and the result stored in register X.
	XAMD j	0 0110 10jj	0 68 + j	1	1	(A)↔(M(DP)), (Y)←(Y)−1 (X)←(X)$\forall$j, where, j=0~3	(Y)=15	x	Exchanges the contents of the RAM and register A. Contents of X are then "exclusive OR-ed" with the value j in the instruction, and the result stored in register X. The contents of register Y are decremented by 1, and when the result is 15, the next instruction is skipped.
	XAMI j	0 0110 11jj	0 6C + j	1	1	(A)↔(M(DP)), (Y)←(Y)+1 (X)←(X)$\forall$j, where, j=0~3	(Y)=0	x	Exchanges the contents of the RAM and register A. Contents of X are then "exclusive OR-ed" with the value j in the instruction and result stored in register X.The contents of register Y are when the incremented by 1, and when the result is 0. the next instruction is skipped.
Arithmetic operations	**LA n**	0 1011 nnnn	0 Bn	1	1	(A)←n, where, n=0~15	Written successively	x	Loads the value n into register A. When LA is written consecutively the first is executed, and successive ones are skipped.
	AM	0 0000 1010	0 0A	1	1	(A)←(A)+(M(DP))	—	x	Adds the contents of the RAM to register A. The result is retained in register A, and the contents of flag CY are unaffected.
	AMC	0 0000 1110	0 0E	1	1	(A)←(A)+(M(DP))+(CY) (CY)← carry	—	0/1	Adds the RAM contents addressed by the active DP and contents of flag CY to register A. The result is stored in register A, and the carry in the active flag CY.
	AMCS	0 0000 1111	0 0F	1	1	(A)←(A)+(M(DP))+(CY) (CY)← carry	(CY)=1 A carry is not produced and	0/1	Adds the contents of the RAM and flag CY to register A. The result is stored in register A and the carry in the CY, but the next instruction is skipped when a carry is produced.
	A n	0 1010 nnnn	0 An	1	1	(A)←(A)+n, where, n=0~15	=0 n≠6	x	Adds value n in the instruction to register A. The contents of flag CY are unaffected and their next instruction is skipped if a carry is not produced, except when n=6.
	SC	0 0100 1001	0 49	1	1	(CY)←1	—	1	Sets active flag CY.
	RC	0 0100 1000	0 48	1	1	(CY)←0	—	0	Resets active flag CY.
	SZC	0 0010 1111	0 2F	1	1	...	(CY)=0	x	Skips next instruction when contents of the active flag CY are O.
	CMA	0 1000 1111	0 8F	1	1	(A)←$\overline{(A)}$	—	x	Stores complement of register A in register A.
Bit operations	**SB j**	0 0100 11jj	0 4C + j	1	1	(Mj(DP))←1, where, j=0~3	—	x	Sets the jth bit of the RAM addressed by the active DP (the bit designated by the value j in the instruction)
	RB j	0 0101 11jj	0 5C + j	1	1	(Mj(DP))←0, where, j=0~3	—	x	Resets the jth bit of the RAM addressed by the active DP (the bit designated by the value j in the instruction).
	SZB j	0 0010 00jj	0 2j	1	1		(Mj(DP))=0 where,j=0~3	x	Skips next instruction when the contents of the jth bit of the RAM addressed by the active DP (the bit which is designated by the value j in the instruction) are O.
Compares	**SEAM**	0 0010 0110	0 26	1	1		(M(DP))=(A)	x	Skips next instruction when contents of register A are equal to the RAM contents addressed by the active DP.
	SEY y	0 0011 yyyy	0 3y	1	1		(Y)=y where, y=0~15	x	Skips next instruvtion. when the contents of register Y are equal to the value y in the instruction.
A/D converter operations	**TLA**	0 0001 1001	0 19	1	1	(L)←(A)	—	x	Transfers contents of register A to register L.
	THA	0 0101 1001	0 59	1	1	(H)←(A)	—	x	Transfers contents of register A to register H.
	TAJ	0 0000 1101	0 0D	1	1	$(Y_1Y_0)=0$ when, : $(A)\leftarrow(J_3J_2J_1J_0)$ $(Y_1Y_0)=1$ when, : $(A)\leftarrow(J_7J_6J_5J_4)$ $(Y_1Y_0)=2$ when, : $(A)\leftarrow(0\ J_{10}J_9J_8)$ $(Y_1Y_0)=3$ when, : (A)←(0 0 0 0)	—	x	Transfers designated contents of register J to register A.
	XAL	0 0001 1000	0 18	1	1	(A)↔(L)	—	x	Exchanges contents of register A with contents of register L.
	XAH	0 0101 1000	0 58	1	1	(A)↔(H)	—	x	Exchanges contents of register A with contents of register H.
	LC7	0 0101 0111	0 57	1	1	(C)←7	—	x	Loads 7 to register C.
	DEC	0 0000 1001	0 09	1	1	(C)←(C)−1	(C)=7	x	Decrements contents of register C by 1, when result is 7, skips next.
	SHL	0 0100 0010	0 42	1	1	$(C_2)=1$ when, : $(H_{(C_1-C_0)})\leftarrow1$ $(C_2)=0$ when, : $(L_{(C_1-C_0)})\leftarrow1$	—	x	Sets the bit in register L or H designated by register C. The box instruction shows the relationship between register C and bit position. (C) 7 6 5 4 3 2 1 0 / Bit H_3 H_2 H_1 H_0 L_3 L_2 L_1 L_0
	RHL	0 0101 0010	0 52	1	1	$(C_2)=1$ when, : $(H_{(C_1-C_0)})\leftarrow0$ $(C_2)=0$ when, : $(L_{(C_1-C_0)})\leftarrow0$	—	x	Resets the bit in register L or H that is designated by register C.
	CPA	0 0000 1000	0 08	1	1 (2)	$\lvert V_{ref}\rvert>\lvert V_{K(i)}\rvert$ when, : $(J_{(i)})\leftarrow1$ $\lvert V_{ref}\rvert<\lvert V_{K(i)}\rvert$ when, : $(J_{(i)})\leftarrow0$ i=0~10		x	Reads all analog values from input port K for comparison with D-A converter output V_{ref} and either sets the respective bit of register J to the next instruction cycle wherever $V_{ref}<V_{K(1)}$ is true, or resets it wherever $V_{ref}<V_{K(1)}$ is true.
	CPAS	0 0101 0001	0 51	1	1	$\lvert V_{ref}\rvert>\lvert V_{K(i)}\rvert$ when, : $(J_{(i)})\leftarrow1$ $\lvert V_{ref}\rvert<\lvert V_{K(i)}\rvert$ when, : $(J_{(i)})\leftarrow0$ i=0~10	—	x	Reads and stores temporarily all analog values from input port K, which are then unaffected by changes in port K inputs. These values are compared with the D-A converter output V_{ref}, calculated from contents of registers H and L and respective bits of register J are set/reset. Repeated when contents of registers H-L are changed.
	CPAE	0 0101 0000	0 50	1	1	Execution of the instruction CPAS is over, and no more changes will made in $(J_{(Y)})$.		x	Terminates execution of instruction CPAS. Contents of register J remain unaffected, maintaining the value immediately before termination, and input port K is again ready to receive inputs.
	SZJ	0 0010 1001	0 29	1	1		$(J_{(Y)})=0$	x	Skips next instruction when the bit in register J, designated by register Y, is 0.

Type of instruction	Mnemonic	Instruction code $D_4\ D_3D_2D_1D_0\ D_3D_2D_1D_0$	16mal notation	No. of words	No. of cycles	Functions	Skip conditions	Flag CY	Description of operation
Jumps	B xy	1 1 x x x y y y y	1 8y + x	1	1	$(PC_L) \leftarrow 16x+y$	—	X	Jumps to address xy of the current page.
						$(PC_H) \leftarrow 7$, $(PC_L) \leftarrow 16x+y$			Jumps to address xy on page 15 when executed, provided that none of instruction RT, RTS, BL, BML, BLA or BMLA was executed after execution of instruction BM or BMA.
	BL pxy	0 0111 pppp 1 1xxx yyyy	0 7p 1 8y + x	2	2	$(PC_H) \leftarrow p$ $(PC_L) \leftarrow 16x+y$	—	X	Jumps to address xy of page p.
	BA xX	0 0000 0001 1 1xxx XXXX	0 01 1 8X + x	2	2	$(PC_L) \leftarrow 16x+(A)$	—	X	Jumps to address x(A) of the current page.
						$(PC_H) \leftarrow 7$, $(PC_L) \leftarrow 16x+(A)$			Jumps to the address x(A) of page 15 provided that none of instructions. RT, RTS, BL, BML, BLA or BMLA was executed after execution of instruction BM or BMA.
	BLA pxX	0 0000 0001 0 0111 pppp 1 1xxx XXXX	0 01 0 7p 1 8X + x	3	3	$(PC_H) \leftarrow p$ $(PC_L) \leftarrow 16x+(A)$	—	X	Jumps to the address x(A) of page p.
Subroutine calls	BM xy	1 0xxx yyyy	1 xy	1	1	$(SK2) \leftarrow (SK1) \leftarrow (SK0) \leftarrow (PC)$ $(PC_H) \leftarrow 6$, $(PC_L) \leftarrow 16x+y$	—	X	Calls for the subroutine starting at address xy on page 14.
						$(PC_H) \leftarrow 6$, $(PC_L) \leftarrow 16x+y$			Jumps to address xy of page 14 provided that none of instructions. RT, RTS, BL, BML, BLA or BMLA was executed after the execution of instructions BM or BMA.
	BML pxy	0 0111 pppp 1 0xxx yyyy	0 7p 1 xy	2	2	$(SK2) \leftarrow (SK1) \leftarrow (SK0) \leftarrow (PC)$ $(PC_H) \leftarrow p$, $(PC_L) \leftarrow 16x+y$	—	X	Calls for the subroutine starting at address xy of page p.
	BMA xX	0 0000 0001 1 0xxx XXXX	0 01 1 xX	2	2	$(SK2) \leftarrow (SK1) \leftarrow (SK0) \leftarrow (PC)$ $(PC_H) \leftarrow 6$, $(PC_L) \leftarrow 16x+(A)$	—	X	Calls for the subroutine starting at address x(A) of page 14.
						$(PC_H) \leftarrow 6$, $(PC_L) \leftarrow 16x+(A)$			Jumps to address xy of page 14 provided that none of instructions. RT, RTS, BL, BML, BLA or BMLA was executed after the execution of instructions BM or BMA.
	BMLA pxX	0 0000 0001 0 0111 pppp 1 0xxx XXXX	0 01 0 7p 1 xX	3	3	$(SK2) \leftarrow (SK1) \leftarrow (SK0) \leftarrow (PC)$ $(PC_H) \leftarrow p$, $(PC_L) \leftarrow 16x+(A)$	—	X	Calls for the subroutine starting at address x(A) of page p.
Program returns	RTI	0 0100 0110	0 46	1	1	$(PC) \leftarrow (SK0) \leftarrow (SK1) \leftarrow (SK2)$ Restore internal flip-flop	—	X	Returns from interrupt routine to main routine. The internal flip-flop is restored to the value held immediately before the interrupt.
	RT	0 0100 0100	0 44	1	1	$(PC) \leftarrow (SK0) \leftarrow (SK1) \leftarrow (SK2)$	—	X	Returns to the main routine from the subroutine.
	RTS	0 0100 0101	0 45	1	2	$(PC) \leftarrow (SK0) \leftarrow (SK1) \leftarrow (SK2)$	Unconditional skip	X	Returns to the main routine from the subroutine, and uncidionally skips the next instruction.
Input/output	SD	0 0001 0101	0 15	1	1	$(D(Y)) \leftarrow 1$, where, $0 \leq (Y) \leq 10$	—	X	Sets the bit of port D that is designated by register Y.
	RD	0 0001 0100	0 14	1	1	$(D(Y)) \leftarrow 0$, where, $0 \leq (Y) \leq 10$	—	X	Resets the bit of port D that is designated by register Y.
	SZD	0 0010 1011	0 2B	1	1	where, $0 \leq (Y) \leq 10$	$(D(Y)) = 0$	X	Skip the next instruction if the contents of the bit of port D that is designated by register Y are o.
	OSAB	0 0001 1011	0 1B	1	1	$(S_7 \sim S_4) \leftarrow (B)$, $(S_3 \sim S_0) \leftarrow (A)$		X	Outputs contents of registers A and B to port S.
	OSPA	0 0001 0111	0 17	1	1	$(S_7 \sim S_0) \leftarrow$ through PLA $\leftarrow (A)$		X	Decodes contents of register A by PLA and the result is output to port.
	OSE	0 0000 1011	0 0B	1	1	$(S) \leftarrow (E)$		X	Outputs contents of register E to port S.
	IAS i	0 0101 010i	0 54 + i	1	1	$i=0$: $(A) \leftarrow (S_7 \sim S_4)$ $i=1$: $(A) \leftarrow (S_3 \sim S_0)$		X	Transfers from port S to register A. The high-order four bit of port S are transferred when the value of i in the instruction is O or the low-order four bits are transferred when the value of i is 1.
	CLD	0 0001 0011	0 13	1	1	$(D) \leftarrow 0$		X	Clears port D.
	CLS	0 0001 0000	0 10	1	1	$(S) \leftarrow 0$		X	Clears port S.
	CLDS	0 0001 0001	0 11	1	1	$(D) \leftarrow 0$, $(S) \leftarrow 0$		X	Clears ports S and D.
Interrupts	EI	0 0000 0101	0 05	1	1	$(INTE) \leftarrow 1$		X	Sets interrupt flag INTE to enable interrupts.
	DI	0 0000 0100	0 04	1	1	$(INTE) \leftarrow 0$		X	Resets interrupt flag INTE to disable interrupts.
	INTH	0 0000 0110	0 06	1	1	$(INTP) \leftarrow 1$		X	Sets interrupt polarity flag INTP to enable interrupts when the interrupt request signal is turned high.
	INTL	0 0000 0111	0 07	1	1	$(INTP) \leftarrow 0$		X	Resets interrupt polarity flag INTP to enable interrupts when the interrupt request signal is turned low.
Misc	NOP	0 0000 0000	0 00	1	1	$(PC) \leftarrow (PC)+1$		X	No operation
Pin	RESET					$(PC_H) \leftarrow 0$, $(PC_L) \leftarrow 0$			Start from address "0" of page 8.
	INT					$(SK_2) \leftarrow (SK_1) \leftarrow (SK_0) \leftarrow (PC)$, $(PC_H) \leftarrow 4$, $(PC_L) \leftarrow 0$			Calls for the subroutine starting at address "0" of page 12.

Symbol	Contents	Symbol	Contents	Symbol	Contents
A	4-bit register (accumulator)	SK1	10-bit stack register	INT	Interrupt request signal.
B	4-bit register	SK2	10-bit stack register	←	Shows direction of data flow.
C	3-bit register	CY	1-bit carry flag	( )	Indicates contents of the register, memory, etc.
E	8-bit register	xx	2-bit binary variable	∀	Exclusive OR
H	4-bit register	yyyy	4-bit binary variable	−	Negation.
J	1-bit register	nnnn	4-bit binary constant	X	Indicates flag is unaffected by instruction execution.
L	4-bit register	i	1-bit binary constant	xy	Label used to indicate the address xxxyyyy
X	2-bit register	jj	2-bit binary constant	pxy	Label used to indicate the address xxxyyyy of page pppp.
Y	4-bit register	XXXX	4-bit unknown binary number	CPS	Indicates which data pointer and carry are active.
DP	6-bit data pointer, combination of registers X and Y.	D	11-bit port	C	Hexadecimal number C + binary number x.
PC_H	The high-order three bits of the program counter.	K	11-bit port	+	
PC_L	The low-order seven bits of the program counter.	S	8-bit port	×	
PC	10-bit program counter, combination of PC_H and PC_L.	INTE	Interrupt enable flag		
SK0	10-bit stack register	INTP	Interrupt polarity flag		

Note 1. When a skip is used with either the M58843-XXXP or M58843-XXXP, the next instruction becomes invalid and the program counter is not incremented by 2. Therefore the number of cycles does not change in accordance with the existence or non-existence of a a skip.In addition, since the M58843-XXXP is housed in a 28-pin package, some pins of the port K and D are not usable.

2. The M58843-XXXP and M58844-XXXSP programs are developed using a support system having a 2048 word × 9-bit ROM memory. When using such a system, page 8 through 15 of the 2048 words (page 0 through 15) are used so that the program counter $PC_H = 0 \sim 7$ is defined as page 8 through 15.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{DD}	Supply voltage	With respect to V_{SS}	0.3～−20	V
V_I	Input voltage, port S and D, X_{IN} and V_P inputs		0.3～−35	V
V_I	Input voltage, other than port S and D, X_{IN} and V_P inputs		0.3～−20	V
V_O	Output voltage, ports S and D		0.3～−35	V
V_O	Output voltage, other than ports S and D		0.3～−20	V
P_d	Power dissipation	Ta=25℃	1100	mW
Topr	Operating temperature		−10～70	℃
Tstg	Storage temperature		−40～125	℃

RECOMMENDED OPERATING CONDITIONS (Ta = -10～70°C, unless otherwise noted)

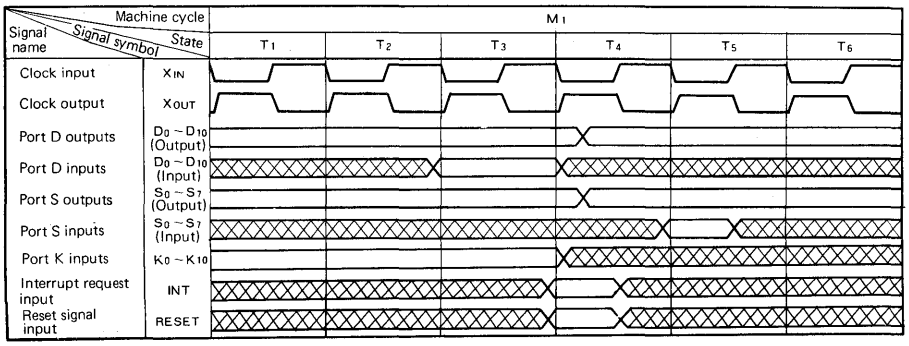
Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{DD}	Supply voltage	−13.5	−15	−16.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage , port D	−1		0	V
V_{IH}	High-level input voltage other than port D	−1.5		0	V
$V_{IH(\phi)}$	High-level clock input voltage	−1.5		0	V
V_{IL}	Low-level input voltage, RESET and INT (Schmitt)	V_{DD}		$V_{DD}+2$	V
V_{IL}	Low-level input voltage, INT (TTL compatible)	V_{DD}		−4.2	V
V_{IL}	Low-level input voltage, ports D and S	−33		−4.2	V
$V_{IL(\phi)}$	Low-level clock input voltage	−33		$V_{DD}+2$	V
$V_{I(K)}$	Digital input voltage, port K	V_{DD}		0	V
$V_{I(K)}$	Analog input voltage, port K	V_{REF}		0	V
V_{REF}	Reference voltage	−5		−7	V
V_{OL}	Low-level output voltage, ports D and S	−33		0	V
f(ϕ)	Internal clock oscillation frequency	300		600	kHz

ELECTRICAL CHARACTERISTICS (Ta = -10～70°C, VDD= -15V ±10%, VSS=0V, f(ϕ)=300～600kHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{T-}	Negative threshold voltage, RESET input	$V_{DD}=-15V$, $T_a=25℃$	$V_{DD}+2$		−4	V
$V_{T+}-V_{T-}$	Hysteresis, RESET input	$V_{DD}=-15V$, $T_a=25℃$		1		V
V_{OH}	High-level output voltage, port D	$V_{DD}=-15V$, $I_{OH}=-15mA$,	−2.5			V
V_{OH}	High-level output voltage, port S	$V_{DD}=-15V$, $I_{OH}=-8mA$,	−2.5			V
I_{IH}	High-level input current, port K (with pull-down resistors)	$V_{DD}=-15V$, $V_{IH}=0V$, $T_a=25℃$	50		250	μA
I_{IH}	High-level input current, ports D and S (with pull-down resistors)	$V_P=-33V$, $V_{IH}=0V$, $T_a=25℃$	80		280	μA
I_I	Input current, port K	To be measured when the instruction CPAS or CPA is not being executed; V_I = -7V		−1	−7	μA
$I_{I(\phi)}$	Clock input current	$V_{I(\phi)}=-33V$, $T_a=25℃$		−20	−40	μA
I_{OH}	High-level output current, port D	$V_{DD}=-15V$, $V_{OH}=-2.5V$,			−15	mA
I_{OH}	High-level output current, port S	$V_{DD}=-15V$, $V_{OH}=-2.5V$,			−8	mA
I_{OL}	Low-level output current, ports D and S	$V_{OL}=-33V$, $T_a=25℃$			−33	μA
I_{DD}	Supply current	$V_{DD}=-15V$, $T_a=25℃$		−27	−41	mA
I_{REF}	Reference current	$V_{REF}=-7V$, $T_a=25℃$			−1	mA
I_P	Pull-down supply current	$V_P=-33$, $T_a=25℃$			−5.5	mA
C_i	Input capacitance, port K	$V_{DD}=V_I=V_0=V_{SS}$, f=1MHz 25mVrms		7	10	pF
$C_{i(\phi)}$	Clock input capacitance	$V_{DD}=X_{OUT}=V_{SS}$, f=1MHz 25mVrms		7	10	pF
	A-D conversion linearity error	$V_{REF}=-7V$	Overall	±2	±3	LSB
	A-D conversion zero error					
	A-D conversion fullscale error					

Note 1. Currents are taken as positive when flowing into the IC (zero-signal conditions) with the minimum and maximum values as absolute values.
2. The overall sum of the port D high-level output currents should be kept below 75mA.

BASIC TIMING DIAGRAM



Note 3. The crosshatched area indicates invalid input.

MITSUBISHI ELECTRIC

M58845-XXXSP

SINGLE-CHIP 4-BIT MICROCOMPUTER WITH 8-BIT A/D CONVERTER AND TWO TIMER/EVENT COUNTER

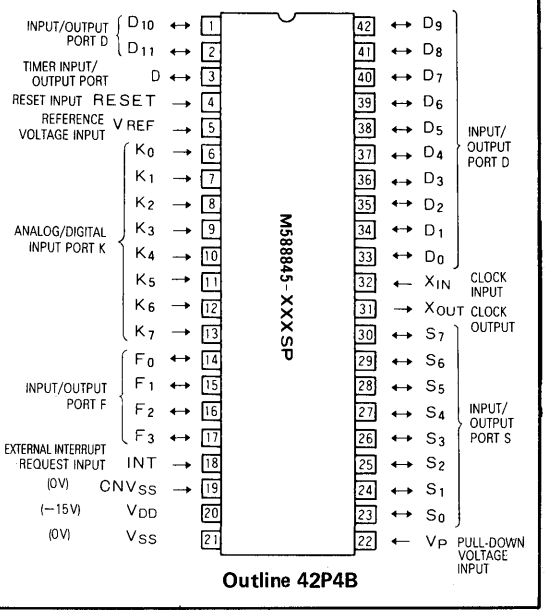
DESCRIPTION

The M58845-XXXSP is a single-chip 4-bit microcomputer developed using p-channel aluminum gate ED-MOS technology. The device includes an 8-bit A-D converter and two timers (one 8-bit timer/counter and one 8-bit timer/event counter). It is housed in a 42-pin shrink plastic molded DIL package.

FEATURES

- Basic machine instructions 77
- Basic instruction execution time (1-word instruction at a clock frequency of 600kHz) 10μs
- Memory capacity ROM: ..... 2048 words x 9 bits
  RAM: ..... 128 words x 4 bits
- Single −15V power supply
- Built-in 8-bit A-D converter (12 analog inputs)
- Two built-in timers (timer 1: 8-bit timer/counter, timer 2: 8-bit timer/event counter, 7-bit prescaler, timer input/output port T) ..... 2 lines
- Interrupt function
  ..... 3 factors (external, timer 1, timer 2), 1 level
- Two built-in data pointers
- Subroutine nesting ..... 3 levels
- Analog/digital inputs (port K) ..... 8 ports
- Input/output (ports D, F, and S) ..... 24 ports
- Timer input/outputs (port T) ..... 1 port
- Direct drive for large fluorescent display tubes is possible
- Built-in decoder PLA for port S outputs (mask option)
- Built-in pull-down transistors (ports D, K, and S mask option)
- Built-in clock generator circuit

PIN CONFIGURATION (TOP VIEW)

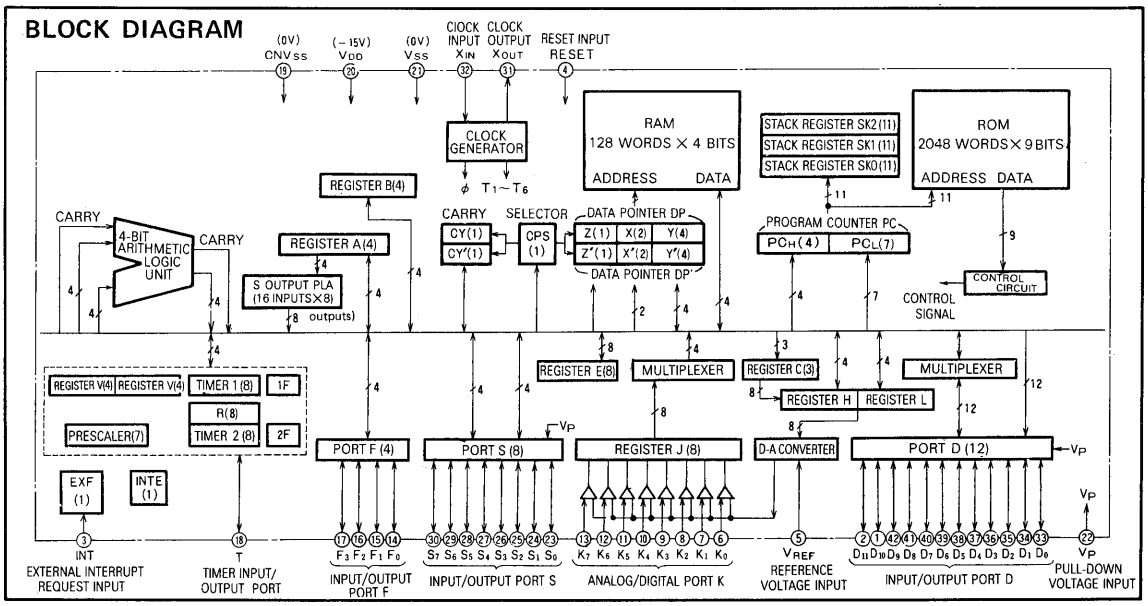


Outline 42P4B

APPLICATIONS

- Microwave ovens, air conditioners, heaters, home sewing machines
- Office equipment, copying machines, medical equipment
- VTR, TVs, cassette decks
- Educational equipment, electronic games

BLOCK DIAGRAM



PERFORMANCE SPECIFICATIONS

Parameter			Performance
Basic machine instructions			77
Instruction execution time (1-word instructions)			10μs (with a clock frequency of 600kHz)
Clock frequency			300 ~ 600kHz
Memory capacity	ROM		2048 words x 9 bits
	RAM		128 words x 4 bits
Input/output ports, and interrupt request inputs (34 lines)	K(Note 1)	Input	1 bit x 8 or 4 bits x 2 (analog/digital)
	D(Note 2)	Input	1 bit x 12
		Output	1 bit x 12
	F	Input	4 bits x 1
		Output	4 bits x 1
	S(Note 2)	Input	4 bits x 2
		Output	8 bits x 1
	T (Note 3)	Input	1 bit x 1
		Output	1 bit x 1
	INT(external interrupt request)(Note 3)		1 bit x 1
A-D conversion circuit			Built-in (accuracy±2LSB)
Timers (2)			Timer 1: 8-bit timer/counter Timer 2: 8-bit timer/event counter 7-bit prescaler, timer input/output port
Pull-down voltage input pin			Used for driving devices such as large fluorescent display tubes (ports D and S)
Subroutine nesting			3 levels
Interrupts			3 factors (external, timer 1, timer 2), 1 level
Clock generator			Built-in (for use with externally connected RC circuit or ceramic resonator)
I/O characteristics of ports	Port D		−33V input/output withstanding voltage, output current −15mA
	Port S		−33V input/output withstanding voltage, output current −8mA
	Ports other than D and S		−20V input/output withstanding voltage, output current −6mA
Supply voltage			−15V (typ)
Device structure			p-channel aluminum gate ED-MOS
Package			42-pin silicon plastic molded DIL package
Power dissipation (excluding ports)			350mW (typ)

Note 1. Built-in pull-down transistors and discharge transistors (mask options)
2. Built-in pull-down transistors (mask option)
3. Input characteristics mask option (TTL compatible, with a Schmitt circuit)

PIN DESCRIPTION

Pin	Name	Input or output	Function
V_{SS}	Ground		Connected to 0V potential
V_{DD}	Supply voltage		Connected to a −15V supply
V_P	Pull-down supply	In	Input for the supply voltage connected to the load resistors (mask option) for ports D and S
$K_7 \sim K_0$	I/O port K	In	This port can be used for analog and digital input, acting as 8 individual bit inputs or 2 4-bit input groups. Pull-down transistors and input discharge transistors are available as mask options.
$D_{11} \sim D_0$	I/O port D	In/out	Port D consists of a 12-bit input/output port, all bits operating individually. When a port D output is programmed low, the output floats and the input signal can be sensed. The outputs are open drain circuits which can be provided with pull-down transistors as a mask option.
$F_3 \sim F_0$	I/O port F	In/out	Port F is a 4-bit input/output port. When the output is programmed to low, the output floats and the input signal can be sensed. The output circuits are open drain circuits.
$S_7 \sim S_0$	I/O port S	In/out	The I/O port S can be used as either an 8-bit output port or a pair of 4-bit input ports. When the output port S is programmed to the low level, it remains in the floating state so that it can be used as an input port.
T	Timer I/O port T	In/out	This port is used as the timer to event counter input, and the timer to overflow output, the function being software selectable.
INT	Interrupt request input	In	This is the input for interrupt requests.
RESET	Reset	In	When this input is kept high for at least 3 machine cycles, the reset state is enabled.
V_{REF}	Reference voltage input	In	This is the input for the reference voltage required by the D-A converter.
X_{IN}	Clock input	In	These are the input and output pins for the built-in clock generator. A ceramic resonator (300 kHz ~ 600 kHz) or a resistor/capacitor combination are connected to these pins to provide the required oscillation stability.
X_{OUT}	Clock output	Out	
CNV_{SS}	CNV_{SS}	In	This input is connected to V_{SS} and must have a high-level input applied to it (0V).

4

BASIC FUNCTION BLOCKS

Program Memory (ROM)

This 2048-word x 9-bit ROM can be programmed with machine instruction codes in accordance with the customer's specifications. It consists of 16 pages, each containing an address range of 0~127. Fig. 1 shows the address map for this ROM.

Program Counter (PC)

This counter is used to specify ROM addresses and the sequence of read-out of instructions stored in ROM. The program counter is an 11-bit counter, the upper order 4 bits of which (PC_H) indicate the ROM page, and the lower 7 bits of which are a pure binary address designation. Each time an instruction is executed, PC_L is incremented by 1 step. For branching and subroutine call instructions, its value is set to the designated address.

When the 127 address is reached for every page, the address value returns to the first address of that page. Therefore, for moving from one page to another page, the page byte itself must be modified. This is done using the **BL** and **BLA** instructions.

Page 2 and page 3 are special pages used for subroutine calls. Page 2 can be called with a 1-word instruction from any arbitrary page. This instruction is either **BM** or **BMA**. When either **BM** or **BMA** is executed, subsequent **BM** or **BMA** instructions are equivalent to **B** and **BA** on page 2. Also, **B** or **BA** is equivalent to **B** or **BA** on page 3. This condition is cancelled when the **RT, RTS, BL, BML, BLA,** or **BMLA** instruction is executed. Table 3 shows the instruction codes and corresponding states.

Stack Registers (SK_0, SK_1, SK_2)

These registers are used to temporarily store the contents of the PC while executing subroutines or interrupt programs until the program returns to its original routine. The SK registers are organized in 3 words of 11 bits each, enabling up to 3 levels of subroutine nesting. If 1 level is used for an interrupt routine, the remaining 2 levels can be used for subroutine calls.

Data Memory (RAM)

This 512-bit (128 words x 4 bits) RAM is used to store both processing and control data. One RAM word consists of 4 bits with bit manipulation possible over the entire storage area. The 128 words are arranged as 2 file groups x 4 files x 16 digits x 4 bits. Fig. 2 shows the RAM address map. The RAM address specification is made by the combination of data pointer DP register Z, register X, and register Y. Thus, the selector CPS and data pointer DP must be set. However, as long as the address is not changed this is not necessary.

Data Pointers (DP, DP')

These registers are used to designate the RAM address, and bit position for the I/O port D and register J. Each data pointer is composed of a 7-bit register. Register Z (the most significant bit of DP) designates the RAM file group; register X (the central 2 bits) designates the RAM file; and register Y (the least significant 4 bits) designates the digit position of the RAM file. At the same time, register Y designates the bit positions of the I/O port D and register J.

4-Bit Arithmetic Logic Unit (ALU)

This unit executes 4-bit arithmetic and logical operations by means of a 4-bit adder and related logic circuitry.

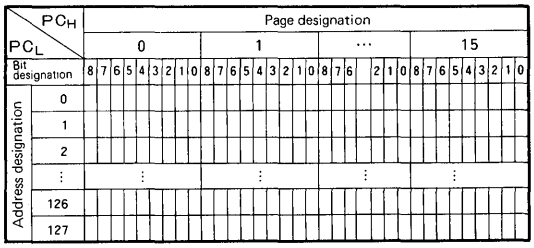


Fig. 1 ROM Address map

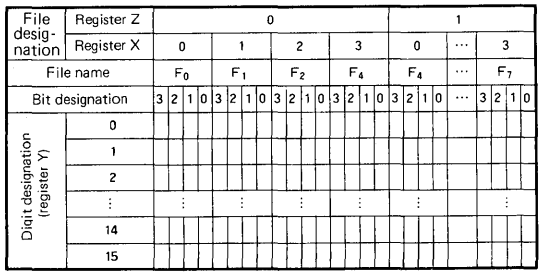


Fig. 2 RAM Address map

Register A and Carry Flag (CY)

Register A is a 4-bit accumulator that constitutes the basis for arithmetic operations. Data processing operations such as arithmetic and logical operations, data transfer, exchange, conversion, and data input/output are executed by means of this register. The carry flag CY is used to store carry or overflow after execution of arithmetic and logical operations by the arithmetic logic unit. The carry flag may also be used as a 1-bit flag. Two carry flags, CY and CY', are available and selected by selector CPS, as is the data pointer DP.

Registers B and E

Register B is composed of 4 bits and can be used as a 4-bit temporary storage register or for 8-bit data transfer in conjunction with register A. Register E is composed of 8 bits and is used not only as an 8-bit temporary storage register, but also as a temporary for the I/O port S.

A/D Conversion Circuit

The following A-D conversion functions are controlled by software as described below.

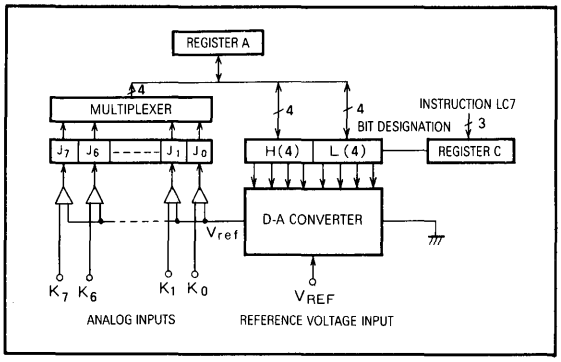


Fig. 3 A-D conversion circuit block diagram

(1) Comparators

The comparators are implemented entirely with PMOS devices and use a chopper-type amplification method. They are capable of determining the larger of the D-A converter output V_{ref} and the port K input signals $V_K(Y)$ (where $(Y)=0\sim7$).

(2) Register J

Register J is composed of 8 1-bit registers, each representing the comparison result from the comparators. All register bits are set simultaneously. The value of the register J with respect to the comparison results is as follows.

1 when $|V_{ref}| > |V_K(Y)|$
0 when $|V_{ref}| < |V_K(Y)|$

In this relationship Y represents the bit position in register J which is designated by register Y. The comparison results can be checked for each bit using the SZJ instruction.

(3) Registers H and L

These two 4-bit registers are capable of transferring and exchanging data to and from register A. The 8-bit digital data for the D-A converter is transferred from these registers, the higher order 4 bits from H and the lower order 4 bits from L.

(4) Register C

This 3-bit register is used as a counter to designate bit positions in the H and L registers.

(5) D-A Converter

The D-A converter converts the digital values stored in the registers H and L, referencing with the external reference voltage V_{REF} applied at the pin V_{REF}, to the analog value of the internal reference voltage V_{ref}. The theoretical value of the internal reference voltage V_{ref} if defined as follows.

$$Vref = \frac{n-0.5}{256} \times V_{REF}, \text{ where, } n = 1, 2, \ldots\ldots 255$$

$$Vref = 0 \quad , \text{where, } n = 0$$

In the above relationships n is the value weighted according to the contents of registers H and L.

A/D Conversion Algorithms

A/D conversion is controlled by the programming of the previously described functional blocks. Thus, by modifying the program, either the successive approximation method or the sequential comparision method may be selected. In addition, a digital input of high or low level may be used to select the method, eliminating the software selection of the A/D conversion technique.

(1) Successive Approximation Method
In this method, the conversion speed is maintained at a constant 600kHz regardless of the amplitude of the analog signal. The A/D conversion process requires 0.6ms. 12 program words are required.

(2) Sequential Comparison Method
In this method the conversion speed varies in accordance with the rate of change of the analog quantity. When the rate of change is slow, the conversion rate increases. 30 program words are required.

Interrupt Functions

The M58845-XXXSP provides 3-factor, 1-level vector interrupt capability, enabling unique branching addresses for each interrupt factor.

The interrupt vector addresses are shown in Table 1.

Table 1 Vector Interrupt Addresses

Interrupt factor		Interrupt address
Interrupt type	Causal condition	
External interrupt	Rising edge at the INT input pin	Page 1, address 0
Timer 1 interrupt	Timer 1 overflow	Page 1, address 2
Timer 2 interrupt	Timer 2 overflow	Page 1, address 4

An interrupt is generated whenever any of the causal conditions listed in Table 1 are satisfied at a time when the INTE flag is set to 1 (when the EI instruction is executed the INTE flag is set to 1, enabling interrupt; the DI instruction clears this flag to 0, prohibiting interrupts). If any of the interrupt causing conditions continues when the INTE flag is 0, an interrupt is generated when the INTE flag is set to 1.

The interrupts generated as a result of timer 1 and timer 2 overflow conditions can be software controlled, allowing confirmation of the overflow condition using a skip instruction.

When an interrupt program is used, one level of the three-level stack register is required, the remaining two levels being used for subroutines. After the interrupt program is started, the data pointer DP, register A, carry flag CY, and registers used by the interrupt program are saved. The **RTI** instruction is required to restore these before returning to the main program.

When an interrupt occurs, the microcomputer internal states are as follows.

(1) Program counter
The current address in the main program is stored in a stack register and the vector interrupt address as shown in Table 4 is loaded into the program counter.

(2) Interrupt flag INTE
The flag INTE is reset to disable further interrupts. This disabled state will continue even after return to the main program by the **RTI** instruction until the execution of an **EI** instruction.

(3) Skip flags
Skip flags are provided to discriminate skip instructions and consecutively described skip instructions. Each flag has its own stack within which the skip state is saved. As a mask option, the interrupt pins may be provided with Schmitt input circuits.

Timer/Event Counter (2 Lines)

The timer/event counter section consists of two lines (timers). As shown in Fig. 8, this section includes timer 1 and its overflow flag (1F) and timer 2 and its overflow flag (2F), as well as the timer input/output port T and the timer control registers V and W.

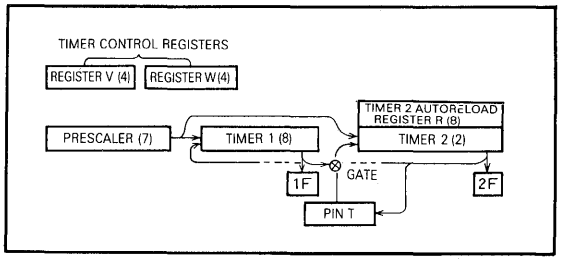


Fig. 4 Timer/event counter block diagram

The two timers (timer 1 and 2) are controlled by means of the timer control registers.

(1) Timer 1
Timer 1 is implemented using an 8-bit binary counter capable of being set and read by means of the **T1AB** and **TAB1** instructions respectively. Starting and stopping of the counter as well as the selection of the source (prescaler or timer 2) is accomplished by means of the timer control register. When an overflow condition occurs, setting the 1F to 1 stops the

counting operation.

(2) Timer 2

Time 2 is implemented using an 8-bit binary counter and is provided with an auto-reload register (register R). Timer 2 data can be read using the **TAB2** instruction and register R may be set as well as ready by means of the **TRAB** and **TABR** instructions respectively. Starting and stopping the counter as well as the selection of the source (prescaler or external input from port T) is controlled by the timer control registers. In addition, when port T has been chosen as the source, if only timer 1 is counting, gating is possible by means of using counter enabling controlled by the timer control registers. The overflow condition results in the setting of the flag 2F, after which timer 2 can be set with data once more by register R (auto-reload register) and continue counting.

(3) Prescaler

The overflow time can be selected as either 160μs or 1270μs (when using a 600kHz clock frequency) by means of the counter control registers.

(4) Timer I/O port T

This port can be selected by the counter control register as the source for timer 2. In addition, when another source has been selected, a pulse is available at this port every time timer 2 reaches the overflow condition.

(5) Timer 1 and 2 overflow flags 1F and 2F

These flags are set when the corresponding timer has reached the overflow condition. To test these flags, generation of an interrupt and skip instructions (**SNZ1, SNZ2**) can be used. The selection of which will be used is made by the timer control registers. By using either, these flags will be reset.

(6) Timer control registers V and W

The timer control registers are used to perform the above described control functions. Instructions **TVA** and **TWA** are used to transfer control data to these register.

Input/Output Ports

(1) Port K (K_7~K_0)

This analog/digital input port is capable of 8-bit input using the **SZJ** instruction and two groups of 4-bit inputs using the **IAS i** instruction. The analog signal may be A/D converted using either successive approximation or sequential comparison, as determined by the program. Also, an arbitrary threshold level in the range 0~−7V with respect to the digital signal may be input, enabling the use of the port as a high-noise immunity input.

Pull-down transistors and discharge transistors (for use with capacity touch-type keys) may be selected as mask options.

(2) Port D (D_{11}~D_0)

This port consists of 12 bits which can be used for both input and output functions by means of the **SZD, SD,** and **RD** instructions. The output section provides individual bit latching and the contents of register Y can be used to designate a single bit of port D for output or sensing. When using the port for input, the output must be cleared to 0 first. The instructions **CLD** and **CLDS** can be used to clear all bits of the port to 0. The outputs are open-drain circuits which can be provided with pull-down transistors as a mask option.

(3) Port F (F_3~F_0)

This 4-bit port is controlled for output and input by the **OFA** and **IAF** instructions respectively. When using a bit for input, that bit output must first be set to 0. The outputs are open drain circuits.

(4) Port S (S_7~S_0)

This port can perform 8-bit output using the **OSAB, OSPA,** and **OSE** instructions and 4-bit input using the **IAS i** instruction.

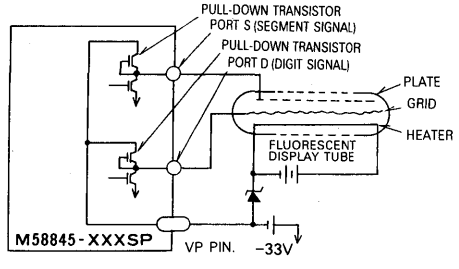
A built-in S output PLA has been provided which can code 4 bits of register A data arbitrarily and provide output using the **OSPA** instruction. The PLA output coding is a mask option.

When the port is used for input, the outputs must first be set to 0. All the port S bits may be set to 0 by means of the **CLS** or **CLDS** instructions.

The outputs are open-drain circuits which can be provided with pull-down transistors as a mask option.

V_P Pin

This pin is used to supply the required voltage for the port D and port S pull-down transistors. Built-in pull-down transistors can be provided as a mask option for driving



Note 1. The M58845-XXXSP can be used to directly drive fluorescent display tubes demanding up to −33V of output level.
Note 2. To provide complete blanking, the heater should be provided with a voltage of approximately 4 V from the VP pin.

Fig. 5 Fluorescent display tube drive circuit

fluorescent display tubes, as shown in Fig. 5, eliminating the need for the usual externally connected pull-down resistors and resulting in a reduction in the number of system components.

Reset

When the RESET pin is kept high for at least 3 machine cycles, the reset state is enabled. After reset has been performed, when the RESET input is driven low, program execution will begin at page 0, address 0.

When the reset state is enabled, the following operations are performed.

(1) The program counter is set to 0, address 0, (PC) ← 0
(2) The interrupt mode is in the disabled state. INTE ← 0 (the same as for the execution of the **DI** instruction)
(3) The carry and data pointer selector is set to 0, specifying DP and CY.
(4) Registers V and W are set to 0. V=W ← 0_{16}
(5) The 3 interrupt flags, external interrupt flag (EXF), timer 1 overflow flag (1F), and timer 2 overflow flag (2F) are reset. EXF=1F=2F ← 0
(6) All outputs of port D are cleared to low (D) ← 0
(7) All outputs of port F are cleared to low (F) ← 0
(8) All outputs of port S are cleared to low (S) ← 0
(9) All outputs of port T are cleared to low (T) ← 0

Clock Generator Circuits

A clock generator circuit has been built in, to allow control of the frequency by means of an externally connected RC circuit or ceramic resonator. In addition, an external clock signal may be applied at the X_{IN} pin, leaving the X_{OUT} pin open. Circuit examples are shown in Fig. 6~8.

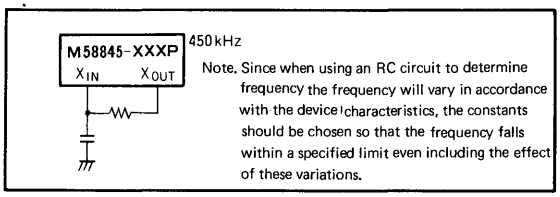


Fig. 6 External RC circuit

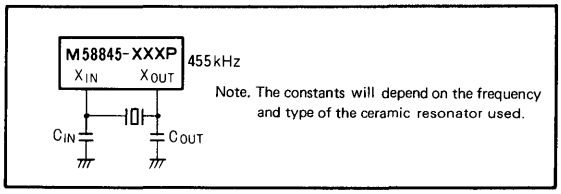


Fig. 7 Externally connected ceramic resonator

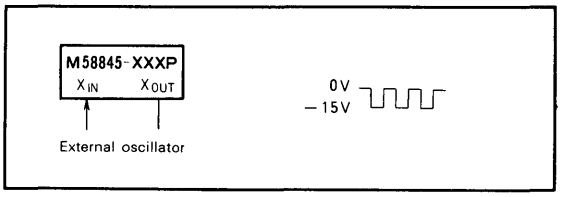


Fig. 8 External clock input circuit

Mask Options

The following mask options are available, specifiable at the time of initial ordering.

(1) S output PLA data
(2) Port K (K_7~K_0) discharge transistors
(3) Port K (K_7~K_0) pull-down transistors
(4) Port D (D_{11}~D_0) pull-down transistors
(5) Port S (S_7~S_0) pull-down transistors
(6) Selection of interrupt input TTL-compatible Schmitt circuits
(7) Selection of RESET input TTL-compatible Schmitt circuits
(8) Selection of port T TTL-compatible Schmitt circuits

Documentation Required upon Ordering

The following information should be provided when ordering a custom mask.

(1) M58845-XXXSP mask confirmation sheet
(2) ROM data — 3 EPROM sets
(3) S output PLA coding — On confirmation sheets
(4) Port K input discharge transistors — On confirmation sheets
(5) Port K pull-down transistors
(6) Port D pull-down transistors
(7) Port S pull-down transistors
(8) Selection of interrupt input TTL-compatible Schmitt circuits
(9) Selection RESET input TTL-compatible Schmitt circuits
(10) Selection of Port T input TTL-compatible Schmitt circuits

MACHINE INSTRUCTIONS

Type of instruction	Mnemonic	Instruction code D_8 $D_7D_6D_5D_4$ $D_3D_2D_1D_0$	16mal notation	No. of words	No. of cycles	Functions	Skip conditions	Flag CY	Description of operation
Register-to-register transfers	**TAB**	0 0001 1110	0 1E	1	1	(A)←(B)	—	X	Transfers contents of register B to register A.
	TBA	0 0001 1100	0 1C	1	1	(B)←(A)	—	X	Transfers contents of register A to register B.
	TAY	0 0001 1101	0 1D	1	1	(A)←(Y)	—	X	Transfers contents of register Y to register A.
	TYA	0 0000 1100	0 0C	1	1	(Y)←(A)	—	X	Transfers contents of register A to register Y.
	TEAB	0 0001 1010	0 1A	1	1	$(E_7 \sim E_4) \leftarrow (B)$ $(E_3 \sim E_0) \leftarrow (A)$	—	X	Transfer contents of registers A and B to register E.
	TEPA	0 0001 0110	0 16	1	1	$(E_7 \sim E_0) \leftarrow$ through PLA$\leftarrow (A)$	—	X	Decodes contents of register A in the PLA and transfers result to register E.
RAM addresses	**LXY x, y**	0 11xx yyyy	0 CY + x	1	1	(X)←x where, x=0~3 (Y)←y where, y=0~15	Written successively	X	Loads value of "x" into register X, and of "y" into Y. When LXY is written successively the first is executed and successive ones are skipped.
	LZ z	0 0100 101z	0 4A + z	1	1	(Y)←z where, z=0,1	—	X	Loads value of "z" into register Z.
	INY	0 0000 0010	0 02	1	1	(Y)←(Y)+1	(Y)=0	X	Increments contents of register Y by 1. Skips next instruction when new contents of register Y are "0".
	DEY	0 0000 0011	0 03	1	1	(Y)←(Y)−1	(Y)=15	X	Decrements contents of register Y by 1. Skips next instruction when new contents of register Y are "15".
	LCPS i	0 0100 000i	0 4i	1	1	(CPS)←i where, i=0,1	—	X	Transfers designated contents of register J to register A.
RAM-accumulator transfers	**TAM j**	0 0110 01jj	0 64 + j	1	1	(A)←(M(DP)) $(X) \leftarrow (X) \forall j$ where, j=0~3	—	X	Transfers the RAM contents addressed by the active DP to register A. Register X is then "exclusive OR-ed" with the value j in the instruction, and the result stored in register X.
	XAM j	0 0110 00jj	0 6j	1	1	(A)←→(M(DP)) $(X) \leftarrow (X) \forall j$ where, j=0~3	—	X	Exchanges the contents of the RAM DP and register A. Contents of X are then "exclusive OR-ed" with the value j, and the result stored in register X.
	XAMD j	0 0110 10jj	0 68 + j	1	1	(A)←→(M(DP)) (Y)←(Y)−1 $(X) \leftarrow (X) \forall j$ where, j=0~3	(Y)=15	X	Exchanges the contents of the RAM and register A. Contents of X are then "exclusive OR-ed" with the value j in the instruction, and the result stored in register X. The contents of register Y are decremented by 1, and when the result is 15, the next instruction is skipped.
	XAMI j	0 0110 11jj	0 6C + j	1	1	(A)←→(M(DP)) (Y)←(Y)+1 $(X) \leftarrow (X) \forall j$ where, j=0~3	(Y)=0 (Y)=masked skip condition	X	Exchanges the contents of the RAM and register A. Contents of X are then "exclusive OR-ed" with the value j in the instruction and result stored in register X. The contents of register Y are incremented by 1, and when the result meets the next instruction is skipped with the marked skip condition.
Arithmetic operations	**LA n**	0 1011 nnnn	0B n	1	1	(A)←n where, n=0~15	Written successively	X	Loads the value n into register A. When LA is written consecutively the first is executed, and successive ones are skipped.
	AM A	0 0000 1010	0 0A	1	1	(A)←(A)+(M(DP))	—	X	Adds the contents of the RAM to register A. The result is retained in register A, and the contents of flag CY are unaffected.
	AMC	0 0100 0011	0 43	1	1	(A)←(A)+(M(DP))+(CY) CY←Carry	—	0/1	Adds the RAM contents addressed by the active DP and contents of flag CY to register A. The result is stored in register A and the carry in the active flag CY.
	AMCS	0 0101 0011	0 53	1	1	(A)←(A)+(M(DP))+(CY) CY←Carry	— A carry is not produced and	0/1	Adds the contents of the RAM and flag CY to register A. The result is stored in register A and the carry in the CY, but the next instruction is skipped when a carry is produced.
	A n	0 1010 nnnn	0 An	1	1	(A)←(A)+n where, n=0~15	=0 n≠6	X	Adds value n in the instruction to register A. The contents of flag CY are unaffected and their next instruction is skipped if a carry is not produced, except when n=6.
	SC	0 0100 1001	0 49	1	1	(CY)←1	—	1	Sets active flag CY.
	RC	0 0100 1000	0 48	1	1	(CY)←0	—	0	Resets active flag CY.
	SZC	0 0010 1111	0 2F	1	1		(CY=0)	X	Skips next instruction when contents of the active flag CY are 0.
	CMA	0 0000 1111	0 0F	1	1	(A)←($\overline{A}$)	—	X	Stores complement of register A in register A.
Bit operations	**SB j**	0 0100 11jj	0 4C + j	1	1	$(M_j(DP)) \leftarrow 1$ where, j=0~3	—	X	Sets the jth bit of the RAM addressed by the active DP (the bit designated by the value j in the instruction).
	RB j	0 0101 11jj	0 5C + j	1	1	$(M_j(DP)) \leftarrow 0$ where, j=0~3	—	X	Resets the jth bit of the RAM addressed by the active DP (the bit designated by the value j in the instruction).
	SZB j	0 0010 00jj	0 2j	1	1		$(M_j(DP))=0$ where, j=0~3	X	Skips next instruction when the contents of the jth bit of the RAM addressed by the active DP (the bit which is designated by the value j in the instruction) are 0.
Compares	**SEAM**	0 0010 0110	0 26	1	1		(M(DP))=(A)	X	Skips next instruction when contents of register A are equal to the RAM contents addressed by the active DP.
	SEY y	0 0011 yyyy	0 3y	1	1		(Y)=y where, y=0~15	X	Skips next instruction when the contents of register Y are equal to the value y in the instruction.
A/D converter operations	**TLA**	0 0001 1001	0 19	1	1	(L)←(A)	—	X	Transfers contents of register A to register L.
	THA	0 0101 1001	0 59	1	1	(H)←(A)	—	X	Transfers contents of register A to register H.
	XAL	0 0001 1000	0 18	1	1	(A)←→(L)	—	X	Exchanges contents of register A with contents of register L.
	XAH	0 0101 1000	0 58	1	1	(A)←→(H)	—	X	Exchanges contents of register A with contents of register H.
	LC7	0 0101 0111	0 57	1	1	(C)←7	—	X	Loads 7 to register C.
	DEC	0 0000 1001	0 09	1	1	(C)←(C)−1	(C)=7	X	Decrements contents of register C by 1, when result is 7, skips
	SHL	0 0100 0010	0 42	1	1	$(C_2)=1$ when : $(H(C_1 \sim C_0)) \leftarrow 1$ $(C_2)=0$ when : $(L(C_1 \sim C_0)) \leftarrow 1$	—	X	Sets the bit in register L or H designated by register C. The box instruction shows the relationship between register C and bit position.
	RHL	0 0101 0010	0 52	1	1	$(C_2)=1$ when : $(H(C_1 \sim C_0)) \leftarrow 0$ $(C_2)=0$ when : $(L(C_1 \sim C_0)) \leftarrow 0$	—	X	Resets the bit in register L or H that is designated by register C.
	CPA	0 0000 1000	0 08	1	2	$\lvert Vref \rvert > \lvert V_{K(i)} \rvert$ when : $(J(i)) \leftarrow 1$ $\lvert Vref \rvert < \lvert V_{K(i)} \rvert$ when : $(J(i)) \leftarrow 0$ i=0~7	—	X	Reads all analog values from input port K for comparison with D-D-A converter output V_{ref}, and either sets the respective bit of register J to the next instruction cycle, wherever $V_{ref} > V_{K(1)}$ is true, or resets it, wherever $V_{ref} < V_{K(1)}$ is true.
	CPAS	0 0101 0001	0 51	1	1	$\lvert Vref \rvert > \lvert V_{K(i)} \rvert$ when : $(J(i)) \leftarrow 1$ $\lvert Vref \rvert < \lvert V_{K(i)} \rvert$ when : $(J(i)) \leftarrow 0$	—	X	Reads and stores temporarily all analog values from input port K, which are then unaffected by changes in port K inputs. These values are compared with the D-A converter output V_{ref}, calculated from contents of registers H and L, and respective bits of register J are set/reset. Repeated when contents of registers H-L are changed.

(C)	7	6	5	4	3	2	1	0
Bit	H_3	H_2	H_1	H_0	L_3	L_2	L_1	L_0

Type of instruction	Mnemonic	Instruction code $D_8\ D_7D_6D_5D_4\ D_3D_2D_1D_0$	16mal notation	No. of words	No. of cycles	Functions	Skip conditions	Flag CY	Description of operation
A/D converter operations	**CPAE**	0 0101 0000	0 50	1	1	Execution of the instruction CPAS is over, and no more changes will made in $(J_{(Y)})$	—	X	Terminates execution of instruction CPAS Contents of register J remain unaffected, maintaining the value immediately before termination, and input port K is again ready to receive input.
	TAJ	0 0000 1101	0 0D	1	1	$(Y_0)=0$ when : $(A)\leftarrow(J_3\ J_2\ J_1\ J_0)$ $(Y_0)=1$ when : $(A)\leftarrow(J_7\ J_6\ J_5\ J_4)$	—	X	
	SZJ	0 0010 1001	0 29	1	1		$(J(y))=0$	X	Skips next instruction when the bit in register J, designated by register Y, is 0.
Timer operation	**T1AB**	0 1000 0100	0 84	1	1	$(1_7\sim1_4)\leftarrow(B)$ $(1_3\sim1_0)\leftarrow(A)$	—	X	Transfers contents of register A and register B to timer 1.
	TRAB	0 1000 0101	0 85	1	1	$(R_7\sim R_4)\leftarrow(B)$ $(R_3\sim R_0)\leftarrow(A)$	—	X	Transfers contents of register A and register B to timer 2 auto reload register R.
	TAB1	0 1000 1000	0 88	1	1	$(B)\leftarrow(1_7\sim1_4)$ $(A)\leftarrow(1_3\sim1_0)$	—	X	Transfers contents of timer 1 to register A and register B.
	TABR	0 1000 1001	0 89	1	1	$(B)\leftarrow(R_7\sim R_4)$ $(A)\leftarrow(R_3\sim R_0)$	—	X	Transfers contents of timer 1 auto reload register R to register A and register B.
	TAB2	0 1000 1010	0 8A	1	1	$(B)\leftarrow(2_7\sim2_4)$ $(A)\leftarrow(2_3\sim2_0)$	—	X	Transfers contents of timer 2 to register A and register B.
	TVA	0 1000 0110	0 86	1	1	$(V)\leftarrow(A)$	—	X	Transfers contents of register A to timer control register V.
	TWA	0 1000 0111	0 87	1	1	$(W)\leftarrow(A)$	—	X	Transfers contents of register A to timer control register W.
	SNZ1	0 1000 0010	0 82	1	1		$(1F)=1$	X	Skips the next instruction if flag 1F is 1.
	SNZ2	0 1000 0011	0 83	1	1		$(2F)=1$	X	Skips the next instruction if flag 2F is 1.
Branch	**B xy**	1 1xxx yyyy	1 8y + x	1	1	$(PC_L)\leftarrow16x+y$	—	X	Jumps to address xy of the current page.
						$(PC_H)\leftarrow3$, $(PC_L)\leftarrow16x+y$			Jumps to address xy on page 3 when executed, provided that none of instruction RT, RTS, BL, BML, BLA or BMLA was executed after execution of instruction BM or BMA.
	BL pxy	0 0111 PPPP 1 1xxx yyyy	0 7P 1 8y + x	2	2	$(PC_H)\leftarrow p$ $(PC_L)\leftarrow16x+y$	—	X	Jumps to address xy of page p.
	BA xy	0 0000 0001 1 1xxx XXXX	0 01 1 8X × x	2	2	$(PC_L)\leftarrow16x+(A)$	—	X	Subroutine on the current page. Exchange the lower 4 bits of the contents of address xX with the contents of register A and branch to address 16x+A
						$(PC_H)\leftarrow3$, $(PC_L)\leftarrow16x+(A)$			Page 3 subroutine: After execution of a BM or BMA instruction without execution of a RT, RTS, BL, BML, BLA, or BMLA instruction, when a BA instruction is executed branching is done to address 16x+(A) on page 3
	BLA pxy	0 0000 0001 0 0111 PPPP 1 1xxx XXXX	0 01 0 7P 1 8X + x	3	3	$(PC_H)\leftarrow p$ $(PC_L)\leftarrow16x+(A)$	—	X	Subroutine on a different page: Exchange the lower 4 bits of the contents of address xX with the contents of register A and branch to the address 16x+(A)
Subroutine calls	**BM xy**	1 0xxx yyyy	1 xy	1	1	$(SK_2)\leftarrow(SK_1)\leftarrow(SK_0)\leftarrow(PC)$ $(PC_H)\leftarrow2$, $(PC_L)\leftarrow16x+y$	—	X	Calls for the subroutine starting at address x(A) of page 2.
						$(PC_H)\leftarrow2$, $(PC_L)\leftarrow16x+y$			Jumps to address xy of page 2 provided that none of instructions. RT, RTS, BL, BML, BLA or BMLA was executed after the execution of instructions BM or BMA.
	BML pxy	0 0111 PPPP 1 0xxx yyyy	0 7P 1 xy	2	2	$(SK_2)\leftarrow(SK_1)\leftarrow(SK_0)\leftarrow(PC)$ $(PC_H)\leftarrow p$, $(PC_L)\leftarrow16x+y$	—	X	Calls for the subroutine starting at address xy of page p.
	BMA xX	0 0000 0001 1 0xxx XXXX	0 01 1 xX	2	2	$(SK_2)\leftarrow(SK_1)\leftarrow(SK_0)\leftarrow(PC)$ $(PC_H)\leftarrow2$, $(PC_L)\leftarrow16x+(A)$	—	X	Calls for the subroutine starting at address x(A) of page 2.
						$(PC_H)\leftarrow2$, $(PC_L)\leftarrow16x+(A)$			Jumps to address x(A) of page 2 provided that none of instructions. RT, RTS, BL, BML, BLA or EMLA was executed after the execution of instructions BM or BMA.
	BMLA pxX	0 0000 0001 0 0111 PPPP 1 0xxx XXXX	0 01 0 7P 1 xX	3	3	$(SK_2)\leftarrow(SK_1)\leftarrow(SK_0)\leftarrow(PC)$ $(PC_H)\leftarrow p$, $(PC_L)\leftarrow16x+(A)$	—	X	Calls for the subroutine starting at address x(A) of page p.
Program returns	**RTI**	0 0100 0110	0 46	1	1	$(PC)\leftarrow(SK_0)\leftarrow(SK_1)\leftarrow(SK_2)$	—	X	Returns from interrupt routine to main routine. The internal flip-flop is restored to the value held immediately before the interrupt.
	RT	0 0100 0100	0 44	1	1	$(PC)\leftarrow(SK_0)\leftarrow(SK_1)\leftarrow(SK_2)$	—	X	Returns to the main routine from the subroutine.
	RTS	0 0100 0101	0 45	1	1	$(PC)\leftarrow(SK_0)\leftarrow(SK_1)\leftarrow(SK_2)$		X	Returns to the main routine from the subroutine, and unconditionally skips the next instruction.
Input/output	**CLD**	0 0001 0011	0 13	1	1	$(D)\leftarrow0$	—	X	Clears port D. (low level output)
	CLS	0 0001 0000	0 10	1	1	$(S)\leftarrow0$	—	X	Clears port S.
	CLDS	0 0001 0001	0 11	1	1	$(D)\leftarrow0$ $(S)\leftarrow0$	—	X	Clears ports S and D.
	SD	0 0001 0101	0 15	1	1	$(D(Y))\leftarrow1$ where, $Y=0\sim11$	—	X	Sets the bit of port D that is designated by register Y.
	RD	0 0001 0100	0 14	1	1	$(D(Y))\leftarrow0$ where, $Y=0\sim11$	—	X	Resets the bit of port D that is designated by register Y.
	SZD	0 0010 1011	0 2B	1	1		$(D(Y))=0$ where, $Y=0\sim11$	X	Skips the next instruction if the contents of the bit of port D that is designated by register Y are 0.
	OSAB	0 0001 1011	0 1B	1	1	$(S_7\sim S_4)\leftarrow(B)$ $(S_3\sim S_0)\leftarrow(A)$	—	X	Output contents of registers A and B to port S.
	OSPA	0 0001 0111	0 17	1	1	$(S_7\sim S_4)\leftarrow$ through PLA$\leftarrow(A)$	—	X	Decodes contents of register A by PLA and the result is output to ports.
	OSE	0 0000 1011	0 0B	1	1	$(S)\leftarrow(E)$	—	X	Outputs contents of register E to port S.
	IAS i	0 0101 010i	0 54 + j	1	1	$i=0(A)\leftarrow(S_7\sim S_4)$ $i=1(A)\leftarrow(S_3\sim S_0)$	—	X	Transfers from port S to register A. The high-order four bits of port S are transferred when the value of i in the instruction is 0 or the low-order four bits are transferred when the value of i is 1.
	OFA	0 1000 0001	0 81	1	1	$(F)\leftarrow(A)$	—	X	Sets interrupt flag INTE to enable interrupts.
	IAF	0 1000 1100	0 8C	1	1	$(A)\leftarrow(F)$	—	X	Resets interrupt flag INTE to disable interrupts.
Interrupts	**EI**	0 0000 0101	0 05	1	1	(INTE)$\leftarrow1$		X	Outputs contents of register A to port F.
	DI	0 0000 0100	0 04	1	1	(INTE)$\leftarrow0$		X	Transfers input from port F to register A.
Misc	**NOP**	0 0000 0000	0 00	1	1	$(PC_L)\leftarrow(PC_L)+1$		X	No operation.

4

Symbol	Contents	Symbol	Contents	Symbol	Contents
A	4-bit register (accumulator)	SK_0	11-bit stack register	←	Shows direction of data flow
B	4-bit register	SK_1	11-bit stack register	( )	Indicates contents of register, memory, etc.
C	3-bit register	SK_2	11-bit stack register	xx	2-bit binary variable
E	8-bit register	1	Timer 1	yyyy	4-bit binary variable
H	4-bit register	2	Timer 2	z	1-bit binary variable
J	8-bit register	CY	1-bit carry flag	nnnn	4-bit binary variable
L	4-bit register	INTE	Interrupt enable flag	i	1-bit binary constant
R	8-bit timer 2 auto reload register	CPS	Indicates which data pointer and carry are active	jj	2-bit binary constant
V	4-bit register	1F	1-bit timer 1 overflow flag	XXXX	4-bit unknown bibary number
W	4-bit register	2F	1-bit timer 2 overflow flag	⊻	Exclusive-OR
X	2-bit register	EXF	1-bit external interrupt flag	−	Negation
Y	4-bit register	D	12-bit port	X	Indicates flag is uneffected by instruction execution
Z	1-bit register	F	4-bit port	xy	Label used to indicate the address XXXYYYY
DP	7-bit data pointer, combination of registers X, Y, and Z	K	8-bit port	pxy	Label used to indicate the address XXXYYYY of page PPPP
PC_H	The high-roder 4-bits of the program counter	S	8-bit port	C	Hexadecimal number C + binary number x
PC_L	The low-order 7-bits of the program counter	T	1-bit port	+	
PC	11-bit program counter, combination of PC_H and PC_L	INT	i Interrupt request signal	x	

Note 1. When a skip has occurred, the next instruction only is ignored and the program counter is not incremented by 2, therefore, the number of cycles does not change in accordance with the existence or non-existence of skip

INSTRUCTION CODE TABLE

D_8–D_4 / Hexadecimal number C / D_3–D_0		0 0000	0 0001	0 0010	0 0011	0 0100	0 0101	0 0110	0 0111	0 1000	0 1001	0 1010	0 1011	0 1100	0 1101	0 1110	0 1111	1 0000 ↓ 1 0111	1 1000 ↓ 1 1111
		0 0	0 1	0 2	0 3	0 4	0 5	0 6	0 7	0 8	0 9	0 A	0 B	0 C	0 D	0 E	0 F	10～17	18～1F
0000	0	NOP	CLS	SZB 0	SEY 0	LCPS 0	CPAE	XAM 0	BL BML	−	−	A 0	LA 0	LXY 0,0	LXY 1,0	LXY 2,0	LXY 3,0	BM	B
0001	1	BA BMA BLA BMLA	CLDS	SZB 1	SEY 1	LCPS 1	CPAS	XAM 1	BL BML	OFA	−	A 1	LA 1	LXY 0,1	LXY 1,1	LXY 2,1	LXY 3,1	BM	B
0010	2	INY	−	SZB 2	SEY 2	SHL	RHL	XAM 2	BL BML	SNZ1	−	A 2	LA 2	LXY 0,2	LXY 1,2	LXY 2,2	LXY 3,2	BM	B
0011	3	DEY	CLD	SZB 3	SEY 3	AMC	AMCS	XAM 3	BL BML	SNZ2	−	A 3	LA 3	LXY 0,3	LXY 1,3	LXY 2,3	LXY 3,3	BM	B
0100	4	DI	RD	−	SEY 4	RT	IAS 0	TAM 0	BL BML	T1AB	−	A 4	XA 4	LXY 0,4	LXY 1,4	LXY 2,4	LXY 3,4	BM	B
0101	5	EI	SD	−	SEY 5	RTS	IAS 1	TAM 1	BL BML	TRAB	−	A 5	LA 5	LXY 0,5	LXY 1,5	LXY 2,5	LXY 3,5	BM	B
0110	6	−	TEPA	SEAM	SEY 6	RTI	−	TAM 2	BL BML	TVA	−	A 6	LA 6	LXY 0,6	LXY 1,6	LXY 2,6	LXY 3,6	BM	B
0111	7	−	OSPA	−	SEY 7	−	LC7	TAM 3	BL BML	TWA	−	A 7	LA 7	LXY 0,7	LXY 1,7	LXY 2,7	LXY 3,7	BM	B
1000	8	CPA	XAL	−	SEY 8	RC	XAH	XAMD 0	BL BML	TAB1	−	A 8	LA 8	LXY 0,8	LXY 1,8	LXY 2,8	LXY 3,8	BM	B
1001	9	DEC	TLA	SZJ	SEY 9	SC	THA	XAMD 1	BL BML	TABR	−	A 9	LA 9	LXY 0,9	LXY 1,9	LXY 2,9	LXY 3,9	BM	B
1010	A	AM	TEAB	−	SEY 10	LZ 0	−	XAMD 2	BL BML	TAB2	−	A 10	LA 10	LXY 0, 10	LXY 1, 10	LXY 2, 10	LXY 3, 10	BM	B
1011	B	OSE	OSAB	SZD	SEY 11	LZ 1	−	XAMD 3	BL BML	−	−	A 11	LA 11	LXY 0,11	LXY 1,11	LXY 2,11	LXY 3,11	BM	B
1100	C	TYA	TBA	−	SEY 12	SB 0	RB 0	XAMI 0	BL BML	IAF	−	A 12	LA 2	LXY 0,12	LXY 1,12	LXY 2,12	LXY 3,12	BM	B
1101	D	TAJ	TAY	−	SEY 13	SB 1	RB 1	XAMI 1	BL BML	−	−	A 13	LA 13	LXY 0,13	LXY 1,13	LXY 2,13	LXY 3,13	BM	B
1110	E	−	TAB	−	SEY 14	SB 2	RB 2	XAMI 2	BL BML	−	−	A 14	LA 14	LXY 0,14	LXY 1,14	LXY 2,14	LXY 3,14	BM	B
1111	F	CMA	−	SZC	SEY 15	SB 3	RB 3	XAMI 3	BL BML	−	−	A 15	LA 15	LXY 0,15	LXY 1,15	LXY 2,15	LXY 3,15	BM	B

Note 1: This list shows the machine codes and corresponding machine instructions. D_3~D_0 indicate the low-order 4 bits of the machine code and D_8~D_4 indicate the high-order 5 bits. Hexadecimal numbers are also shown that represent the codes An instruction may consist of one, two, or three words, but only the first word is listed. Code combination indicated with a bar (-) must not be used.

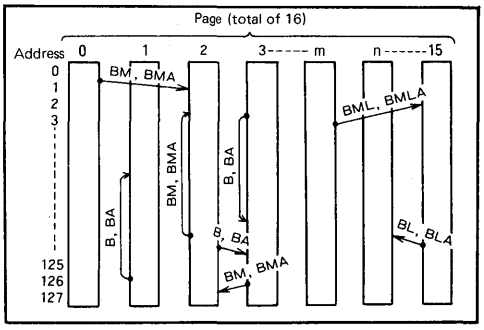
Note 2: Two-word instruction

	Second word
BL	1 1xxx yyy
BML	1 0xxx yyyy
BA	1 1xxx XXXX
BMA	1 0xxx XXXX

Three-word instruction

	Second word	Third word
BLA	0 0111 pppp	1 1xxx XXXX
BM	0 0111 pppp	1 0xxx XXXX

Note 3. Relationships between branching and page by means of branching instructions and subroutine calling instructions.



4

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{DD}	Supply voltage	With respect to V_{SS}	0.3~−20	V
V_I	Input votage (ports D and S, and input VP)		0.3~−35	V
V_I	Input voltage, inputs other than ports D and S, and input VP		0.3~−20	V
V_O	Output voltage, ports D and S		0.3~−35	V
V_O	Output voltage, other outputs than ports D and S		0.3~−20	V
Pd	Power dissipation	Ta=25°C	1100	mW
Topr	Operating temperature		−10~70	°C
Tstg	Storage temperature		−40~125	°C

RECOMMENDED OPERATING CONDITIONS (Ta = -10 ~ 70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{DD}	Supply voltage	−13.5	−15	−16.5	V
V_{SS}	Supply voltage		0		V
V_P	Pull-down transistor supply voltage	0		−33	V
V_{IH}	High-level input voltage	−1.5		0	V
$V_{IH}(\phi)$	High-level clock input voltage	−1.5		0	V
V_{IL}	Low-level input voltage, inputs other than ports D and S	V_{DD}		−4.2	V
V_{IL}	Low-level input voltage ports D and S	−33		−4.2	V
$V_{IL}(\phi)$	Low-level clock input votlage	V_{DD}		$V_{DD}+2$	V
$V_I(K)$	Analog input voltage, port K	V_{REF}		0	V
$V_I(K)$	Digital input voltage, port K	V_{DD}		0	V
V_{REF}	Reference voltage	−5		−7	V
V_{OL}	Low-level output voltage, ports D and S	−33		0	V
$f(\phi)$	Internal clock oscillation frequency	300		600	kHz

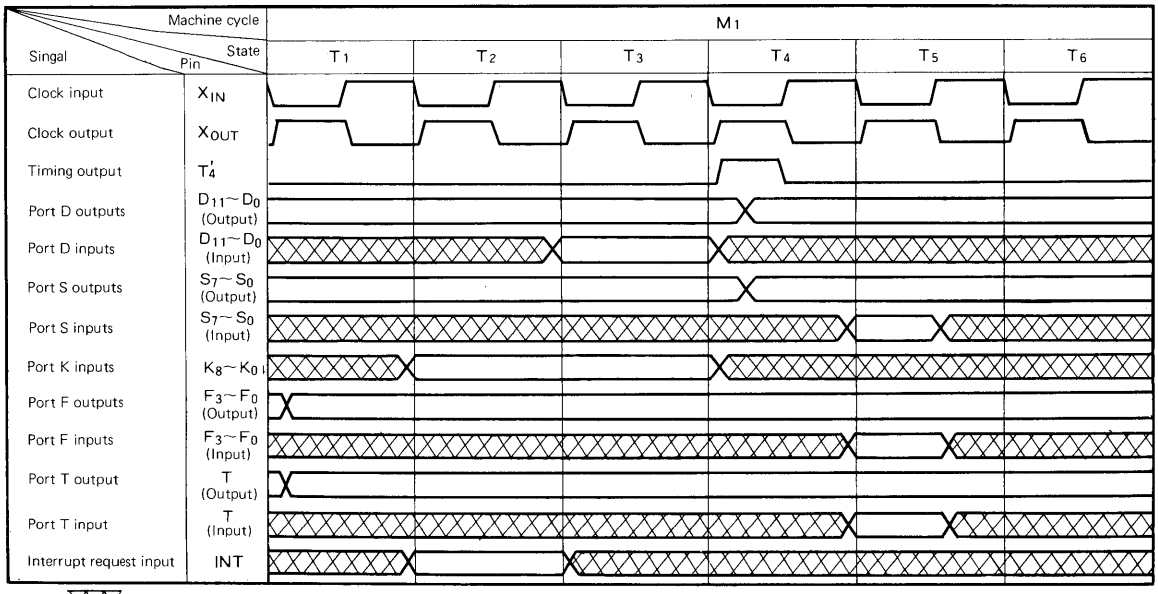
Note 4. $V_{IL}(\phi)$ is specified for the maximum V_{DD} value.

ELECTRICAL CHARACTERISTICS (T_a = -10 ~ 70°C, V_{DD} = -15±10%, V_{SS} = 0V, f(φ) = 300 ~ 600 kHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{OH}	High-level output voltage, port D	V_{DD} = −15V, I_{OH} = −15mA, Ta = 25°C	−2.5			V
V_{OH}	High-level output voltage, ports S and F	V_{DD} = −15V, I_{OH} = −8mA (port S) I_{OH} = −6mA (Port F), Ta = 25°C	−2.5			V
V_{T-}	Negative threshold voltage (Schmitt input mask option)	V_{DD} = −15V, Ta = 25°C	−7		−4	V
$V_{T+}-V_{T-}$	Hysteresis (Schmitt input mask option)	V_{DD} = −15V, Ta = 25°C	1.5		3.5	V
I_I	Input current, port K	Measured when not executing CPA or CPAS V_I = −7V		− 1	−7	μA
I_{IH}	High-level input current, port K (with pull-down resistors)	V_{DD} = −15V, V_{IH} = 0V, Ta = 25°C	50		250	μA
I_{IH}	High-level input current, ports D and S (with pull-down resistors)	V_P = −33V, V_{IH} = 0V, Ta = 25°C	80		280	μA
$I_{I(\phi)}$	Clock input current	$V_{I(\phi)}$ = −15V, Ta = 25°C		−20	−40	μA
I_{OH}	High-level output current, port D (Note 2)	V_{DD} = −15V, V_{OH} = −25V, Ta = 25°C			−15	mA
I_{OH}	High-level output current, ports S and F	V_{DD} = −15V, V_{OH} = −25V, Ta = 25°C		−6 (port F) −8 (port S)		mA
I_{OL}	Low-level output current, ports D and S	V_{OL} = −33V, Ta = 25°C			−33	μA
I_{OL}	Low-level output current, port F	V_{DD} = −15V, Ta = 25°C			−33	μA
I_{DD}	Supply current	V_{DD} = −15V, Ta = 25°C		21		mA
I_{REF}	Reference supply current	V_{REF} = −7V, Ta = 25°C			−1	mA
C_i	Input capacitance, port K	V_{DD} = V_I = V_O = V_{SS}, f = 1MHz, 25mVrms		7	10	pF
$C_{i(\phi)}$	Clock input capacitance	V_{DD} = X_{OUT} = V_{SS}, f = 1MHz, 25mVrms		7	10	pF
	A-D conversion linearity error	V_{REF} = −7V	Overall	± 2	± 3	LSB
	A-D conversion zero error					
	A-D conversion fullscale error					

Note 1. Currents are taken as positive when flowing into the IC (zero signal condition), with the minimum and maximum values as absolute values.
2. It is possible to connect up to 5 lines of the port D at maximum ratings (-15mA) or all lines of port S and F at maximum ratings of -8mA and -6mA respectively.

BASIC TIMING DIAGRAM



Note 3. ⨯⨯⨯ The crosshatch area indicates invalid input.

M58846-XXXSP

SINGLE-CHIP 4-BIT MICROCOMPUTER WITH TWO TIMER/EVENT COUNTER

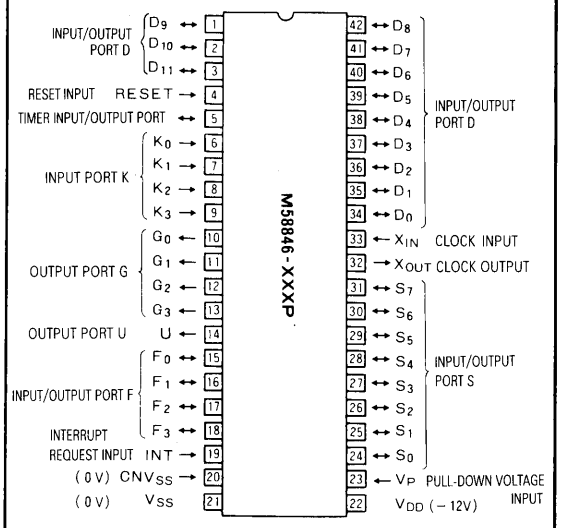
DESCRIPTION

The M58846-XXXSP is a single-chip 4-bit microcomputer developed using p-channel aluminum gate ED-MOS technology. The device includes two timers (one 7-bit timer and one 8-bit timer/event counter). It is housed in a 42-pin shrink plastic molded DIL package.

FEATURES

- Basic machine instructions 65
- Basic instruction execution time (1-word instruction at a clock frequency of 600kHz) 10μs
- Memory capacity ROM: ..... 2048 words x 9 bits
  RAM: ..... 128 words x 4 bits
- Single −12V power supply
- Two built-in timers (timer 1: 7-bit timer/counter, timer 2: 8-bit timer/event counter) ..... 2 lines
- Interrupt function .....
  3 factors (external, timer 1, timer 2), 1 level
- Two built-in data pointers
- Subroutine nesting ..... 3 levels
- Input (port K) ..... 4 lines
- Input/output (ports D, F, and S) ..... 24 lines
- Output (ports G and U) ..... 5 lines
- Timer input/output (port T) ..... 1 line
- Direct drive for large fluorescent display tubes is possible
- Built-in decoder PLA for port S outputs (mask option)
- Built-in pull-down transistors (ports D, K, and S mask option)
- Built-in clock generator circuit

PIN CONFIGURATION (TOP VIEW)

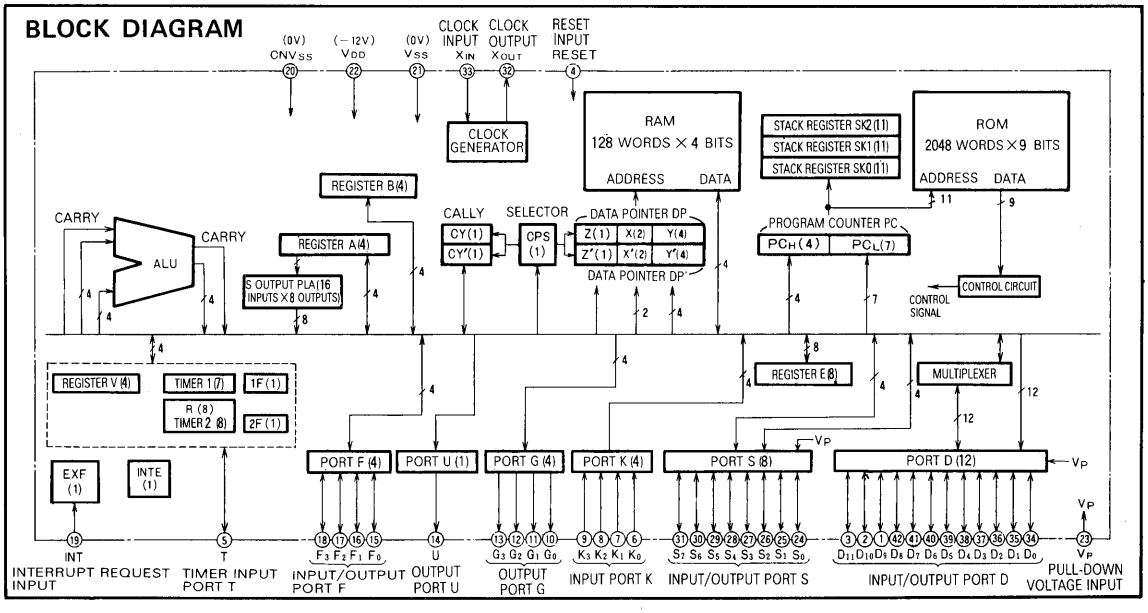


Outline 42P4B

APPLICATIONS

- VTRs, TVs, cassette decks
- Office equipment, copying machines, medical equipment
- Educational equipment, games

BLOCK DIAGRAM



PERFORMANCE SPECIFICATIONS

Parameter			Performance
Basic machine instructions			65
Instruction execution time (1-word instructions)			10 μs (with a clock frequency of 600kHz)
Clock frequency			300 ~ 600kHz
Memory capacity	ROM		2048 words x 9 bits
	RAM		128 words x 4 bits
Input/output ports	K (Note 1)	Input	4 bits x 1
	D (Note 2)	Input	1 bit x 12
		Output	1 bit x 12
	F	Input	4 bits x 1
		Output	4 bits x 1
	S (Note 2)	Input	4 bits x 2
		Output	8 bits x 1
	G	Output	4 bits x 1
	U	Output	1 bit x 1
	T (Note 1)	Input	1 bit x 1
		Output	1 bit x 1
	INT (external interrupt request) (Note 1)		1 bit x 1
Timers			Timer 1: 7-bit timer Timer 2: 8-bit timer/event counter, timer input output port T
Pull-down voltage input pin			Used for driving devices such as large fluorescent display tubes (ports D and S)
Subroutine nesting			3 levels
Interrupts			3 factors (external, timer 1, timer 2), 1 level
Clock generator			Built-in
I/O characteristics of ports	Port D		−33V input/output withstanding voltage, output current −15mA
	Port S		−33V input/output withstanding voltage, output current −8mA
	Ports other than D and S		−20V input/output withstanding voltage, output current −6mA
Supply voltage			−12V (Typ)
Device structure			p-channel aluminum gate ED-MOS
Package			42-pin silicone plastic molded DIL package
Power dissipation (excluding ports)			280mW (typ)

Note 1. Input characteristics mask option (TTL-compatible Schmitt circuit)
2. Built-in pull-down transistors (mask options)

PIN DESCRIPTION

Pin	Name	Input or output	Function
V_{SS}	Ground		Connected to 0V potential
V_{DD}	Supply voltage		Connected to a −12V supply
V_P	Pull-down supply	In	Input for the supply voltage connected to the load resistors (mask option) for ports D and S
$K_3 \sim K_0$	Input port K	In	This port can be used to perform 4-bit TTL-compatible or Schmitt input. Pull-down transistors and input discharge transistors are available as mask options.
$D_{11} \sim D_0$	I/O port D	In/out	Port D consists of a 12-bit input/output port, all bits operating individually. When a port D output is programmed low, the output floats and the input signal can be sensed. The outputs are open drain circuits which can be provided with pull-down transistors as a mask option.
$F_3 \sim F_0$	I/O port F	In/out	Port F is a 4-bit input/output port. When the output is programmed to low, the output floats and the input signal can be sensed. The output circuits are open drain circuits.
$S_7 \sim S_0$	I/O port S	In/out	The I/O port S can be used as either an 8-bit output port or a pair of 4-bit input ports. When the output port S is programmed to the low level, it remains in the floating state so that it can be used as an input port.
$G_3 \sim G_0$	Output port G	Out	This is a 4-bit output port.
U	Output port U	Out	This is a 1-bit output port.
T	Timer I/O port T	In/out	This port is used as the timer 2 event counter input and the timer 2 overflow output, the functions being software selectable.
INT	Interrupt request input	In	This is the input for interrupt requests.
RESET	Reset	In	When this input is kept high for at least 3 machine cycles, the reset state is enabled.
X_{IN}	Clock input	In	These are the input and output pins for the built-in clock generator. A ceramic filter element (300kHz ~ 600kHz) or a resistor/capacitor combination are connected to these pins to provide the required oscillation stability.
X_{OUT}	Clock output	Out	
CNV_{SS}	CNV_{SS}	In	This input is connected to V_{SS} and must have a high-level input applied to it (0V).

4

BASIC FUNCTION BLOCKS

Program Memory (ROM)

This 2048-word x 9-bit Mask ROM can be programmed with machine instruction codes in accordance with the customer's specifications. It consists of 16 pages, each containing an address range of 0~127. Fig. 1 shows the address map for this ROM.

Program Counter (PC)

This counter is used to specify ROM addresses and the sequence of read-out of instructions stored in ROM. The program counter is an 11-bit counter, the upper-order 4 bits of which (PC_H) indicate the ROM page, and the lower 7 bits of which (PC_L) are a pure binary address designation. Each time an instruction is executed, PC_L is incremented by 1 step. For branching and subroutine call instructions, its value is set to the designated address.

When the 127 address is reached for every page, the address value returns to the first address of that page. Therefore, for moving from one page to another page, the page byte itself must be modified. This is done using the **BL** and **BLA** instructions.

Page 2 and page 3 are special pages used for subroutine calls. Page 2 can be called with a 1-word instruction from any arbitrary page. This instruction is either **BM** or **BMA**. When either **BM** or **BMA** is executed, subsequent **BM** or **BMA** instructions are equivalent to **B** and **BA** on page 2. Also, **B** or **BA** is equivalent to **B** or **BA** on page 3. This condition is cancelled when the **RT, RTS, BL, BML, BLA,** or **BMLA** instruction is executed. Note 3 shows the instruction codes and corresponding states.

Stack Registers (SK_0, SK_1, SK_2)

These registers are used to temporarily store the contents of the PC while executing subroutines or interrupt programs until the program returns to its original routine. The SK registers are organized in 3 words of 11 bits each, enabling up to 3 levels of subroutine nesting. If 1 level is used for an interrupt routine, the remaining 2 levels can be used for subroutine calls.

Data Memory (RAM)

This 512-bit (128 words x 4 bits) RAM is used to store both processing and control data. One RAM word consists of 4 bits with bit manipulation possible over the entire storage area. The 128 words are arranged as 2 file groups x 4 files x 16 digits x 4 bits. Fig. 2 shows the RAM address map. The RAM address specification is made by the combination of data pointer DP register Z, register X, and register Y. Thus, the selector CPS and data pointer DP must be set. However, as long as the address is not changed this is not necessary.

Data Pointers (DP, DP')

These registers are used to designate the RAM address, and bit position for the I/O port D and register J. Each data pointer is composed of a 7-bit register. Register Z (the most significant bit of DP) designates the RAM file group; register X (the central 2 bits) designates the RAM file; and register Y (the least significant 4 bits) designates the digit position of the RAM file. At the same time, register Y designates the bit positions of the I/O port DJ.

4-Bit Arithmetic Logic Unit (ALU)

This unit executes 4-bit arithmetic and logical operations by means of a 4-bit adder and related logic circuitry.

Register A and Carry Flag (CY)

Register A is a 4-bit accumulator that constitutes the basis for arithmetic operations. Data processing operations such as arithmetic and logical operations, data transfer, exchange, conversion, and data input/output are executed by means of this register. The carry flag CY is used to store carry or overflow after execution of arithmetic and logical operations by the arithmetic logic unit. The carry flag may also be used as a 1-bit flag. Two carry flags, CY and CY', are available and selected by selector CPS, as is the data pointer DP.

Registers B and E

Register B is composed of 4 bits and can be used as a 4-bit temporary storage register or for 8-bit data transfer in conjunction with register A. Register E is composed of 8 bits and is used not only as an 8-bit temporary storage register, but also as a temporary for the I/O port S.

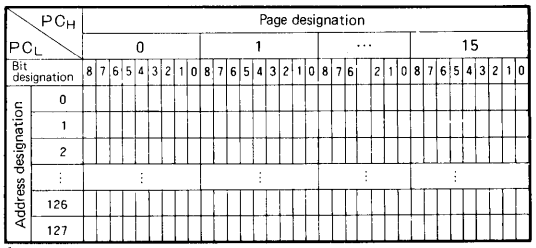


Fig. 1 ROM Address map

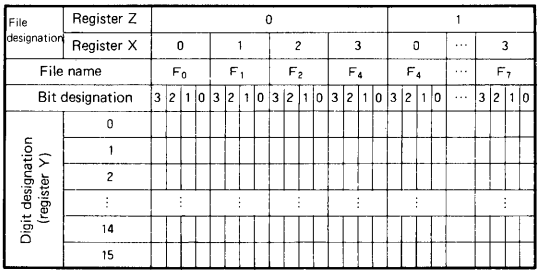


Fig. 2 RAM Address map

Interrupt Functions

The M58846-XXXSP provides 3-factor, 1-level vector interrupt capability, enabling unique branching addresses for each interrupt factor.

Interrupt factor		Interrupt address
Interrupt type	Causal condition	
External interrupt	Rising edge at the INT input pin	Page 1, address 0
Timer 1 interrupt	Timer 1 overflow	Page 1, address 2
Timer 2 interrupt	Timer 2 overflow	Page 1, address 4

Fig. 3 Vector Interrupt Addresses

The interrupt vector addresses are shown in Fig. 1.

An interrupt is generated whenever any of the casual conditions listed in Fig. 3 are satisfied at a time when the INTE flag is set to 1 (when the EI instruction is executed the INTE flag is set to 1, enabling interrupt; the DI instruction clears this flag to 0, prohibiting interrupts). If any of the interrupt causing conditions continues when the INTE flag is 0, an interrupt is generated when the INTE flag is set to 1.

The interrupts generated as a result of timer 1 and timer 2 overflow conditions can be software controlled, allowing confirmation of the overflow condition using a skip instruction.

When an interrupt program is used, one level of the three-level stack register is required, the remaining two levels being used for subroutines. After the interrupt program is started, the data pointer DP, register A, carry flag CY, and registers used by the interrupt program are saved. The instruction **RTI** is required to restore these before returning to the main program.

When an interrupt occurs, the microcomputer internal states are as follows.

(1) Program counter
The current address in the main program is stored in a stack register and the vector interrupt address as shown in Fig. 1 is loaded into the program counter.

(2) Interrupt flag INTE
The flag INTE is reset to disable further interrupts. This diabled state will continue even after return to the main program by the **RTI** instruction until the execution of an **EI** instruction.

(3) Skip flags
Skip flags are provided to discriminate skip instructions and consecutively described skip instructions. Each flag has its own stack within which the skip state is saved.

Timer/Event Counter (2 Lines)

The timer/event counter section consists of two lines (timers). As shown in Fig. 4, this section includes timer 1 and its overflow flag (1F) and timer 2 and its overflow register (register R), as well as the timer input/output port T and the timer control registers V and W.

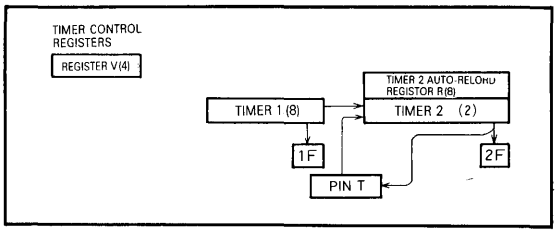


Fig. 4 Timer/event counter block diagram

The two timers (timer 1 and 2) are controlled by means of the timer control registers.

(1) Timer 1
Timer 1 is implemented using a 7-bit counter which divides the machine cycle (100kHz for a 600kHz clock frequency) by 127, setting the flag 1F every time an overflow condition occurs.
The timer is ready to count after a system reset has occured.

(2) Timer 2
Time 2 is implemented using an 8-bit binary counter and is provided with an auto-reload register (register R). Timer 2 data can be read using the **TAB2** instruction and register R may be set as well as read by means of the **T2AB** instruction. Starting and stopping the counter as well as the selection of the source (timer 1 or external input from port T) is controlled by the timer control registers. The overflow condition results in the setting of the flag 2F, after which timer 2 can be set with data once more by register R (auto-reload register) and continue counting.

(3) Timer I/O port T
This port can be selected by the counter control register as the source for timer 2. In addition, when another source has been selected, a pulse is available at this port every time timer 2 reaches the overflow condition.

(4) Timer 1 and 2 overflow flags 1F and 2F
These flags are set when the corresponding timer has reached the overflow condition. To test these flags, generation of an interrupt and skip instructions (**SNZ1**, **SNZ2**) can be used. The selection of which will be used is made by the timer control registers. By using either, these flags will be reset.

(5) Timer control registers V

The timer control register is used to perform the above described control functions. Instruction TVA is used to transfer control data to this register.

INPUT/OUTPUT PORTS

(1) Port K (K_3~K_0)

This port is capable of performing 4-bit input by means of the **IAK** instruction or single-bit input by means of the **SZK** instruction.

The port K input circuits are TTL-compatible and may be provided with Schmitt circuits as a mask option.

In addition, pull-down transistors may be provided as a mask option.

(2) Port D (D_{11}~D_0)

This port consists of 12 bits which can be used for both input and output functions by means of the **SZD**, **SD**, and **RD** instructions. The output section provides individual bit latching and the contents of register Y can be used to designate a single bit of port D for output. When using the port for input, the output must be cleared to 0 first. The instructions **CLD** and **CLDS** can be used to clear all bits of the port to 0.

The outputs are open-drain circuits which can be provided with pull-down transistors as a mask option.

(3) Port F (F_3~F_0)

This 4-bit port is controlled for output and input by the **OFA** and **IAF** instructions respectively. When using a bit for input, that bit output must first be set to 0. The outputs are open-drain circuits.

(4) Port S (S_7~S_0)

This port can perform 8-bit output using the **OSAB**, **OSPA**, and **OSE** instructions and 4-bit input using the **IAS** instruction.

A built-in S output PLA has been provided which can code 4 bits of register A data arbitrarily and provide output using the **OSPA** instruction. The PLA output coding is a mask option.

When the port is used for input, the outputs must first be set to 0. All the port S bits may be set to 0 by means of the **CLS** and **CLDS** instructions.

The outputs are open-drain circuits which can be provided with pull-down transistors as a mask option.

(5) Port G (G_3~G_0)

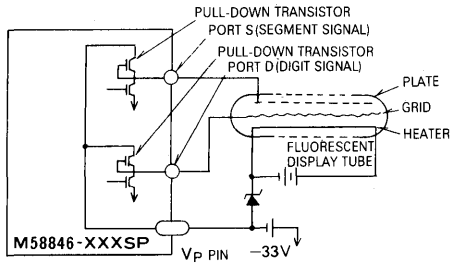
This port can be used to perform 4-bit output by means of the **OGA** instruction. The outputs are open-drain circuits.

(6) Port U

This port can be used to perform 1-bit output by means of the **SU** and **RU** instructions. The outputs are open-drain circuits.

VP PIN

This pin is used to supply the required voltage for the port D and port S pull-down transistors. Built-in pull-down transistors can be provided as a mask option for driving fluorescent display tubes, as shown in Fig. 5, eliminating the need for the usual externally connected pull-down resistors and resulting in a reduction in the number of system components.



Note 1. M58846-XXXSP can be used to directly drive fluorescent display tudes demanding up to −33 V of output level.
2. To provide complete blanking, the heater should be provided with a voltage of approximately 4V from the VP pin.

Fig.5 Fluorescent display tube drive circuit

RESET

When the RESET pin is kept high for at least 3 machine cycles, the reset state is enabled. After reset has been performed, when the RESET input is driven low, program execution will begin at page 0, address 0.

When the reset state is enabled, the following operations are performed.

(1) The program counter is set to 0, address 0. (PC) ← 0

(2) The interrupt mode is in the disabled state. INTE ← 0 (the same as for the execution of the **DI** instruction)

(3) The carry and data pointer selector CPS is set to 0, specifying DP and CY.

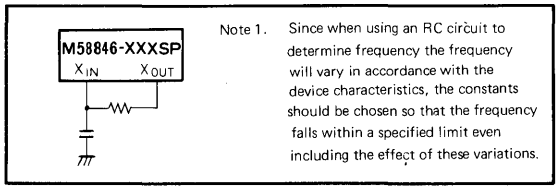
(4) Register V is set to 0. V← 0_{16}

(5) The 3 interrupt flags, external interrupt flag (EXF), timer 1 overflow flag (1F), and timer 2 overflow flag (2F) are reset. EXF=1F=2F ← 0

(6) All outputs of ports D, F, S, G, U, and T are cleared to low (D)=(F)=(S)=(G)=(T) ← 0

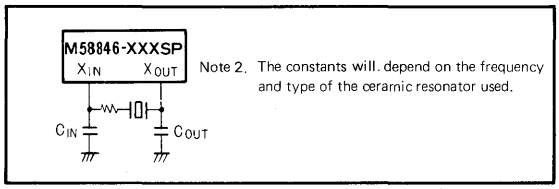
CLOCK GENERATOR CIRCUIT

A clock generator circuit has been built in, to allow control of the frequency by means of an externally connected RC circuit or ceramic resonator. In addition, an external clock signal may be applied at the X_{IN} pin, leaving the X_{OUT} pin open. Circuit examples are shown in Fig. 6~8.



Note 1. Since when using an RC circuit to determine frequency the frequency will vary in accordance with the device characteristics, the constants should be chosen so that the frequency falls within a specified limit even including the effect of these variations.

Fig. 6 External RC circuit



Note 2. The constants will depend on the frequency and type of the ceramic resonator used.

Fig. 7 Externally connected ceramic resonator

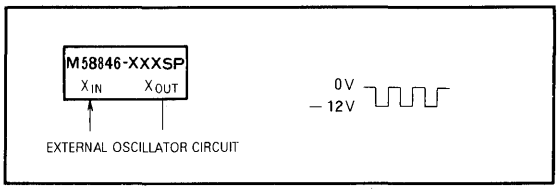


Fig. 8 External clock input circuit

MASK OPTIONS

The following mask options are available, specifiable at the time of initial ordering.

(1) Port S output PLA data
(2) Port K (K_3~K_0) pull-down transistors
(3) Port D (D_{11}~D_0) pull-down transistors
(4) Selection of port K input TTL-compatible Schmitt circuits
(5) Selection of interrupt input TTL-compatible Schmitt circuits
(6) Selection of RESET input TTL-compatible Schmitt circuits
(7) Selection of port T TTL-compatible Schmitt circuits

DOCUMENTATION REQUIRED UPON ORDERING

The following information should be provided when ordering a custom mask

(1) M58846-XXXSP mask confirmation sheet
(2) ROM data — 3 EPROM sets
(3) Port S output PLA coding — On confirmation sheets
(4) Port K pull-down transistors
(5) Port D pull-down transistors
(6) Port S pull-down transistors
(7) Selection of interrupt input TTL-compatible Schmitt circuits
(8) Selection RESET input TTL-compatible Schmitt circuits
(9) Selection of port T input TTL-compatible Schmitt circuits
(10) Selection of port K input TTL-compatible Schmitt circuits

4

MACHINE INSTRUCTIONS

Type of instruction	Mnemonic	Instruction code $D_8\ D_7D_6D_5D_4\ D_3D_2D_1D_0$	16mal notation	No. of words	No. of cycles	Functions	Skip condition	Flag CY	Description of operation
Register-to-register transfers	**TAB**	0 0001 1110	0 1E	1	1	(A)←(B)	–	x	Transfers conents of register B to register A.
	TBA	0 0001 1100	0 1C	1	1	(B)←(A)	–	x	Transfers contents of register A to register B.
	TAY	0 0001 1101	0 1D	1	1	(A)←(Y)	–	x	Transfers conents of register Y to register A.
	TYA	0 0000 1100	0 0C	1	1	(Y)←(A)	–	x	Transfers conents of register A to register Y.
	TEAB	0 0001 1010	0 1A	1	1	$(E_7 \sim E_4) \leftarrow (B)$ $(E_3 \sim E_0) \leftarrow (A)$	–	x	Transfers contents of register A and B to register E.
	TEPA	0 0001 0110	0 16	1	1	$(E_7 \sim E_0) \leftarrow$ through PLA $\leftarrow (A)$	–	x	Decodes contents of register A in the PLA and transfers result to register E.
RAM address	**LXY x,y**	0 11xx yyyy	0 Cy + x	1	1	(X)←x where x=0~3 (Y)←y where y=0~15	Written successively	x	Loads value of "x" into register X, and of "y" into Y. When LXY is written successively, the first is executed and successive ones are skipped.
	LZ z	0 0100 101z	0 4A + z	1	1	(Y)←z where z=0, 1	–	x	Loads value of "z" into register Z.
	INY	0 0000 0010	0 02	1	1	(Y)←(Y)+1	(Y)=0	x	Increments contents of register Y by 1. Skips next instruction when new contents of register Y are "0".
	DEY	0 0000 0011	0 03	1	1	(Y)←(Y)−1	(Y)=15	x	Decrements contents of register Y by 1. Skips nect instruction when new contents of register Y are "15".
	LCPS i	0 0100 000i	0 4i	1	1	(CPS)←i where i=0, 1	–	x	DP and CY are active when i=0, DP' and CY', when i=1.
RAM-accumulator	**TAM j**	0 0110 01jj	0 64 + j	1	1	(A)←(M(DP)) (X)←(X)∀, where j=0~3	–	x	Transfers the RAM contents addressed by the active DP to register A. Register X is then "exclusive OR-ed" with the value j in the instruction, and the result stored in register X.
	XAM j	0 0110 00jj	0 6j	1	1	(A)⟷(M(DP)) (X)←(X)∀j where j=0~3	–	x	Exchanges the contents of the RAM DP and register A. Contents of X are then "exclusive OR-ed" with the value j, and the result stored in register X.
	XAMD j	0 0110 10jj	0 68 + j	1	1	(A)⟷(M(DP)) (Y)←(Y)−1 (X)←(X)∀j where j=0~3	(Y)=15	x	Exchanges the contents of the RAM and register A. Contents of X are then "exclusive OR-ed" with the value j in the instruction, and the result stored in register X. The contents of register Y are decremented by 1, and when the result is 15, the next instruction is skipped.
	XAMI j	0 0110 11jj	0 6C + j	1	1	(A)⟷(M(DP)) (Y)←(Y)+1 (X)←(X)∀j where j=0~3	(Y)=0	x	Exchanges the contents of the RAM and register A. Contents of X are then "exclusive OR-ed" with the value j in the instruction and result stored in register X. The contents of register Y are incremented by 1, and when the result meets the next instruction is skipped with the marked skip condition.
Arithmetic operation	**LA n**	0 1011 nnnn	0Bn			(A)←n where n=0~15	Written successively	x	Loads the value n in to register A. When LA is written consecutively the first is executed, and successive ones are skipped.
	AM	0 0000 1010	0 0A	1	1	(A)←(A)+(M(DP))	–	x	Adds the contents of the RAM to register A. The result is retained in register A, and the conents of flag CY are unaffected.
	AMC	0 0100 0011	0 43	1	1	(A)←(A)+(M(DP))+(CY)	–	0/1	Adds the RAM contents addressed by the active DP and contents of flag CY to register A. The result is stored in register A, and the carry in the active flag CY.
	AMCS	0 0101 0011	0 53	1	1	(A)←(A)+(M(DP))+(CY) CY←Carry	(CY)=1	0/1	Adds the contents of the RAM and flag CY to register A. The result is stored in register A and the carry in the CY, but the next instruction is skipped when a carry is produced.
	A n	0 1010 nnnn	0 An	1	1	(A)←(A)+n where n=0~15	Carry=0 where n≠6	x	Adds value n in the instruction to register A. The contents of flag CY are unaffected and their next instruction is skipped a carry is not produced, except when n=6.
	SC	0 0100 1001	0 49	1	1	(CY)←1	–	1	Sets active flag CY.
	RC	0 0100 1000	0 48	1	1	(CY)←0	–	0	Resets active flag CY.
	SZC	0 0010 1111	0 2F	1	1		(CY=0)	x	Skips next instruction when contents of the active flag CY are O.
	CMA	0 0000 1111	0 0F	1	1	(A)←($\overline{A}$)	–	x	Stores complement of register A in register A.
Bit operations	**SB j**	0 0100 11jj	0 4C + j	1	1	(Mj(DP))←1 where j=0~3	–	x	Sets the jth bit of the RAM (immediate field value) addressed by the active DP (the bit designated by the value j in the instruction)
	RB j	0 0101 11jj	0 5C + j	1	1	(Mj(DP))←0 where j=0~3	–	x	Resets the jth bit of the RAM (immediate field value) addressed by the active DP (the bit designated by the value j in the instruction)
	SZB j	0 0010 00jj	0 2j	1	1		(Mj(DP))=0 where j=0~3		Skips next instruction when the contents of the jth bit of the RAM (immediate field value) addressed by the active DP (the bit which is designated by the value j in the instruction) are O.
Compares	**SEAM**	0 0010 0110	0 26	1	1		(M(DP))=(A)	x	Skips next instruction when contents of register A are equal to the RAM contents addressed by the active DP.
	SEY y	0 0011 yyyy	0 3y	1	1		(Y)=y where y=0~15	x	Skips next instruction when the content of register Y are equal to the value y in the instruction
Timer instruction	**T2AB**	0 1000 0101	0 85	1	1	$(R_7 \sim R_4) \leftarrow (B)$, $(2_7 \sim 2_4) \leftarrow (B)$ $(R_3 \sim R_0) \leftarrow (A)$, $(2_3 \sim 2_0) \leftarrow (A)$	–	x	Transfers the contents of registers A and B to timer 2 and the reload register.
	TAB2	0 1000 1010	0 8A	1	1	$(B) \leftarrow (2_7 \sim 2_4)$ $(A) \leftarrow (2_3 \sim 2_0)$	–	x	Transfers the contents of timer 2 to registers A and B
	TVA	0 1000 0110	0 86	1	1	(V)←(A)	–	x	Transfers the contents of register A to register V
	SNZ1	0 1000 0010	0 82	1	1		(1F)=1	x	Skips the next instruction when the flag 1F is 1
	SNZ2	0 1000 0011	0 83	1	1		(2F)=1	x	Skips the next instruction when the flag 2F is 1
A/D convetor operations	**B xy**	1 1xxx yyyy	1 8y + x	1	1	$(PC_L) \leftarrow 16x + y$	–	x	Jumps to address xy of the current page.
						$(PC_H) \leftarrow 3$, $(PC_L) \leftarrow 16x + y$			Jumps to address xy on page 3 when executed, provided that none of instructions, RT, RTS, BL, BML, BLA or BMLA was executed after execution of instruction BM or BMA.
	BL pxy	0 0111 PPPP 1 1xxx yyyy	0 7P 1 8y + x	2	2	$(PC_H) \leftarrow p$ $(PC_L) \leftarrow 16x + y$	–	x	Jumps to address xy of page p.
	BA xX	0 0000 0001 1 1xxx XXXX	0 01 1 8X + x	2	2	$(PC_L) \leftarrow 16x + (A)$	–	x	Jumps to address x(A) of the current page.
						$(PC_H) \leftarrow 3$, $(PC_L) \leftarrow 16x + (A)$			Jumps to the address x(A) of page 3 provided that none of instructions, RT, RTS, BL, BML, BLA or BMLA was executed alter execution of instruction BM or BMA.

Type of instruction	Mnemonic	Instruction code D_8 $D_7D_6D_5D_4$ $D_3D_2D_1D_0$	16mal notation	No. of words	No. of cycles	Functions	Skip conditions	Flag CY	Description of operation
Jumps	**BLA pxy**	0 0000 0001 0 0111 PPPP 1 1XXX XXXX	0 01 0 7P 1 8X + X	3	3	$(PC_H)\leftarrow p$ $(PC_L)\leftarrow 16x+(A)$	—	X	Jumps to the address x(A) of page p.
Subroutine calls	**BM xy**	1 0xxx yyyy	1 xy	1	1	$(SK_2)\leftarrow(SK_1)\leftarrow(SK_0)\leftarrow(PC)$ $(PC_H)\leftarrow 2,\ (PC_L)\leftarrow 16x+y$	—	X	Calls for the subroutine starting at address xX on page 2
						$(PC_H)\leftarrow 2,\ (PC_L)\leftarrow 16x+y$			Jumps to address xy of page 2 provided that none of instructions. RT, RTS, BL, BML, BLA or BMLA was executed after the execution of instructions BM or BMA.
	BML pxy	0 0111 PPPP 1 0xxx yyyy	0 7P 1 xy	2	2	$(SK_2)\leftarrow(SK_1)\leftarrow(SK_0)\leftarrow(P_C)$ $(PC_H)\leftarrow p,\ (PC_L)\leftarrow 16x+y$	—	X	Calls for the subroutine starting at address xy of page p.
	BMA xX	0 0000 0001 1 0xxx XXXX	0 01 1 XX	2	2	$(SK_2)\leftarrow(SK_1)\leftarrow(SK_0)\leftarrow(PC)$ $(PC_H)\leftarrow 2,\ (PC_L)\leftarrow 16x+(A)$	—	X	Calls for the subroutine starting at address x(A) of page 2.
						$(PC_H)\leftarrow 2,\ (PC_L)\leftarrow 16x+(A)$			Jumps to address x(A) of page 2 provided that none of instructions. RT, RTS, BL, BML, BLA or BMLA was executed after the execution of instructions BM or BMA.
	BMLA pxX	0 0000 0001 0 0111 PPPP 1 0xxx XXXX	0 01 0 7P 1 XX	3	3	$(SK_2)\leftarrow(SK_1)\leftarrow(SK_0)\leftarrow(PC)$ $(PC_H)\leftarrow p,\ (PC_L)\leftarrow 16x+(A)$	—	X	Calls for the subroutine starting at address x(A) of page p.
Program returns	**RTI**	0 0100 0110	0 46	1	1	$(PC)\leftarrow(SK0)\leftarrow(SK1)\leftarrow(SK2)$ Resets interrupt flip-flop	—	X	Returns from interrupt routine to main routine. The internal flip-flop is restored to the value held immediately before the interrupt.
	RT	0 0100 0100	0 44	1	1	$(PC)\leftarrow(SK0)\leftarrow(SK1)\leftarrow(SK2)$	—	X	Returns to the main routine from the subroutine.
	RTS	0 0100 0101	0 45	1	1	$(PC)\leftarrow(SK0)\leftarrow(SK1)\leftarrow(SK2)$	Unconditional skip	X	Returns to the main routine from the subroutine, and unconditionally skips the next instruction.
Input/output	**CLD**	0 0001 0011	0 13	1	1	$(D)\leftarrow 0$	—	X	Clears port D.
	CLS	0 0001 0000	0 10	1	1	$(S)\leftarrow 0$	—	X	Clears port S.
	CLDS	0 0001 0001	0 11	1	1	$(D)\leftarrow 0$ $(S)\leftarrow 0$	—	X	Clears ports S and D.
	SD	0 0001 0101	0 15	1	1	$(D(Y))\leftarrow 1$ where $Y=0\sim 11$	—	X	Sets the bit of port D that is designated by register Y.
	RD	0 0001 0100	0 14	1	1	$(D(Y))\leftarrow 0$ where $Y=0\sim 11$	—	X	Resets the bit of port D that is designated by register Y.
	SZD	0 0010 1011	0 2B	1	1		$(D(Y))=0$ $Y=0\sim 11$	X	Skips the next instruction if the contents of the bit of port D that is designated by register Y and 0.
	OSAB	0 0001 1011	0 1B	1	1	$(S_7\sim S_4)\leftarrow(B)$ $(S_3\sim S_0)\leftarrow(A)$	where —	X	Output contents of registers A and B to port S.
	OSPA	0 0001 0111	0 17	1	1	$(S_7\sim S_4)\leftarrow$ through PLA$\leftarrow(A)$	—	X	Decords conents of register A by PLA and the result is output to port S.
	OSE	0 0000 1011	0 0B	1	1	$(S)\leftarrow(E)$	—	X	Outputs contents of register E to port S.
	IAS i	0 0101 010i	0 54 + i	1	1	$i=0: (A)\leftarrow(S_7\sim S_4)$ $i=1: (A)\leftarrow(S_3\sim S_0)$	—	X	Transfers from port S to register A. The high-order four bits of port S are transferred when the value of i in the instruction is 0 or the low-order four bits are transferred when the value of i is 1.
	OFA	0 1000 0001	0 81	1	1	$(F)\leftarrow(A)$	—	X	
	IAF	0 1000 1100	0 8C	1	1	$(A)\leftarrow(F)$	—	X	Transfers the port F input to register A.
	OGA	0 1000 0100	0 84	1	1	$(G)\leftarrow(A)$	—	X	Outputs contents of register A to port G.
	IAK	0 0101 0111	0 57	1	1	$(A)\leftarrow(K)$	—	X	Transfer the port K input to register A.
	SZK j	0 0101 10jj	0 58 + j	1	1		$(K(j))=0$	X	Skips the next instruction if the jth bit of port K input is 0.
	SU	0 0000 0111	0 07	1	1	$(U)\leftarrow 1$	—	X	Sets port U to 1.
	RU	0 0000 0110	0 06	1	1	$(U)\leftarrow 0$	—	X	Resets port U to 0.
Interrupts	**EI**	0 0000 0101	0 05	1	1	$(INTE)\leftarrow 1$		X	Sets interrupt flag INTE to enable interrupts.
	DI	0 0000 0100	0 04	1	1	$(INTE)\leftarrow 0$		X	Resets interrupt flag INTE to disabel interrupts.
Misc	**NOP**	0 0000 0000	0 00	1	1	$(PC_L)\leftarrow(PC_L)+1$		X	No operation.

Symbol	Contents	Symbol	Contents	Symbol	Contents
A	4-bit register (accumulator)	CY	1-bit carry flag	K	4-bit port
B	4-bit register	1F	1-bit timer 1 overflow flag	S	8-bit port
E	8-bit register	2F	1-bit timer 2 overflow flag	INTE	Interrupt enable flag
R	8-bit timer overflow register	xx	2-bit binary variable	INT	Interrupt request signal
V	4-bit register	yyyy	4-bit binary variable	EXF	1-bit external interrupt flag
X	2-bit register	z	1-bit binary variable	←	Shows the direction of data flow.
Y	4-bit register	nnnn	4-bit binary constant	( )	Indicates the contents of register, memory, etc.
Z	1-bit register	i	1-bit binary constant	⊻	Exclusive OR
DP	7-bit data pointer, combination of registers, X, Y and Z	ii	2-bit binary constant	—	Negation.
PC_H	The high-order four bits of the program counter.	XXXX	4-bit unknown binary number	X	Indicates flag is unaffected by instruction execution
PC_L	The low-order seven bits of the program counter.	1	Timer 1	xy	Label used to indicate the address xxx yyyy
PC	11-bit program counter combination of PC_H and PC_L	2	Timer 2	CPS	Indicate which data pointer and carry flag are active
SK0	11-bit stack register	D	12-bit port	pxy	Label used to indicate the address xxx yyyyon page ppp.
SK1	11-bit stack register	F	4-bit port	C	Hexadecimal number C + binary number X
SK2	11-bit stack register	G	4-bit port	+	
		U	1-bit port	x	

INSTRUCTION CODE LIST

D_8~D_4 / D_3~D_0 Hexadecimal notation		0 0000	0 0001	0 0010	0 0011	0 0100	0 0101	0 0110	0 0111	0 1000	0 1001	0 1010	0 1011	0 1100	0 1101	0 1110	0 1111	1 0000 ~ 1 0111	1 1000 ~ 1 1111
		0 0	0 1	0 2	0 3	0 4	0 5	0 6	0 7	0 8	0 9	0 A	0 B	0 C	0 D	0 E	0 F	10 ~ 17	18 ~ 1F
0000	0	NOP	CLS	SZB 0	SEY 0	LCPS 0	—	XAM 0	BL BML	—	—	A 0	LA 0	LXY 0,0	LXY 1,0	LXY 2,0	LXY 3,0	BM	B
0001	1	BA BMA BLA BMLA	CLDS	SZB 1	SEY 1	LCPS 1	—	XAM 1	BL BML	OFA	—	A 1	LA 1	LXY 0,1	LXY 1,1	LXY 2,1	LXY 1,1	BM	B
0010	2	INY	—	SZB 2	SEY 2	—	—	XAM 2	BL BML	SNZ1	—	A 2	LA 2	LXY 0,2	LXY 1,2	LXY 2,2	LXY 3,2	BM	B
0011	3	DEY	CLD	SZB 3	SEY 3	AMC	AMCS	XAM 3	BL BML	SNZ2	—	A 3	LA 3	LXY 0,3	LXY 1,3	LXY 2,3	LXY 3,3	BM	B
0100	4	DI	RD	—	SEY 4	RT	IAS 0	TAM 0	BL BML	OGA	—	A 4	XA 4	LXY 0,4	LXY 1,4	LXY 2,4	LXY 3,4	BM	B
0101	5	EI	SD	—	SEY 5	RTS	IAS 1	TAM 1	BL BML	T2AB	—	A 5	LA 5	LXY 0,5	LXY 1,5	LXY 2,5	LXY 3,5	BM	B
0110	6	RU	TEPA	SEAM	SEY 6	RTI	—	TAM 2	BL BML	TVA	—	A 6	LA 6	LXY 0,6	LXY 1,6	LXY 2,6	LXY 3,6	BM	B
0111	7	SU	OSPA	—	SEY 7	—	IAK	TAM 3	BL BML	—	—	A 7	LA 7	LXY 0,7	LXY 1,7	LXY 2,7	LXY 3,7	BM	B
1000	8	—	—	—	SEY 8	RC	SZK 0	XAMD 0	BL BML	—	—	A 8	LA 8	LXY 0,8	LXY 1,8	LXY 2,8	LXY 3,8	BM	B
1001	9	—	—	—	SEY 9	SC	SZK 1	XAMD 1	BL BML	—	—	A 9	LA 9	LXY 0,9	LXY 1,9	LXY 2,9	LXY 3,9	BM	B
1010	A	AM	TEAB	—	SEY 10	LZ 0	SZK 2	XAMD 2	BL BML	TAB2	—	A 10	LA 10	LXY 0,10	LXY 1,10	LXY 2,10	LXY 3,10	BM	B
1011	B	OSE	OSAB	SZD	SEY 11	LZ 1	SZK 3	XAMD 3	BL BML	—	—	A 11	LA 11	LXY 0,11	LXY 1,11	LXY 2,11	LXY 3,11	BM	B
1100	C	TYA	TBA	—	SEY 12	SB 0	RB 0	XAMI 0	BL BML	IAF	—	A 12	LA 13	LXY 0,12	LXY 1,12	LXY 2,12	LXY 3,12	BM	B
1101	D	—	TAY	—	SEY 13	SB 1	RB 1	XAMI 1	BL BML	—	—	A 13	LA 13	LXY 0,13	LXY 1,13	LXY 2,13	LXY 3,13	BM	B
1110	E	—	TAB	—	SEY 14	SB 2	RB 2	XAMI 2	BL BML	—	—	A 14	LA 14	LXY 0,14	LXY 1,14	LXY 2,14	LXY 3,14	BM	B
1111	F	CMA	—	SZC	SEY 15	SB 3	RB 3	XAMI 3	BL BML	—	—	A 15	LA 15	LXY 0,75	LXY 1,15	LXY 2,15	LXY 3,15	BM	B

Note 1. This list shows the machine codes and corresponding machine instructions. D_3~D_0 indicate the low order 4 bits of the machine code and D_8~D_4 indicate the high-order 5 bits. Hexadecimal numbers are also shown that represent the codes.
An instruction may consist of one, two ,or three words, but only the first word is listed Code combination indicated with a bar (—) must not be used.

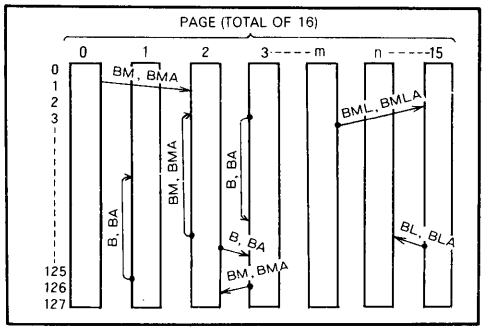
Note 2. Two-Word Instructions

	Second word
BL	1 1xxx yyy
BML	1 0xxx yyyy
BA	1 1xxx XXXX
BMA	1 0xxx XXXX

Three-Word Instructions

	Second word	Third word
BLA	0 0111 pppp	1 1xxx XXXX
BMLA	0 0111 pppp	1 0xxx XXXX

Note 3. Relationships for branching by means of branching instructions and subroutine calling instructions.



MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{DD}	Supply voltage	With respect to V_{SS}	0.3～−20	V
V_I	Input voltage (ports D and S, and input V_P)		0.3～−33	V
V_I	Input voltage, inputs other than ports D and S, and input V_P		0.3～−20	V
V_O	Output voltage, ports D and S		0.3～−33	V
V_O	Output voltage, other outputs than ports D and S		0.3～−20	V
Pd	Power dissipation	Ta=25°C	1100	mW
Topr	Operating temperature		−10～70	°C
Tstg	Storage temperature		−40～125	°C

4

RECOMMENDED OPERATING CONDITIONS (T_a=−10～70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{DD}	Supply voltage	−11	−12	−13	V
V_{SS}	Supply voltage		0		V
V_P	Pull-down transistor supply voltage	0		−33	V
V_{IH}	High-level input voltage, ports S and F	−1.5		0	V
V_{IH}	High-level input voltage, port D	−1.0		0	V
$V_{IH(\phi)}$	High-level clock input voltage	−1.5		0	V
V_{IL}	Low-level input voltage, inputs other than ports D and S	V_{DD}		−4.2	V
V_{IL}	Low-level input voltage, ports D and S	−33		−4.2	V
$V_{IL(\phi)}$	Low-level clock input voltage	V_{DD}		V_{DD}+2	V
V_{OL}	Low-level output voltage, ports D and S	−33		0	V
$f(\phi)$	Internal clock oscillation frequency	300		600	kHz

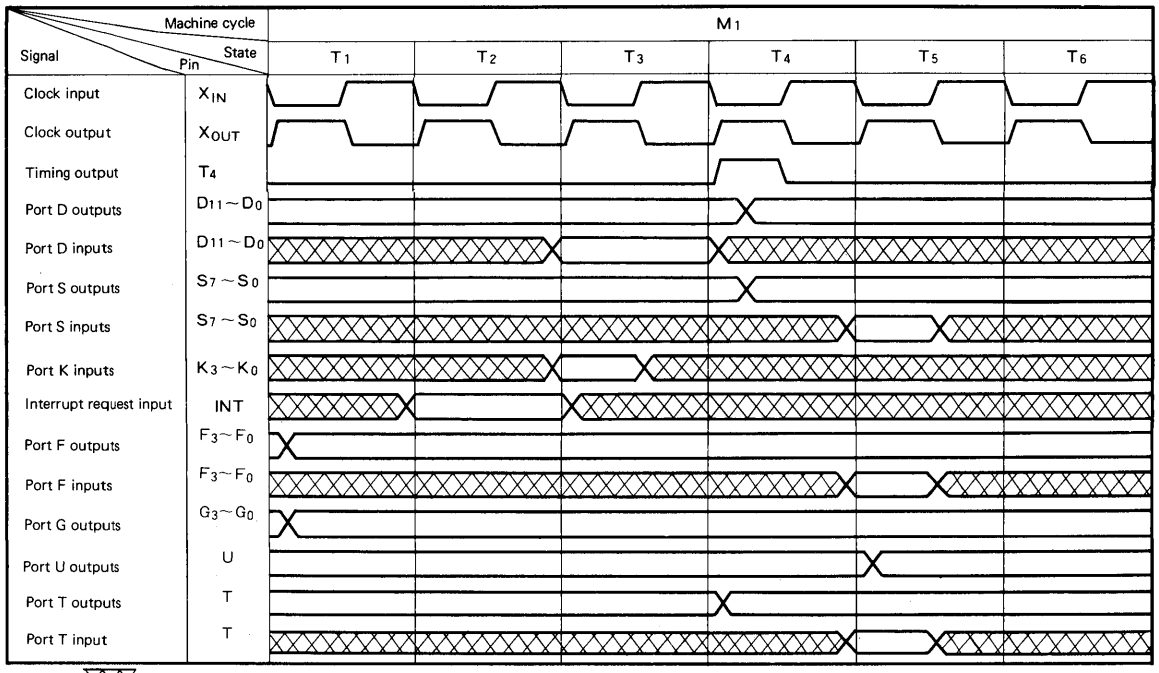
Note 1. $V_{IL(\phi)}$ is specified for the maximum V_{DD} value

ELECTRICAL CHARACTERISTICS (T_a=−10～70°C, V_{DD}=−12V 10%, V_{SS}=0V, f(φ)=300～600kHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IL}	Low-level output voltage, port F		V_{DD}		−4.2	V
V_{OH}	High-level output voltage, port D	V_{DD}=−12V, I_{OH}=−15mA, Ta=25°C	−2.5			V
V_{OH}	High-level output voltage, ports S and F	V_{DD}=−12V, I_{OH}=−8mA (port S) I_{OH}=−5mA (port F), Ta=25°C	−2.5			V
V_{T-}	Negative threshold voltage (Schmitt input mask option)	V_{DD}=−12V, Ta=25°C	−7		−4	V
$V_{T+}-V_{T-}$	Hysteresis (Schmitt input mask option).	V_{DD}=−12V, Ta=25°C	2		3.5	V
$I_{I(\phi)}$	Clock input current	$V_{I(\phi)}$=−12V, Ta=25°C		−20	−40	μA
I_{IH}	High-level input current, port K (with pull-down resistors)	V_{DD}=−12V, V_{IH}=0V, Ta=25°C	50		250	μA
I_{IH}	High-level input current, ports D and S (with pull-down resistors)	V_P=−33V, V_{IH}=0V, Ta=25°C	80		280	μA
I_{OH}	High-level output current, port D (Note 2)	V_{DD}=−12V, V_{OH}=−2.5V, Ta=25°C			−15	mA
I_{OH}	High-level output current, ports S and F	V_{DD}=−12V, V_{OH}=−2.5V, Ta=25°C		−5 (port F) −8 (port S)		mA
I_{OL}	Low-level output current, ports D and S	V_{OL}=−33V, Ta=25°C			−33	μA
I_{OL}	Low-level output current, port outputs	V_{DD}=−12V, Ta=25°C			−33	μA
I_{DD}	Supply current	V_{DD}=−12V, Ta=25°C		21		mA
$C_{i(\phi)}$	Clock input capacitance	V_{DD}=X_{OUT}=V_{SS}, f=1MHz, 25mVrms			10	pF

Note 2. Currents are taken as positive when flowing into the IC (zero signal condition), with the minimum and maximum values as absolute values.
3. It is possible to connect up to 5 lines of the port D at maximum ratings (−15mA) or all lines of port S and F at maximum ratings of (−8mA) and (−5mA) respectively.

BASIC TIMING



Note 1. XXX The crosshatch area indicates invalid input

MITSUBISHI ELECTRIC

M58847-XXXSP

SINGLE-CHIP 4-BIT MICROCOMPUTER

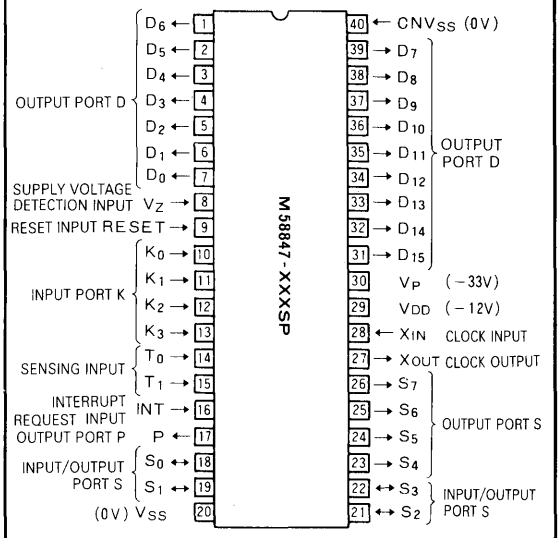
DESCRIPTION

The M58847-XXXSP is a single-chip 4-bit microcomputer fabricated using p-channel aluminum gate ED-MOS technology. It is housed in a 40-pin shrink plastic molded DIL package and provides 25 output lines, 4 input lines, 2 sensing lines and 1 interrupt input. Because of its low power consumption, it is ideal for consumer electronics applications requiring many control signals.

FEATURES

- Basic machine instructions 52
- Instruction execution time (for 1 word instructions using a 400kHz clock frequency) 15μs
- Memory capacity: ROM ..... 2048 words x 9 bits
  RAM ..... 128 words x 4 bits
- Single −12V power supply
- Subroutine nesting ..... 2 levels
- Interrupt function ..... 1 factor, 1 level
- Input (port K) ..... 4 ports
- Output (ports D and P) ..... 17 ports
- Input/output (port S) ..... 8 ports
- Sensing input (port T) ..... 2 ports
- High withstanding voltage and large current output
- Built-in pull-down transistors (ports T, K, D, P, and S, mask option)
- Built-in clock generator circuit

PIN CONFIGURATION (TOP VIEW)

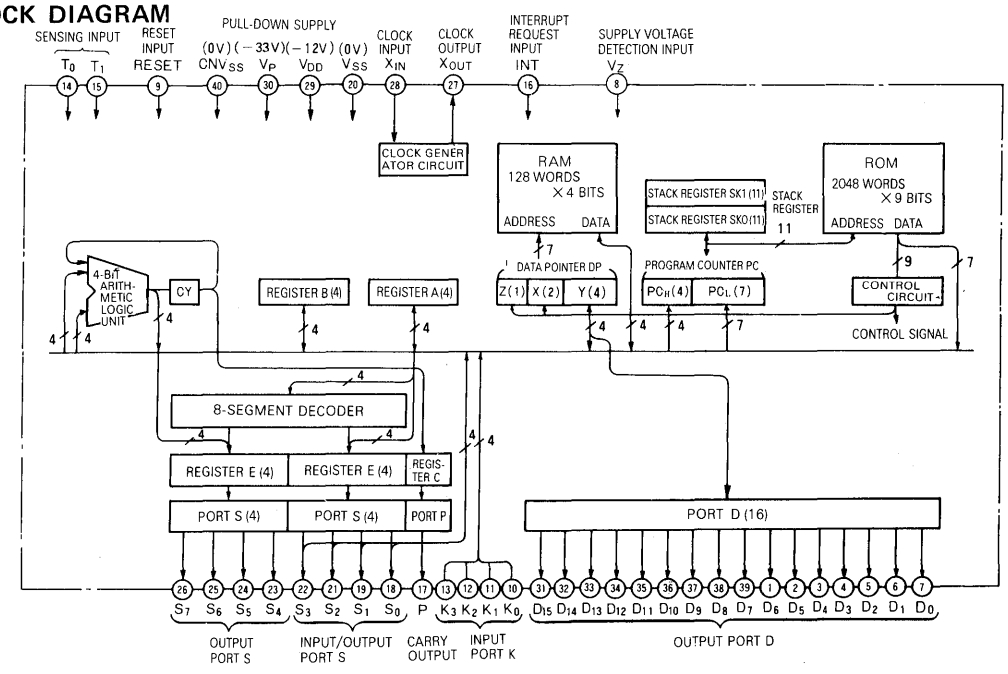


Outline 40P4B

APPLICATIONS

- VTRs, TVs, cassette decks
- Microwave ovens, air conditioners, heaters, washing machines, home sewing machines
- Office equipment, copying machines, medical equipment
- Educational equipment, electronic games

BLOCK DIAGRAM



PERFORMANCE SPECIFICATIONS

Parameter			Performance
Basic machine instructions			52
Instruction execution time			15 μs (1-word instructions using a clock frequency of 400 kHz)
Clock frequency			240kHz ~ 400kHz
Memory capacity	ROM		2048 words x 9 bits
	RAM		128 words x 4 bits
Input/output ports	K	Input	4 bits x 1
	S	Output	8 bits x 1
		Input	4 bits x 1
	P	Output	1 bit x 1
	D	Output	1 bit x 16
	T	Sensing input	1 bit x 2
Subroutine nesting			2 levels (including one level of interrupt)
Clock generator			Built-in (externally connected RC circuit or ceramic resonator)
I/O chracteristics of ports	I/O withstanding voltage		−33V
	Ports P and S output current		− 8 mA
	Port D output current		−15mA
Supply voltage	V_{DD}		−12V
	V_{SS}		0 V
Device structure			p-channel aluminum gate ED-MOS
Package			40-pin shrink plastic molded DIL package
Power dissipation			10mW (typ)

PIN DESCRIPTIONS

Pin	Name	Input or output	Function
V_{DD}	Supply voltage		V_{DD} and V_{SS} are the power supply pins. V_{DD} should be connected to −12V±10% and V_{SS} should be grounded. V_P is the pull-down supply voltage input for the pull-down transistors (mask options) for ports P, S, and D.
V_{SS}	Supply voltage		
V_P	Pull-down voltage input		
V_Z	Supply voltage detection input	In	This input pin is provided for use in detecting a drop in the supply voltage.
RESET	Reset input	In	This pin is used to intialize the microcomputer. If it is held high for at least two machine cycles after V_{DD} reaches to within 10% of −12V, the reset condition is enabled.
CNV_{SS}	CNV_{SS} input	In	This pin is not reserved for customer use but should be connected to V_{SS}.
X_{IN}	Clock input	In	These are the input and output pins for the built-in clock generator. A ceramic resonator element (240~400 kHz) or RC circuit may be connected to these pins to provide the required oscillation stability.
X_{OUT}	Clock output	Out	
T_1, T_0	Sensing input	In	Sensing input pin
$K_3 \sim K_0$	Input port K	In	4-bit input port
$S_3 \sim S_0$	I/O port S	In/out	$S_7 \sim S_4$ and P comprise an output port $S_3 \sim S_0$ comprise an input/output port
$S_7 \sim S_4$	Output port S	Out	
P	Output port P	Out	
$D_{15} \sim D_0$	Output port D	Out	The individual bits of this 16-bit output port may be set and reset separately.
INT	Interrupt request input	In	This interrupt signal input pin triggers on the input signal edge.

BASIC FUNCTION BLOCKS

Program Memory (ROM)

This 2048 word x 9-bit ROM can be programmed with machine instruction codes in accordance with the customer's specifications. It consists of 16 pages, each containing an address range of 0~127.

The page is specified by the upper order 4 bits (PC_H) of the program counter.

The address within a particular page is specified by the lower order 7 bits which form a polynomial counter (PC_L). When the last address is reached (127), the address wraps around to the 0th address.

The BL instruction is used to branch to a different page than the current page. While the program counter is in reality a polynomial counter, a cross-assembly technique is used to allow the programmer to think of this counter as a normal pure binary counter, for ease in programming.

Page 0 and page 1 are special pages used for subroutine calls. The single-word instruction BM can be used to call a subroutine on page 0 from any arbitrary page. When the BM instruction is executed, the SM flag is set and until any of the BL, BML, RT or RTS instructions are executed, the B and BM instructions are used for functions differing from their normal functions.

Until any of the above listed instructions is executed after an BM instruction execution, the B instruction has the effect of branching to the 1st page and the BM instruction has the effect of branching to the 0th page. The flag SM is reset when the BL, BML, RT, or RTS instruction is executed.

Fig. 1 shows the ROM address map.

Program Counter (PC)

This counter is used to specify ROM addresses and the sequence of read-out of instructions stored in ROM. The upper 4 bits (PC_H) are used to specify the page in ROM and the lower 7 bits (PC_L) of which are a polynomial counter used to specify the address on the specified page.

Stack Registers (SK_0, SK_1)

These registers are used to temporarily store the contents of the PC while executing subroutines or interrupt programs until the program returns to the main routine.

The stack registers are organized in 2 words of 11 bits, allowing 2 levels of subroutine nesting.

Data Memory (RAM)

This 512-bit (128 words x 4 bits) RAM is used to store both processing and control data. One RAM word consists of 4 bits with bit manipulation possible over the entire storage area. The 128 words are arranged in 2 file groups x 4 files x 16 digits x 4 bits.

The word addresses for the data RAM are specified by means of the data pointer which consists of 1 bit of the register Z, 2 bits of the register X and 4 bits of the register Y. Fig. 2 shows the RAM address map. There are 8 files (F_0~F_7) consisting of 16 words of 4 bits, which are convenient as a 16-digit register.

The specification for these file grimps is made by registers Z and X.

Data Pointer (DP)

This register is used to designate RAM addresses as well as bit position for the output port D. The data pointer is a 7-bit register, the uppermost bit of which is register Z which is used to specify the RAM file group, the central 2 bits of which form register X which is used to specify the RAM file, and the lower 4 bits of which form register Y which is used to specify the digit within the file. In addition, when the register Z's bit is 1, register Y is used to specify the bit position for the output port D.

4-bit Arithmetic Logic Unit (ALU)

This unit executes 4-bit arithmetic and logical operations by means of a 4-bit adder and related logic circuitry.

Register A and Carry Flag (CY)

Register A is a 4-bit accumulator that constitutes the basis for arithmetic operations. Data processing operations such as arithmetic and logical operations, data transfer, exchange, conversion, and data input/output are executed by means of this register. The carry flag CY is used to store carry or overflow after execution of arithmetic and logical operations by the arithmetic unit. The carry flag may also be used as a 1-bit flag.

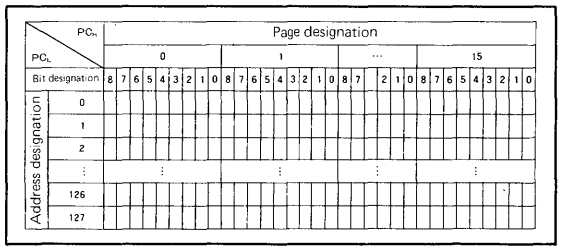


Fig. 1 ROM address map

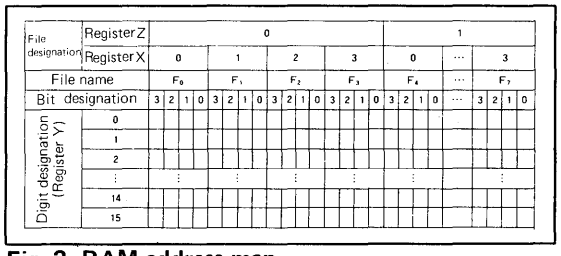


Fig. 2 RAM address map

Registers B, E, and C

Register B is composed of 4 bits and can be used as a 4-bit temporary storage register or for 8-bit data transfer in conjunction with register A. Register E is an 8-bit register which can be used for temporary data storage or as an auxiliary register for input/output port S, and it also has left shift capability. Register C is a 1-bit register, to which the contents of the carry flag can be transferred. It can also be used to perform left shift when linked to register E.

Interrupt Functions

An interrupt input has been provided to allow the M58847-XXXSP to accept external interrupts. When the input signal changes from low to high, an edge-sensing flag is set, causing the interruption of the normally executed program if the interrupt enable flag is set. When an interrupt is received, the following things occur.

(1) The program counter and SM flag are saved on each stack.
(2) The program counter is set to the 0th address on page 2.
(3) The SM flag and edge-sensing flag are reset.
(4) The interrupt enable flag is reset.

In the above state the program begins at page 2, address 0, the first address of the interrupt program. The instruction RTI is used to end the interrupt program and return the processor to the main program flow.

Since the SM flag has a single-level stack, one level of interrupt is possible. The program counter, however, has a two level stack, enabling subroutine nesting of one level after an interrupt uses one of these levels.

The microcomputer can accept an interrupt request in the following conditions.

When not executing a B, BL, BM, BML, LA, LXY, RT, RTS, RTI, DI, or EI instruction or not executing a skip operation and the interrupt enable flag is set.

Input/Output Ports

Ports T, K, S, D, and P may be provided with pull-down transistors as a mask option. Fig. 3 shows the circuits for the input/output ports.

In addition, the contents of the register A are decoded to 8 bits by built-in 8 segment decoder and transferred to register E or port S. The decoder function is fixed and not available in special forms as a mask option. Table 1 shows the decoder function.

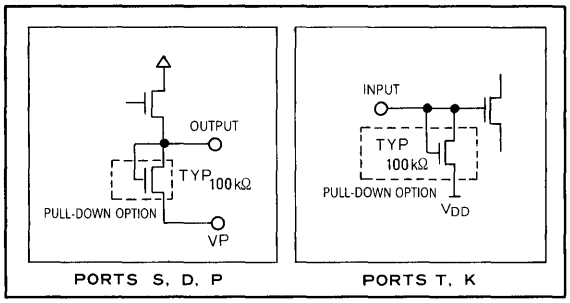


Fig. 3 Input/output circuits

Table 1 Decoder function table

Hexadecimal value	Register A				Port S output								Display
	A_3	A_2	A_1	A_0	S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0	
0	0	0	0	0	L	L	H	H	H	H	H	H	0
1	0	0	0	1	L	L	L	L	L	H	H	L	1
2	0	0	1	0	L	H	L	H	H	L	H	H	2
3	0	0	1	1	L	H	L	L	H	H	H	H	3
4	0	1	0	0	L	H	H	L	L	H	H	L	4
5	0	1	0	1	L	H	H	L	H	H	L	H	5
6	0	1	1	0	L	H	H	H	H	H	L	H	6
7	0	1	1	1	L	L	H	L	L	H	H	H	7
8	1	0	0	0	L	H	H	H	H	H	H	H	8
9	1	0	0	1	L	H	H	L	H	H	H	H	9
A	1	0	1	0	L	H	L	H	H	H	L	L	O
B	1	0	1	1	H	L	L	L	L	L	L	L	-
C	1	1	0	0	L	H	H	H	H	L	L	H	E
D	1	1	0	1	L	L	H	H	H	L	L	H	C
E	1	1	1	0	L	H	L	L	L	L	L	L	—
F	1	1	1	1	L	L	L	L	L	L	L	L	Blank

Reset

The RESET input has been provided to enable initialization of the microcomputer. If the input is kept high for at least two machine cycles after the supply voltage V_{DD} reaches to within 10% of −12V, the microcomputer will be reset, enabling the following states.

(1) The program counter is set to 0 (PC) ← 0
(2) Ports S, P and D are turned off (S) ← 0 (P) ← 0 (D) ← 0
(3) Flag SM is reset (SM) ← 0
(4) The edge-sensing flag is reset
(5) The interrupt enable flag is reset (INTE) ← 0

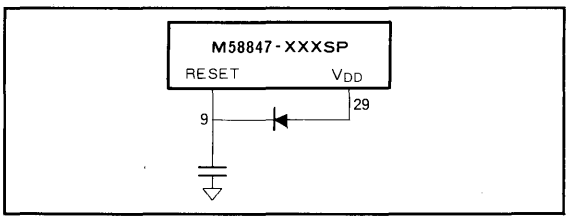


Fig. 4 Power-on reset circuit

In addition, when the supply voltage V_{DD} is in the range −7V ~ −13.2V and the V_Z input is driven high, an internal transistor is turned on and the RESET pin is set to the level of V_{SS}. Even if the V_Z pin returns to low, the internal transistor will remain turned on until the RESET pin is driven high. By using this function it is possible to sense temporary drops in the supply voltage to allow reset at these times to return to normal operation.

Clock Generator Circuits

A clock generator circuit has been built in to allow control of the frequency by means of an externally connected RC circuit or ceramic resonator. The choice of frequency determining element is made at the time of purchase as a mask option. Circuit examples are shown in Fig. 5~7.

Mask Options

- Port T pull-down transistors
- Port K pull-down transistors
- Port D pull-down transistors
- Port S pull-down transistors
- Port P pull-down transistors
- Oscillation conditions

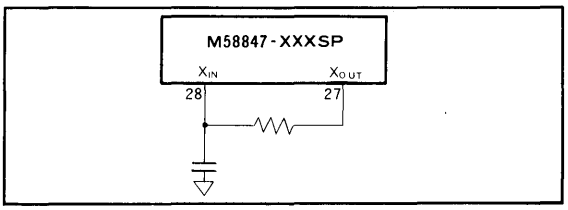


Fig. 5 External RC circuit

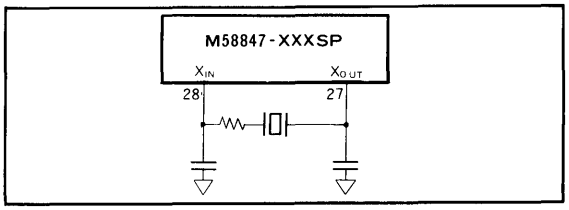


Fig. 6 External ceramic resonator

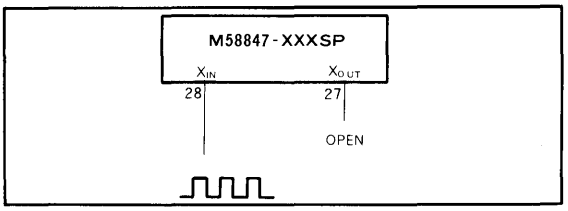


Fig. 7 External clock circuit

Documentation Required upon Ordering

The following information should be provided when ordering a custom mask.

(1)	M58847-XXXSP mask confirmation sheet	
(2)	ROM data	3 EPROM sets
(3)	Port D pull-down transistors	On confirmation sheets
(4)	Port S pull-down transistors	On confirmation sheets
(5)	Port P pull-down transistors	On confirmation sheets
(6)	Port T pull-down transistors	On confirmation sheets
(7)	Port K pull-down transistors	On confirmation sheets
(8)	Oscillation conditions	On confirmation sheets

MACHINE INSTRUCTIONS

Type of instruction	Mnemonic	Instruction code D_8 $D_7D_6D_5D_4$ $D_3D_2D_1D_0$	16mal notation	No. of words	No. of cycles	Functions	Skip conditions	Flag CY	Description of operation
Register-to-register transfers	TAB	0 1011 1001	0B9	1	1	(A)←(B)	—	×	Transfers contents of register B to register A.
	TBA	0 1011 0101	0B5	1	1	(B)←(A)	—	×	Transfers contents of register A to register B.
	TAY	0 1011 1010	0BA	1	1	(A)←(Y)	—	×	Transfers contents of register Y to register A.
	TYA	0 1011 0110	0B6	1	1	(Y)←(A)	—	×	Transfers contents of register A to register Y.
	TEAB	0 1011 0001	0B1	1	1	(E_7~E_4)←(B), (E_3~E_0)←(A), (C)←(CY) (C)←(CY)	—	×	Transfers contents of registers A and B to register E.and the contents of the carry flag to register C.
	TEPA	0 1011 0000	0B0	1	1	(E_7~E_0)← 8-segment decoder ←(A), (C)←(CY)	—	×	Decodes contents of register A in the 8-segment decoder and transfers result to register E. The contents of the carry flag are transferred to register.
	TXA	0 1111 0101	0F5	1	1	(X)←(A_1A_0) (Z)←($\overline{A_2}$) (CY)←($\overline{A_3}$)	—	0/1	Transfers the first and second bits of the register A to register X, complement of the third bit to register Z, and complement of the fourth bit to the carry flag CY.
	TAX	0 1111 1001	0F9	1	1	(A_1A_0)←(X) (A_2)←($\overline{Z}$) (A_3)←($\overline{CY}$)	—	×	Transfers the contents of register X to the first and second bits of register A, complement of the contents of register Z to the third bit of register A, and complement of the contents of the carry flag CY to the fourth bit of register A.
RAM addresses	LXY x,y	0 01yy yyxx	048 (+2 y_3 + y_2) (y_1 +4 y_0 + x)	1	1	(X)←x, where, x= 0 ~ 3 (Y)←y, where, y= 0 ~ 15	Written successively	×	Loads value of "x" into register X, and of "y" into Y. When LXY is written successively, the first is executed and successive ones are skipped.
	LZ z	0 0000 110z	00C + z	1	1	(Z)←z, where z= 0, 1	—	×	Loads value of "z" into register Z.
	INY	0 1110 0100	0E4	1	1	(Y)←(Y)+ 1	(Y)= 0	×	Increments contents of register Y by 1. Skips next instruction when new contents of register Y are "0".
	DEY	0 1110 1000	0E8	1	1	(Y)←(Y)− 1	(Y)= 15	×	Decrements contents of register Y by 1. Skips next instruction when new contents of register Y are "15".
	SADR j	0 1100 00jj	0Cj	1	1	j= 0 : specifies the 0th digit of F4 j= 1 : specifies the 0th digit of F5 j= 2 : specifies the 0th digit of F6 j= 3 : specifies the 0th digit of F7	—	×	During the following instruction cycle only, the 0th digit of the file soecified by the immediate field (in the range F4 to F7). The contents of the data pointer remain unchanged.
RAM-accumulator transfers	TAM j	0 1010 00jj	0Aj	1	1	(A)←(M(DP)), (X)←(X)∀j, where, j= 0 ~ 3	—	×	Transfers the RAM contents addressed by the active DP to register A. Register X is then "exclusive OR-ed" with the value j in the instruction, and the result stored in register X.
	XAM j	0 1010 11jj	0AC + j	1	1	(A)↔(M(DP)), (X)←(X)∀j, where, j= 0 ~ 3	—	×	Exchanges the contents of the RAM and register A. Contents of X are then "exclusive OR-ed" with the value j and the result stored in register X.
	XAMD j	0 1010 10jj	0A8 + j	1	1	(A)↔(M(DP)), (X)←(X)∀j, (Y)←(Y)− 1 where, j= 0 ~ 3	(Y)= 15	×	Exchanges the contents of the RAM and register A. Contents of X are then "exclusive OR-ed" with the value j in the instruction, and the result stored in register X. The contents of register Y are decremented by 1, and when the result is 15, the next instruction is skipped.
	XAMI j	0 1010 01jj	0A4 + j	1	1	(A)↔(M(DP)), (X)←(X)∀j, (Y)←(Y)+ 1 where, j= 0 ~ 3	(Y)= 0	×	Exchanges the contents of the RAM and register A. Contents of X are then "exclusive OR-ed" with the value j in the instruction and the result stored in register x. The contents of register Y are incremented by 1, and when the result meets with the marked skip condition. the next instruction is skipped
Arithmetic operation	LA n	0 1000 nnnn	08n	1	1	(A)←n, where, n= 0 ~ 15	Written successively	×	Loads the value n into register A. When LA is written consecutively the first is executed, and successive ones are skipped.
	AM	0 1011 1110	0BE	1	1	(A)←(A)+(M(DP))	—	×	Adds the contents of the RAM to register A. The result is retained in register A, and the contents of flag CY are unaffected.
	AMC	0 1011 1100	0BC	1	1	(A)←(A)+(M(DP))+(CY), (CY)← Carry	—	0/1	Adds the RAM contents addressed by the active DP and contents of flag CY to register A. The result is stored in register A, and the carry in the active flag CY.
	AMCS	0 1011 1101	0BD	1	1	(A)←(A)+(M(DP))+(CY), (CY)← Carry	Carry= 1	0/1	Adds the contents of the RAM and flag CY to register A. The result is stored in register A and the carry in the CY, but the next instruction is skipped when a carry is produced.
	A n	0 1001 nnnn	09n	1	1	(A)←(A)+n, where, n= 0 ~ 15	A carry is not produced and = 0 n≠ 6	×	Adds value n in the instruction to register A. The contents of flag CY are unaffected and the next instruction is skipped if a carry is not produced, except when n=6.
	SC	0 0000 0110	006	1	1	(CY)← 1	—	1	Sets active flag CY.
	RC	0 0000 0101	005	1	1	(CY)← 0	—	0	Resets active flag CY.
	SZC	0 0000 0010	002	1	1	(CY)= 0 ?	(CY)= 0	×	Skips next instruction when contents of the active flag CY are 0 .
	CMA	0 1011 0111	0B7	1	1	(A)←($\overline{A}$)	—	×	Stores complement of register A in register A.
Bit operation	SB j	0 0001 00jj	01j	1	1	(M_j(DP))← 1, where, j= 0 ~ 3	—	×	Sets the jth bit of the RAM addressed by the active DP (the bit designated by the value j in the instruction).
	RB j	0 0001 01jj	014 + j	1	1	(M_j(DP))← 0, where, j= 0 ~ 3	—	×	Resets the jth bit of the RAM addressed by the active DP (the bit designated by the value j in the instruction).
	SZB j	0 0001 10jj	018 + j	1	1	(M_j(DP))= 0 ?, where, j= 0 ~ 3	(M_j(DP))=0	×	Skips next instruction when the contents of the jth bit of the RAM addressed by the active DP (the bit which is designated by the value j in the instruction) are 0.
Compares	SEAM	0 1011 1111	0BF	1	1	(M(DP))=(A) ?	(M(DP))=(A)	×	Skips next instruction when contents of register A are equal to the RAM contents addressed by the active DP.
	SEY y	0 0010 yyyy	02y	1	1	(Y)=y ?, where, y= 0 ~ 15	(Y)=y		Skips next instruction when the contents of register Y are equal to the value y in the instruction.
Jumps	B xy	1 1xxx yyyy	18y + x	1	2	(PCL)←16x+y, where, (SM)= 0	—	×	Jumps to address xy of the current page.
						(PCH)← 1 (PCL)←16x+y, where, (SM)= 1			Jumps to address xy on page 1 when executed, provided that none of instructions RT, RTS, BL or BML, was executed after execution of instruction BM.
	BL pxy	0 0011 pppp 1 1xxx yyyy	03p 18y + x	2	3	(PCH)←p, (SM)← 0 (PCL)←16x+y	—	×	Jumps to address xy of page p.

MITSUBISHI ELECTRIC

Type of instruction	Mnemonic	Instruction code $D_8\ D_7D_6D_5D_4\ D_3D_2D_1D_0$	16mal notation	No. of words	No. of cycles	Functions	Skip conditions	Flag CY	Description of operation
Subroutine calls	**BM xy**	**1 0 x x x y y y y**	**1 x y**	1	2	$(SK_1)\leftarrow(SK_0)\leftarrow(PC)$, where, $(SM)=0$ $(PC_H)\leftarrow0$, $(PC_L)\leftarrow16x+y$, $(SM)\leftarrow1$			Calls for the subroutine starting at address xy on page 0.
						$(PC_H)\leftarrow0$ $(PC_L)\leftarrow16x+y$, where, $(SM)=1$	—	×	Jumps to address xy of page 0 provided that none of instructions RT, RTS, BL or BML, was executed after the execution of instruction, BM.
	BML pxy	**0 0 0 1 1 p p p p** **1 0 x x x y y y y**	**0 3 p** **1 x y**	2	3	$(SK_1)\leftarrow(SK_0)\leftarrow(PC)$ $(PC_H)\leftarrow p$, $(PC_L)\leftarrow16x+y$, $(SM)\leftarrow0$	—	×	Calls for the subroutine starting at address xy of page p.
Program returns	**RT**	**0 0 0 0 1 1 1 1**	**0 1 F**	1	2	$(PC)\leftarrow(SK_0)\leftarrow(SK_1)$, $(SM)\leftarrow0$	—	×	Returns to the main routine from the subroutine.
	RTS	**0 0 0 0 1 1 1 0**	**0 1 E**	1	2	$(PC)\leftarrow(SK_0)\leftarrow(SK_1)$, $(SM)\leftarrow0$	Unconditional skip	×	Returns to the main routine from the subroutine, and unconditionally skips the next instruction.
Interrupts	**EI**	**0 0 0 0 0 1 0 1 1**	**0 0 B**	1	1	$(INTE)\leftarrow1$	—	×	Sets interrupt flag INTE to enable interrupts.
	DI	**0 0 0 0 0 1 0 1 0**	**0 0 A**	1	1	$(INTE)\leftarrow0$	—	×	Resets interrupt flag INTE to disable interrupts.
	RTI	**0 0 0 0 1 1 1 0 1**	**0 1 D**	1	2	$(PC)\leftarrow(SK_0)\leftarrow(SK_1)$, $(SM)\leftarrow(SM_0)$	—	×	Returns from interrupt routine to main routine. The internal subroutine mode flag is restored to the value held immediately before the interrupt.
Input/output	**SD**	**0 0 0 0 0 1 1 1 1**	**0 0 F**	1	1	$(D(Y))\leftarrow1$, where, $(Z)=1$	—	×	Sets the bit of port D, that is designated by register Y, when the contents of register Z are 1.
	RD	**0 0 0 0 0 1 1 1 0**	**0 0 E**	1	1	$(D(Y))\leftarrow0$, where, $(Z)=1$	—	×	Resets the bit of port D, that is designated by register Y, when the contents of register Z are 1.
	OSAB	**0 1 0 1 1 0 0 1 1**	**0 B 3**	1	1	$(S_1\sim S_4)\leftarrow(E_1\sim E_4)\leftarrow(B)$, $(P)\leftarrow(C)\leftarrow(CY)$, $(S_3\sim S_0)\leftarrow(E_3\sim E_0)\leftarrow(A)$	—	×	Output contents of registers A and B to port S., and the contents of the carry flag to port P.
	OSPA	**0 1 0 1 1 0 0 1 0**	**0 B 2**	1	1	$(S_7\sim S_0)\leftarrow(E_7\sim E_0)\leftarrow$8-segment decoder $\leftarrow(A)$, $(P)\leftarrow(C)\leftarrow(CY)$	—	×	Decodes contents of register A by 8 segment decoder and the result is output to port S. and output the contents of the carry flag to port P
	OSE	**0 1 1 1 1 0 0 1 0**	**0 F 2**	1	1	$(S_1\sim S_0)\leftarrow(E_7\sim E_0)$, $(P)\leftarrow(C)$	—	×	Outputs contents of registers E and C to ports S and P.
	SHFT	**0 0 0 0 0 1 0 0 0**	**0 0 8**	1	1	$(En)\leftarrow(En-1)$, $(E_0)\leftarrow(C)\leftarrow(CY)$	—	×	Links register E and register C and shifts left. The contents of register C are shifted into the least significant bit of register E and the contents of the flag CY are shifted into register C. The most significant bit of register E is lost.
	IAS	**0 1 1 1 1 0 0 0 0**	**0 F 8**	1	1	$(A)\leftarrow(S_3\sim S_0)$	—	×	Transfers the 4 lower order bits of port S to register A.
	IAK	**0 1 0 1 1 0 0 0 0**	**0 B 8**	1	1	$(A)\leftarrow(K_3\sim K_0)$	—	×	Transfers the 4 bits of port K to register A.
	SZTO	**0 0 0 0 0 0 0 0 1**	**0 0 1**	1	1	$T_0=0$?	$T_0=0$	×	Skips the next instruction if the sensing input T_0 is low.
	SZT1	**0 0 0 0 0 1 0 0 0**	**0 0 4**	1	1	$T_1=0$?	$T_1=0$	×	Skips the next instruction if the sensing input T_1 is low.
	CLDS	**0 0 0 0 0 0 1 1 1**	**0 0 7**	1	1	$(D)\leftarrow0$, $(S)\leftarrow0$, $(P)\leftarrow0$	—	×	Clears ports D, S and P
Misc	**NOP**	**0 0 0 0 0 0 0 0 0**	**0 0 0**	1	1	$(PC)\leftarrow(PC)+1$	—	×	No operation.

Symbol	Contents	Symbol	Contents	Symbol	Contents
A	4-bit register (accumulator)	SK_1	11-bit stack register	( )	Indicates contents of the register, memory, etc.
B	4-bit register	CY	1-bit carry flag	∀	Exclusive OR
C	1-bit register	xx	2-bit binary variable	—	Negation
E	8-bit register	yyyy	4-bit binary variable	×	Indicates flag is unaffected by instruction execution
X	2-bit register	z	1-bit binary variable	xy	Label used to indicate the address xxxyyyy
Y	4-bit register	nnnn	4-bit binary constant	pxy	Label used to indicate the address xxxyyyy of page pppp.
Z	1-bit register	ii	2-bit binary constant	C	Hexadecimal number C + binary number x.
DP	7-bit data pointer, combination of registers, X Y and Z	D	16-bit port	+	
PC_H	The high-order four bits of the program counter.	K	4-bit port	x	
PC_L	The low-order seven bits of the program counter.	S	8-bit port	SM	1-bit subroutine mode flag
PC	11-bit program counter, combination of PC_H and PC_L	P	1-bit port	SM_0	1-bit subroutine mode flag save register
SK_0	11-bit stack register	←	Shows direction of data flow	INTE	Interrupt enable flag

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LIST OF INSTRUCTION CODES

D_8 ~ D_4 / D_3 ~ D_0 Hexadecimal notation		0 0000	0 0001	0 0010	0 0011	0 0100	0 0101	0 0110	0 0111	0 1000	0 1001	0 1010	0 1011	0 1100	0 1101	0 1110	0 1111	1 0000 ~ 1 0111	1 1000 ~ 1 1111
		0 0	0 1	0 2	0 3	0 4	0 5	0 6	0 7	0 8	0 9	0 A	0 B	0 C	0 D	0 E	0 F	10~17	18~1F
0000	0	NOP	SB 0	SEY 0	BL BML	LXY 0, 0	LXY 0, 4	LXY 0, 8	LXY 0, 12	LA 0	A 0	TAM 0	TEPA	SADR 0	—	—	—	BM	B
0001	1	SZTO	SB 1	SEY 1	BL BML	LXY 1, 0	LXY 1, 4	LXY 1, 8	LXY 1, 12	LA 1	A 1	TAM 1	TEAB	SADR 1	—	—	—	BM	B
0010	2	SZC	SB 2	SEY 2	BL BML	LXY 2, 0	LXY 2, 4	LXY 2, 8	LXY 2, 12	LA 2	A 2	TAM 2	OSPA	SADR 2	—	—	OSE	BM	B
0011	3	—	SB 3	SEY 3	BL BML	LXY 3, 0	LXY 3, 4	LXY 3, 8	LXY 3, 12	LA 3	A 3	TAM 3	OSAB	SADR 3	—	—	—	BM	B
0100	4	SZT1	RB 0	SEY 4	BL BML	LXY 0, 1	LXY 0, 5	LXY 0, 9	LXY 0, 13	LA 4	A 4	XAMI 0	—	—	—	INY	—	BM	B
0101	5	RC	RB 1	SEY 5	BL BML	LXY 1, 1	LXY 1, 5	LXY 1, 9	LXY 1, 13	LA 5	A 5	XAMI 1	TBA	—	—	—	TXA	BM	B
0110	6	SC	RB 2	SEY 6	BL BML	LXY 2, 1	LXY 2, 5	LXY 2, 9	LXY 2, 13	LA 6	A 6	XAMI 2	TYA	—	—	—	—	BM	B
0111	7	CLDS	RB 3	SEY 7	BL BML	LXY 3, 1	LXY 3, 5	LXY 3, 9	LXY 3, 13	LA 7	A 7	XAMI 3	CMA	—	—	—	—	BM	B
1000	8	SHFT	SZB 0	SEY 8	BL BML	LXY 0, 2	LXY 0, 6	LXY 0, 10	LXY 0, 14	LA 8	A 8	XAMD 0	IAK	—	—	DEY	IAS	BM	B
1001	9	—	SZB 1	SEY 9	BL BML	LXY 1, 2	LXY 1, 6	LXY 1, 10	LXY 1, 14	LA 9	A 9	XAMD 1	TAB	—	—	—	TAX	BM	B
1010	A	DI	SZB 2	SEY 10	BL BML	LXY 2, 2	LXY 2, 6	LXY 2, 10	LXY 2, 14	LA 10	A 10	XAMD 2	TAY	—	—	—	—	BM	B
1011	B	EI	SZB 3	SEY 11	BL BML	LXY 3, 2	LXY 3, 6	LXY 3, 10	LXY 3, 14	LA 11	A 11	XAMD 3	—	—	—	—	—	BM	B
1100	C	LZ 0	—	SEY 12	BL BML	LXY 0, 3	LXY 0, 7	LXY 0, 11	LXY 0, 15	LA 12	A 12	XAM 0	AMC	—	—	—	—	BM	B
1101	D	LZ 1	RTI	SEY 13	BL BML	LXY 1, 3	LXY 1, 7	LXY 1, 11	LXY 1, 15	LA 13	A 13	XAM 1	AMCS	—	—	—	—	BM	B
1110	E	RD	RTS	SEY 14	BL BML	LXY 2, 3	LXY 2, 7	LXY 2, 11	LXY 2, 15	LA 14	A 14	XAM 2	AM	—	—	—	—	BM	B
1111	F	SD	RT	SEY 15	BL BML	LXY 3, 3	LXY 3, 7	LXY 3, 11	LXY 3, 15	LA 15	A 15	XAM 3	SEAM	—	—	—	—	BM	B

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{DD}	Supply voltage	With respect to V_{SS} (output transistors cutoff)	0.3～−18	V
V_I	Input voltage, Port S and VP		0.3～−35	V
V_I	Input voltage, other than port S (Note 1)		0.3～−18	V
V_O	Output voltage, ports S, P, and D		0.3～−35	V
V_O	Output voltage, other than ports S, P and D		0.3～−18	V
Pd	Power dissipation	Ta=25°C	1000	mW
Topr	Operating temperature		−10～70	°C
Tstg	Storage temperature		−40～125	°C

Note 1. $V_{I(\phi)}$=1.1～−35V for use of ceramic resonater

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RECOMMENDED OPERATING CONDITIONS (Ta = −10～70°C, unless otherwise noted)

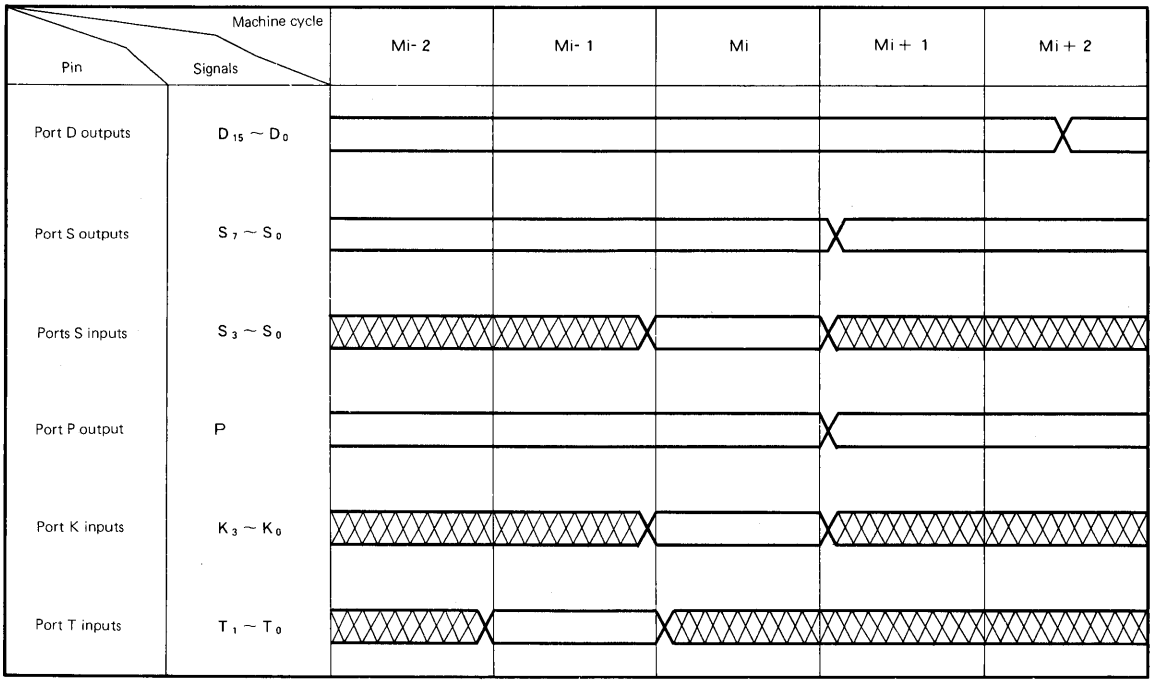
Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{DD}	Supply voltage	−10.8	−12	−13.2	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage, ports T and K and RESET inputs	−1.5	−1.0	0	V
V_{IH}	High-level input voltage, port S, INT and V_Z inputs	−0.4		0	V
$V_{IH(\phi)}$	High-level clock input voltage	−0.9		0	V
V_{IL}	Low-level input voltage, ports T and K and RESET inputs	V_{DD}		−6	V
V_{IL}	Low-level input voltage, INT and V_Z inputs	V_{DD}		−4	V
V_{IL}	Low-level input voltage, port S input	−33		−4	V
$V_{IL(\phi)}$	Low-level clock input voltage for external clock	V_{DD}		V_{DD}+2	V
V_{OL}	Low-level output voltage, Ports S, P and D	−33		0	V
$f(\phi)$	Internal clock oscillation frequency	240	300	400	kHz

ELECTRICAL CHARACTERISTICS (V_{DD} = -12V±10%, V_{SS} = 0V, f(φ) = 300 kHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Nom	Max	
V_{OH}	High-level output voltage, port D	V_{DD}=−12V, I_{OH}=−15mA, Ta=25°C	−2.5			V
V_{OH}	High-level output voltage, ports S and P	V_{DD}=−12V, I_{OH}=−8mA, Ta=25°C	−2.5			V
I_{IH}	High-level input current, ports T and K inputs	V_{DD}=−12V, V_{IH}=0V, Ta=25°C	80		490	μA
I_{IH}	High-level input current, RESET input	V_{DD}=−12V, V_{IH}=0V, Ta=25°C	20		120	μA
I_{IL}	Low-level input current, ports T and K, RESET and INT inputs	V_{DD}=−12V, V_{IL}=−12V, Ta=25°C			−12	μA
I_{OH}	High-level output current, ports S, P and D	V_{DD}=−12V, V_P=−12V, V_{OH}=0V, Ta=25°C, with output transistors cutoff	80		560	μA
I_{OL}	Low-level output current, ports S, P and D	V_{DD}=−12V, V_P=−12V, V_{OL}=−12V, Ta=25°C, with output transistors cutoff			−12	μA
$I_{I(\phi)}$	Clock input current	V_{DD}=−12V, $V_{I(\phi)}$=−12V, Ta=25°C			−10	μA
I_{DD}	Supply current	V_{DD}=−12V, Ta=25°C, with input and output pins open		−0.9	−3.4	mA

Note 1. Currents are taken as positive when flowing into the IC (zero-signal condition), with the minimum and maximum values as absolute values.
2. Total sum of high-level output current of port D must be under 75mA.

INPUT/OUTPUT INSTRUCTION TIMING



Note 1. The above timing relationships apply for the case of an instruction executed at the M_ith machine cycle.
2. ▨ The crosshatched area indicates invalid input.