MATHSTAR™

MOA1400D Product Brief

1 GHz Field Programmable Object Array™

FPOA Overview

MathStar's MOA1400D family of 1 GHz Field Programmable Object Arrays (FPOAs) delivers 2-4 times the performance of today's top FPGAs. The FPOA combines high-performance and re-programmability to meet a wide variety of application needs. FPOAs operate deterministically at 1 GHz and therefore do not suffer from timing closure delays.

The MOA1400D family of FPOAs provides 256 Arithmetic Logic Units (ALU), 80 Register Files (RF), and 64 Multiply Accumulators (MAC). The 1 GHz interconnect fabric joins each Silicon Object to the array. The Object array and associated I/O are shown below:
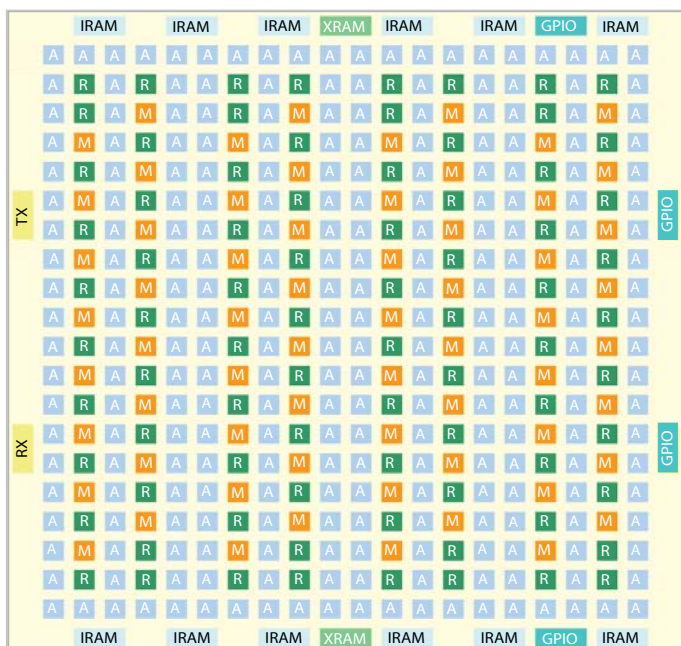
FPOA Applications:

- Digital Signal Processing
- Machine Vision
- Professional Video
- Image Processing
- Medical Imaging
- Test and Measurement
- Military/Aerospace

Discover our application-specific libraries at **www.mathstar.com**

A	Arithmetic Logic Units
R	Register Files
M	Multiply/Accumulators
IRAM	Internal SRAM Banks
XRAM	External Memory Interfaces
GPIO	General Purpose I/O Banks
TX	High Speed Transmit Ports
RX	High Speed Transmit Ports

Silicon Object and I/O Specifications

Resources	Number	Operating Speed	Size Each	Total Capability
ALU	256 objects	Up to 1 GHz	16 bits + control logic	One operation per clock
RF	80 objects	Up to 1 GHz	128 Byte + 80 tag bits	One operation per clock
MAC	64 objects	Up to 1 GHz	16x16 bit multiplier	One operation per clock
Internal RAM	12 banks	Up to 500 MHz	768 x 76 bits	5.7 GBytes/sec
External RAM	2 interfaces	Up to 200 MHz DDR	36 bit RLDRAM II	1.8 GBytes/sec
GPIO	4 banks	Up to 100 MHz	44 pins per bank	176 pins
High Speed I/O Transmit	1 port	18-400 MHz DDR	16 + 1 bit LVDS	12.8 Gbps
High Speed I/O Receive	1 port	250-400 MHz DDR	16 + 1 bit LVDS	12.8 Gbps

Array Object - Programming Features

A Arithmetic Logic Unit (ALU)
16 bit data path
4 fully programmable control bits
8 instruction state machine per ALU
Each state programmable with over 20 instructions
(Add/Sub, shift/rotate, AND/OR/XOR, etc.)

R Register File (RF)
Configurable to 64 entries of 16 + 4 bit data or 32 entries
of 32 + 8 bit data
Three operational modes
- Single-cycle, dual ported RAM
- Single-cycle, dual-ported FIFO
- Single-cycle Read Sequential/Write Random

M Multiply Accumulator (MAC)
16 x 16 single cycle throughput multiplier
32 bit intermediate result, signed or unsigned
40 bit accumulator, 256 accumulations before overflow

IRAM Internal RAM
12 independent blocks of 7.3 KB each
Each RAM is 768 Bytes deep and 76 bits wide
Two cycle access up to 1 GHz
87.5 KB maximum memory size

Periphery Object - Programming Features

XRAM External RAM
2 Independent RLDRAM II memory controllers
Each controller operates up to 200 MHz DDR
Each controller is 36 bits wide
72 MB maximum memory size per interface (packed)
1.8 GB/s maximum throughput per interface

TX High Speed LVDS Transmit port
16+1 or 8+1 bit width configuration
Operation from 18 MHz to 400 MHz DDR
Operation up to 400 MHz SDR
Up to 12.8 Gbps data throughput per interface

RX High Speed LVDS Receive port
16+1 or 8+1 bit width configuration
Operation from 250 MHz to 400 MHz DDR
Operation up to 400 MHz SDR
Up to 12.8 Gbps data throughput per interface

GPIO General Purpose I/O
176 pins total - 4 banks of 44 pins each
Operation up to 100 MHz
LVCMOS: 2.5 V and 3.3 V tolerant
Highly programmable clocking - internal, external or
asynchronous

Packaging - Environmental Specifications

Operating Parameter	Minimum	Nominal	Maximum
Voltage	1.14 V	1.2 V	1.26 V
Junction Temperature	0° C	85° C	125° C
Package Size	n/a	40 x 40 mm	n/a

Ordering Information

Maximum Operating Frequency	Product Code	Package
1 GHz	MOA1400D-10	CSBGA-668
800 MHz	MOA1400D-08	CSBGA-668
400 MHz	MOA1400D-04	CSBGA-668

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