μCOM-43/44/45 4-BIT SINGLE CHIP MICROCOMPUTERS

DESCRIPTION

The μCOM-43 Family consists of three device types designed to offer a full range of cost/performance tradeoffs. All three devices share compatible hardware and instruction set. The μCOM-43 Family is designed for general purpose controller applications and offers ideal devices for industrial controls, appliance controls, games, etc.

All three devices contain the functional blocks necessary to enable their use for both industrial and non-industrial controller applications. These blocks include: a 4-bit parallel ALU; 8-bit wide ROM for program storage; 4-bit wide RAM for data storage; stack register for subroutines; extensive I/O; and an on-chip clock generator.

The instruction set of the μCOM-43 Family is designed to perform controller-oriented functions and for efficient use of the fixed program memory space. The instruction set includes a number of multifunction instructions, powerful I/O instructions including single bit manipulation, and test-and-skip instructions for conditional processing.

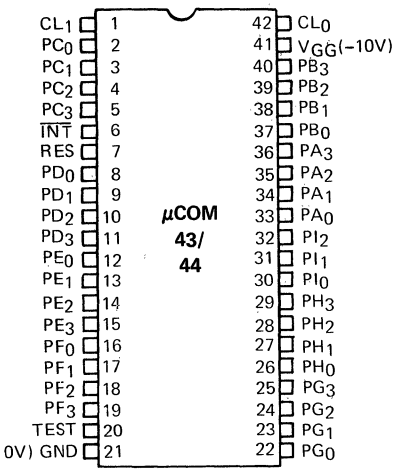
The three device types comprising the μCOM-43 Family are differentiated by ROM/RAM size and I/O lines. The μCOM-43 has 2000 x 8 ROM, 96 x 4 RAM and 35 I/O lines. The μCOM-44 has 1000 x 8 ROM, 64 x 4 RAM and 35 I/O lines. The μCOM-45 has 1000 x 8 or 640 x 8 ROM, 32 x 4 RAM and 21 I/O lines. In addition, the μCOM-43 has real hardware interrupt, 3 level stack and programmable timer, while the μCOM-44/45 have pseudo-interrupt capability and a single level stack.

FEATURES

- Stand Alone 4-Bit Microcomputers for Control Applications
- Powerful Instruction Set Capable of: Binary Addition; Decimal Addition and Subtraction; Logical Operations
- 10 μs Instruction Cycle
- Choice of ROM Size: 2000 x 8 – μCOM-43
1000 x 8 – μCOM-44
1000 x 8 – μCOM-45
640 x 8
- Choice of RAM Size: 96 x 4 – μCOM-43
64 x 4 – μCOM-44
32 x 4 – μCOM-45
- Choice of I/O Power: 35 lines – μCOM-43
35 lines – μCOM-44
21 lines – μCOM-45
- All Capable of Single Bit Manipulation and 4-Bit Parallel Processing.
- Interrupt Capability
- On-Chip Clock Generator
- Open Drain Outputs
- Choice of PMOS or CMOS Technology, Both Requiring Single Supplies
- Available in 42 Pin or 28 Pin Plastic Dual-in-Line Packages

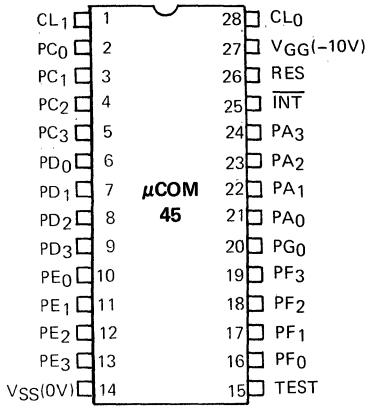
μCOM-43/44/45

PIN CONFIGURATIONS



PIN NAMES

CL_0–CL_1	External Clock Source
PC_0–PC_3	Input/Output Port C
$\overline{INT}$	Interrupt Input
RES	Reset
PD_0–PD_3	Input/Output Port D
PE_0–PE_3	Output Port E
PF_0–PF_3	Output Port F
TEST	Input for Testing (Normally GND)
PG_0–PG_3	Output Port G
PH_0–PH_3	Output Port H
PI_0–PI_3	Output Port I
PA_0–PA_3	Input Port A
PB_0–PB_3	Input Port B



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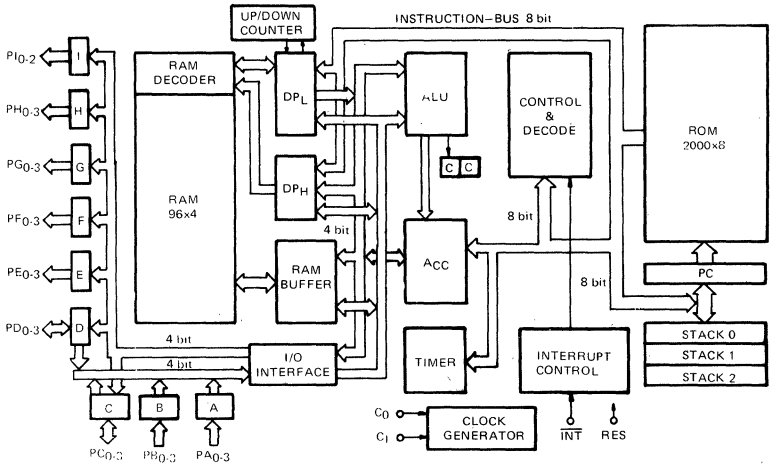
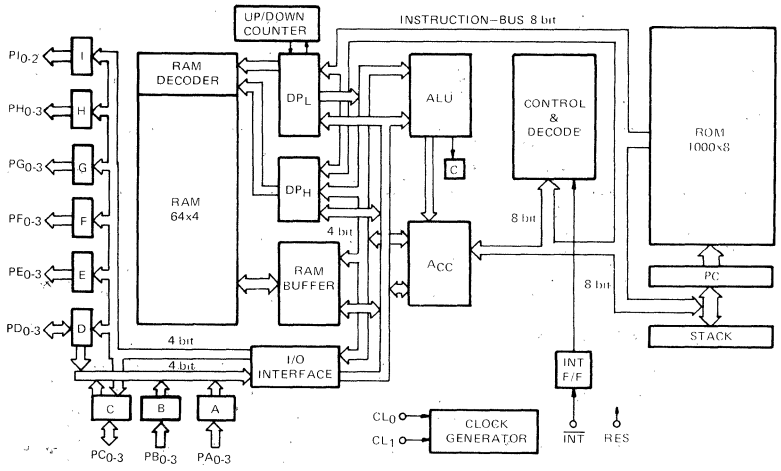
PG_0	Output Port G
PA_0–PA_3	Input Port A
$\overline{INT}$	Interrupt Input
RES	Reset

BLOCK DIAGRAM μCOM-43

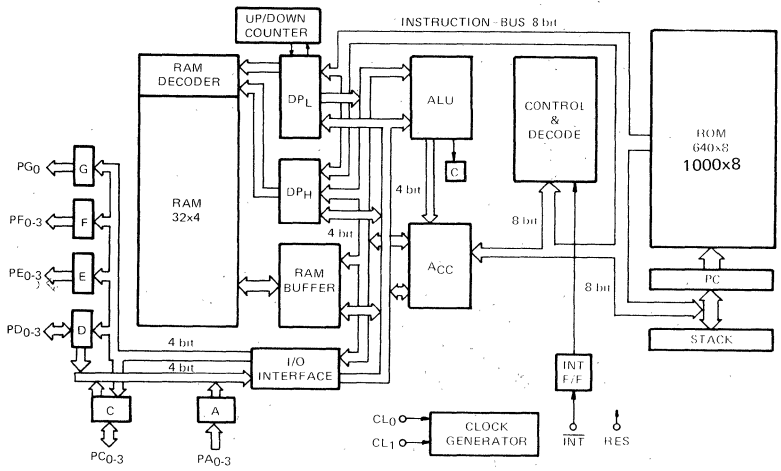


BLOCK DIAGRAMS

μCOM-44



μCOM-45



FUNCTIONAL DESCRIPTION

Program Counter

The 11-bit program counter (10-bit for μCOM-44/45) is organized as a 3-bit register (2-bit for μCOM-44/45) and an 8-bit binary up-counter (lower eight bits). The contents of the upper register specify one of the fields of the ROM. The 8-bit binary counter is divided so that the contents of the higher two bits specify one of four pages in a field and the lower six bits specify one of 64 addresses in a page. The contents of the lower eight bits of the program counter (8-bit binary up-counter) are simply incremented to execute the instructions sequentially. In a field, a page is automatically extended to the next one and four pages (256 bytes) are automatically executed.

Stack Register

The stack register is a last-in-first-out (LIFO) push down stack register organized as 3 words x 11 bits (1 word x 10 bits for μCOM-44/45). This register is used to save the contents of the program counter (return address) when a subroutine is called or an interrupt is acknowledged.

ROM (Read-Only Memory)

The user's application program is stored in the 8-bit wide mask programmable read-only memory (ROM). The ROM is organized into fields and pages. The 2000 word ROM of the μCOM-43 has eight fields, the 1000 word ROM of the μCOM-44/45 has four fields and the 640 word ROM of the low-end μCOM-45 has two fields. Each field is divided into four pages of 64 words each, and each word consists of eight bits.

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RAM (Data Memory)

The RAM is organized in a multi-row by 16 column configuration. It is addressed by a data pointer of which the higher bits (DPH) address the row and the lower bits (DPL) address the column. The exact RAM size for each device is shown below.

	RAM	ROW/COLUMN ORGANIZATION	DPH	DPL
μCOM-43	96 x 4	6 x 16	3	4
μCOM-44	64 x 4	4 x 16	2	4
μCOM-45	32 x 4	2 x 16	1	4

Internal Registers

The ALU (Arithmetic Logic Unit) and the ACC (Accumulator) form the heart of the μCOM-43 Family microcomputer system. The ALU performs arithmetic and logical operations and tests for operation results. The result of an operation by the ALU is stored in the ACC and in the carry F/F. The ACC is a 4-bit register which stores ALU results and other data to be processed. The carry F/F is a single bit flip-flop which indicates when a carry bit is generated during addition.

Flag Register (μCOM-43 Only)

A 4-bit word in the RAM can be specifically used as a software controlled general purpose flag register. The individual flag bits can be set or reset and tested for either a 1 or a 0. This can be done directly without modifying the RAM data pointer.

Working Registers (μCOM-43 Only)

There are six words in RAM that can be used as 4-bit general purpose working registers. These registers can be directly manipulated without modification of the data pointer and are used for data transfer and exchange between the data pointer and the working register, and between the ACC and the working register.

Programmable Interval Timer (μCOM-43 Only)

The μCOM-43 contains a software programmable interval timer composed of a 6-bit polynomial counter and a 6-bit programmable binary counter.

The initial setting of the timer is done using the timer set instruction STM, with the timer starting to count at the end of the STM instruction execution. The STM instruction contains six binary bits of immediate data which is loaded in the 6-bit programmable binary counter upon STM instruction execution. By varying the 6-bit immediate data, one of 64 time intervals can be programmed.

I/O Ports

The μCOM-43/44 have 35 input/output ports (μCOM-45 has 21) for communication with and control of the external world. These ports are organized into nine input/output ports (A to I). Eight ports (A to H) are composed of four bits each and the last port (I) is composed of three bits.

Input Ports	(4 bits each): A, B ①
Input/Output Ports	(4 bits each): C, D
Output Ports	(4 bits each): E, F, G ②, H ①
Output Ports	(3 bits): I ①

Notes: ① Not on μCOM-45.

② G Port on μCOM-45 is a single line.

FUNCTIONAL DESCRIPTION (CONT.)

In order to provide flexible and efficient use of these I/O ports, a variety of input/output instructions are provided which enable single bit set/reset, single bit test and conditional skip, 4-bit parallel input/output and 8-bit immediate parallel output. The I/O instructions are divided into two types, the ones dedicated to specific ports and the ones that use the 4-bit data in the DPL to select a desired port. The former include such instructions as IA and OE that specifically access port A and E, respectively. The latter require that a 4-bit code assigned to the desired port be loaded into the DPL using data pointer manipulation instructions prior to I/O instruction execution.

INSTRUCTION SET

The μCOM-43 has an 80 instruction set. The μCOM-44/45 have a 58 instruction subset of the μCOM-43. The majority of the 22 instruction difference is related to added hardware features of the μCOM-43. The instruction set is summarized below.

MNEMONIC	BYTES	CYCLES	DESCRIPTION	CONDITION FOR SKIP
CLA	1	1	$A_{CC} \leftarrow 0$	
CMA	1	1	$A_{CC} \leftarrow (A_{\overline{CC}})$	
CIA	1	1	$A_{CC} \leftarrow (A_{\overline{CC}})+1$	
INC	1	1/2-3	$A_{CC} \leftarrow (A_{CC})+1$; skip if Carry	Carry
DEC	1	1/2-3	$A_{CC} \leftarrow (A_{CC})-1$; skip if Borrow	Borrow
CLC	1	1	$C \leftarrow 0$	
STC	1	1	$C \leftarrow 1$	
XC	1	1	$(C) \leftrightarrows (C')$	
RAR	1	1	$(A_{CCn-1}) \leftarrow (A_{CCn})$; $C \leftarrow (A_{CC0})$; $(A_{CC3}) \leftarrow (C)$	
INM	1	1/2-3	$[(DP)] \leftarrow [(DP)]+1$; skip if $[(DP)]=0$	$[(DP)]=0$
DEM	1	1/2-3	$[(DP)] \leftarrow [(DP)]-1$; skip if $[(DP)]=F$	$[(DP)]=F$
AD	1	1/2-3	$A_{CC} \leftarrow (A_{CC})+[(DP)]$; skip if Carry	Carry
ADS	1	1/2-3	A_{CC}, $C \leftarrow (A_{CC})+[(DP)]+(C)$; skip if Carry	Carry
ADC	1	1	A_{CC}, $C \leftarrow (A_{CC})+[(DP)]+(C)$	
DAA	1	1	$A_{CC} \leftarrow (A_{CC})+6$	
DAS	1	1	$A_{CC} \leftarrow (A_{CC})+10$	
EXL	1	1	$A_{CC} \leftarrow (A_{CC}) \forall [(DP)]$	
LI	1	1	$A_{CC} \leftarrow I_3 I_2 I_1 I_0$	
S	1	1	$[(DP)] \leftarrow (A_{CC})$	
L	1	1	$A_{CC} \leftarrow [(DP)]$	
LM	1	1	$A_{CC} \leftarrow [(DP)]$; $DP_H \leftarrow (DP_H) \forall 0M_1M_0$	
X	1	1	$(A_{CC}) \leftrightarrows [(DP)]$	
XM	1	1	$(A_{CC}) \leftrightarrows [(DP)]$; $DP_H \leftarrow (DP_H) \forall 0M_1M_0$	
XD	1	1/2-3	$(A_{CC}) \leftrightarrows [(DP)]$; $DP_L \leftarrow (DP_L)-1$; skip if $(DP_L)=F$	$(DP_L)=F$
XMD	1	1/2-3	$(A_{CC}) \leftrightarrows [(DP)]$; $DP_H \leftarrow (DP_H) \forall 0M_1M_0$; $DP_L \leftarrow (DP_L)-1$; skip if $(DP_L)=F$	$(DP_L)=F$
XI	1	1/2-3	$(A_{CC}) \leftrightarrows [(DP)]$; $DP_L \leftarrow (DP_L)+1$; skip if $(DP_L)=0$	$(DP_L)=0$
XMI	1	1/2-3	$(A_{CC}) \leftrightarrows [(DP)]$; $DP_H \leftarrow (DP_H) \forall 0M_1M_0$; $DP_L \leftarrow (DP_L)+1$; skip if $(DP_L)=0$	$(DP_L)=0$
LDI	2	2	$DP \leftarrow I_6-I_0$	
LDZ	1	1	$DP_H \leftarrow 0$; $DP_L \leftarrow I_3 I_2 I_1 I_0$	
DED	1	1/2-3	$DP_L \leftarrow (DP_L)-1$; skip if $(DP_L)=F$	$(DP_L)=F$
IND	1	1/2-3	$DP_L \leftarrow (DP_L)+1$; skip if $(DP_L)=0$	$(DP_L)=0$
TAL	1	1	$DP_L \leftarrow (A_{CC})$	
TLA	1	1	$A_{CC} \leftarrow (DP_L)$	

MNEMONIC	BYTES	CYCLES	DESCRIPTION	CONDITION FOR SKIP
XHX	1	2	(X)←(DP$_H$)	
XLY	1	2	(Y)←(DP$_L$)	
THX	1	2	X←(DP$_H$)	
TLY	1	2	Y←(DP$_L$)	
XAZ	1	2	(Z)←(A$_{CC}$)	
XAW	1	2	(W)←(A$_{CC}$)	
TAZ	1	2	Z←(A$_{CC}$)	
TAW	1	2	W←(A$_{CC}$)	
XHR	1	2	(R)←(DP$_H$)	
XLS	1	2	(S)←(DP$_L$)	
SMB	1	1	[(DP, B$_1$B$_0$)]←1	
RMB	1	1	[(DP, B$_1$B$_0$)]←0	
TMB	1	1/2-3	skip if [(DP, B$_1$B$_0$)]=1	[(DP, B$_1$B$_0$)]=1
TAB	1	1/2-3	skip if (A$_{CC}$(B$_1$B$_0$))=1	(A$_{CC}$(B$_1$B$_0$))=1
CMB	1	1/2-3	skip if (A$_{CC}$(B$_1$B$_0$))=[(DP, B$_1$B$_0$)]	(A$_{CC}$(B$_1$B$_0$))=[(DP, B$_1$B$_0$)]
SFB	1	2	FLAG (B$_1$B$_0$)←1	
RFB	1	2	FLAG (B$_1$B$_0$)←0	
FBT	1	2/3-4	skip if (FLAG (B$_1$B$_0$))=1	(FLAG(B$_1$B$_0$))=1
FBF	1	2/3-4	skip if (FLAG (B$_1$B$_0$))=0	(FLAG(B$_1$B$_0$))=0
CM	1	1/2-3	skip if (A$_{CC}$)=[(DP)]	(A$_{CC}$)=[(DP)]
CI	2	2/3-4	skip if (A$_{CC}$)=I$_3$I$_2$I$_1$I$_0$	(A$_{CC}$)=I$_3$I$_2$I$_1$I$_0$
CLI	2	2/3-4	skip if (DP$_L$)=I$_3$I$_2$I$_1$I$_0$	(DP$_L$)=I$_3$I$_2$I$_1$I$_0$
TC	1	1/2-3	skip if (C)=1	(C)=1
TIT	1	1/2-3	skip if (INT F/F)=1; INT F/F←0	(INT F/F)=1
JCP	1	1	PC$_{5-0}$←P$_5$-P$_0$	
JMP	2	2	PC←P$_{10}$-P$_0$	
JPA	1	2	PC$_{5-0}$←A$_3$A$_2$A$_1$A$_0$00	
EI	1	2	INTE F F←1	
DI	1	2	INTE F F←0	
CZP	1	1	STACK←(PC) PC←00000P$_3$P$_2$P$_1$P$_0$00	
CAL	2	2	STACK←(PC); PC←P$_{10}$-P$_0$	
RT	1	2	PC←(STACK)	
RTS	1	3-4	PC←(STACK); PC←(PC)+1,2	Unconditional
STM	2	2	TM F F←0; TIMER←I$_5$-I$_0$	
TTM	1	1/2-3	skip if (TM F/F)=1	(TM F/F)=1
SEB	1	2	PORT E (B$_1$B$_0$)←1	
REB	1	1	PORT E (B$_1$B$_0$)←0	
SPB	1	1	PORT (DP$_L$, B$_1$B$_0$)←1	
RPB	1	1	PORT (DP$_L$, B$_1$B$_0$)←0	
TPA	1	2/3-4	skip if (PORT A (B$_1$B$_0$))=1	(PORT A (B$_1$B$_0$))=1
TPB	1	1/2-3	skip if (PORT (DL$_L$, B$_1$B$_0$))=1	(PORT (DP$_L$, B$_1$B$_0$)=1
OE	1	2	PORT E←(A$_{CC}$)	
OP	1	1	PORT (DP$_L$)←(A$_{CC}$)	
OCD	2	2	PORT C,D←I$_7$-I$_0$	
IA	2	2	A$_{CC}$←(PORT A)	
IP	1	1	A$_{CC}$←(PORT (DP$_L$))	
NOP	1	1	No Operation	

These instructions apply only to the μCOM-43.