Intel® Open Source HD Graphics and Intel Iris™ Plus Graphics

Programmer's Reference Manual

For the 2016 - 2017 Intel Core™ Processors, Celeron™ Processors, and Pentium™ Processors based on the "Kaby Lake" Platform

Volume 10: HEVC Codec Pipeline (HCP)

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Notices and Disclaimers

Table of Contents

High Efficiency Video Coding (HEVC) Introduction

The HEVC Codec Pipeline (HCP) is a fixed function hardware video codec responsible for decoding and encoding HEVC (High Efficiency Video Coding) video streams.

Scope

The primary scope of the HCP BSpec document is to provide a description of the HCP commands processed by the Video Command Streamer (VCS). The secondary scope is to provide a description of the status registers on the Message Channel Interface to support encoding and decoding of the HEVC video format.

The BSpec sections include:

- Summary of Features
- Architecture Overview
- Commands
- Register Definitions
- Acronyms and Applicable Standards

Summary of Features

The following sections define the HEVC Decoder and Encoder general features and the features specific to HEVC decoding and encoding, respectively.

HCP Hardware Pipeline Features

- Supports both decoder and encoder functions, setup on a per picture basis:
  - Hardware acceleration provides Ctb/CU level decode and encode.
  - No context switch is supported within a frame process.
- Supports Video Command Streamer (VCS):
  - Shared with MFX HW pipeline, and at any one time, only one pipeline (MFX or HCP) and one operation (decoding or encoding) can be active.
- Supports Message Channel Interface:

Feature
Supports Tile-YS and Tile-YF.
Supports Tile-Y Legacy.

- Supports NV12 video buffer plane:
  - Supports 4:2:0, 8-bit per pixel component (Y, Cb and Cr) video.
- Supports 8Kx8K frame size.

HEVC Decoder Features

- Supports full-featured HEVC Main Profile standard, up to Level 6.2.
- Supports the long format HW decoding interface:
  - All headers (SPS, PPS, Slice Header) are parsed and decoded outside the HCP HW pipeline. They are then fed to the HW through a set of HCP state commands.
- Supports inner-loop decode with hardware entry points for Encoder.
- Error detection/resiliency down to the Ctb/CU level.

HEVC Encoder Features

- Supports ENC-PAK architecture
- Supports multiple pass BRC rate control operation flow
- Supports the HEVC Main Profile standard, with certain restrictions on the feature set and coding parameters, listed in the following table:

HEVC Encoder Features and Restrictions

Note that there is a difference between what PAK supported and what ENC supported. A feature/function that is supported in the PAK, does not necessary being supported by ENC and MediaSDK and the like.

Coding Tool	Gen9 Support	Gen9 Restriction	Comments
LCU Size	Yes (spec)		Support all 3 sizes: 16x16, 32x32, 64x64.
CU Size	Yes (spec)		Support 8x8, 16x16, 32x32, 64x64. Max 64 CU per LCU; min. CU size intel supported is 8x8 for all LCU size.
PU Partition	Yes (spec)		Support all inter symmetric (square) and asymmetric (non-square) PU partitioning, according to HEVC spec. PU Size for inter : Smallest allowed is 4x8 and 8x4, and they cannot be bidirectional. Inter 4x4 PU is not allowed in Main Profile.
TU QuadTree		Partial (intel) max depth is set to 3	Max depth is 3 (64x64 CU with 4x4 TU). Decoder supports this depth, but probably no need to search this for encode. Better to just split CU. HM common conditions set the max to 2 for both inter and intra. Intel Encoder only supports 2 levels of quad-tree. That is, max_transform_hierarchy_depth_inter/intra <= 2. Max num of TUs per CU is 16.
AMP	Yes (spec)		Asymmetric Motion Partition (rectangular PU partitioning - 2NxnU, 2NxnD, nLx2N or nRx2N). Available only for 64x64 to 16x16 CU.
AMVP	Yes (spec)		Adaptive/Advanced Motion Vector Prediction : spatial and PU-based temporal co-located MV candidates with scaling. Logic available from decoder. HW PAK is supporting temporal MV candidates.

Coding Tool	Gen9 Support	Gen9 Restriction	Comments
Merge	Yes (spec)		Merge Skip and Regular Merge. Max. 5 MV Merge candidates (4 spatial + 1 temporal co-located) with scaling. Logic available from decoder. [merge_flag, merge_index, skip_flag]
Parallel Motion Merge		No (intel)	Tool for parallel decode of MVs. Since this isn't constrained by Main Profile, the decoder has to meet performance targets in the worst case anyway.
MC Interpolation Filter	Yes (spec)		¼-pel Luma MV precision, 1/8-pel Chroma MV precision. 8-tap Luma filtering for both ½-pel and ¼-pel locations (1-pass). 4-tap Chroma filtering. Use separable (first horizontal then vertical 1-D filtering) filter coefficients. Not all filter kernels are symmetrical and can map into simple arithmetic. It is a DCT-IF based filter. All operations are within 16-bit data.
Weighted Prediction	Yes (spec)		Free for PAK since decoder already has it. Cross fade and fade-in/out detection required by VME. VME must supply weights, implicit weighted prediction is not supported in HEVC. Only explicit weight is supported. They are both unidirectional and bidirectional.
Combined Reference Frame List		No (intel)	Combine List0 and List1 into a single list to remove uni-prediction signaling overhead.
Intra modes	Yes (spec)		33 directions and DC/Planar modes, with adaptive pre-filtering on reference pixels and boundary smoothing. Intel ENC-VME Mode search reduction for large CUs (64x64 and 32x32) for performance speed up with minimal loss.
IPCM (intra)		No (intel)	Can be disabled completely by SPS, or only allowed at certain CU sizes. No bit maximum on CUs in any profile/level (yet), so as of today there's no mandate to support this for encode. Gen9 PAK does not support IPCM, so ENC cannot generate IPCM mode.
Constrained Intra		No (intel)	Allow only intra neighboring blocks for current block intra-prediction. Enabling this is a coding loss and does not result in a performance improvement in HW designs.
2D DCT Transform	Yes (spec)		Square shape only; 32x32, 16x16, 8x8 and 4x4.
Transform Skip Evaluation		No (intel) ENC will estimate the use of transform skip	Significant coding gains for screen content (PowerPoint etc.). This tool is disabled in the common conditions but isn't explicitly disallowed by Main Profile. FQ is not bypass.
Sign bit hiding		No (intel)	Coding gain by removing one bypass bin per TU. Requires some smarts in the PAK.
Trellis		No (intel)	Trellis Quantization
SAO		No (intel)	Difficult to implement in single pass, performance impact in 2-pass or with previous frame search. Needs investigation. Decoder will support it.

Coding Tool	Gen9 Support	Gen9 Restriction	Comments
Loop Filter across tiles/slices boundary		No (intel)	Can be disabled for tiles and or slices in SPS, so that filter across all tiles and slices boundaries. Main profile doesn't constrain.
Scaling List	Yes (spec)		This uses the default (or custom) qp adjustment on a per-frequency basis within a TU. Good coding improvement over flat scaling.
dQP		Partial (intel) Yes for LCU; No for CU	Being able to change QP per LCU or even up to once per 8x8 CU can lead to significant coding gains. Not sure how easy it is for VME to decide qp values though.
Chroma QP offset		No (intel)	No ROI.
Dependent slices		No (intel)	It is now part of Main Profile, but Intel will not support it. SW can perform the slice repackaging without re-encoding.
Tiles		No (intel)	Although in Main Profile, it results in coding loss and doesn't improve performance on HW. SW parallel processing (multithreaded) tool
Wavefront (aka WPP)		No (intel)	Latest Main Profile spec has included Wavefront. We got a feedback that this feature is highly desirable to support high performance multithreading HEVC decoder.
Lossless coding		No (intel)	Note: this is not the same as IPCM. Also details of this are in flux.
Interlaced Video		No (intel)	Only progressive video encoding is supported.
LM mode	No (spec)		Chroma-from-luma intra prediction (Linear Mode) is not allowed in Main Profile (yet).
NSQT	No (spec)		Non square transform is not allowed in the Main Profile
ALF	No (spec)		Expensive and not in Main Profile currently. If decoder is going to support it, may consider for encoder as well.
Entropy slices	No (spec)		Not allowed in Main Profile, it is a SW parallel processing (multithreaded) tool.
Slice granularity != 0	No (spec)		Not allowed by Main Profile, and highly likely to be removed from the standard completely.

Architecture Overview

This section discusses HEVC features as follows:

Name
VP9 Decoder

VP9 Decoder

The HCP Decoder, following diagram, is a hardware based pipeline that accelerates the stream decode for an external Host Processor. The Host Processor is defined as a system processor external to the HCP that is responsible for high level parsing of the elementary stream and workload creation.

HCP Command Summary

The HCP is configured for encoding or decoding through a set of batch commands defined in the following sections. The software driver builds a frame level workload using these commands and stores these workloads in graphics memory where they are fetched by the Video Command Streamer (VCS) and presented to the HCP for processing. The commands are processed by the Workload Parser within the HCP and the hardware is configured by the Workload Parser prior to each frame level encode or decode. A workload is defined as a set of commands necessary to encode or decode one frame.

The software driver is required to read the HCP disable fuse to determine if the HCP is enabled. If it is disabled, then the software driver must not enable HCP batch commands to be sent to the HCP or a hang event may occur. Only when the HCP is enabled through the fuse, should the batch commands be sent to the HCP.

Workload Command Model

DWord0 of each command is defined in HCP DWord0 Command Definition. The HCP is selected with the **Media Instruction Opcode "7h**" for all HCP Commands.

HCP DWord0 Command Definition

DWord	Bits	Description
0	31:29	**Command Type** = PARALLEL_VIDEO_PIPE = 3h
	28:27	**Pipeline Type** = 2h
	26:23	**Media Instruction Opcode = Codec/Engine Name** = HCP = 7h
	22:16	**Media Instruction Command** = *<see Workload Command Model >*
	15:12	**Reserved: MBZ**

DWord	Bits	Description
	11:0	**Dword Length** (Excludes Dwords 0, 1) = <*command length*>

Each HCP command has assigned a media instruction command as defined in HCP Media Instruction Commands (Opcode=7h).

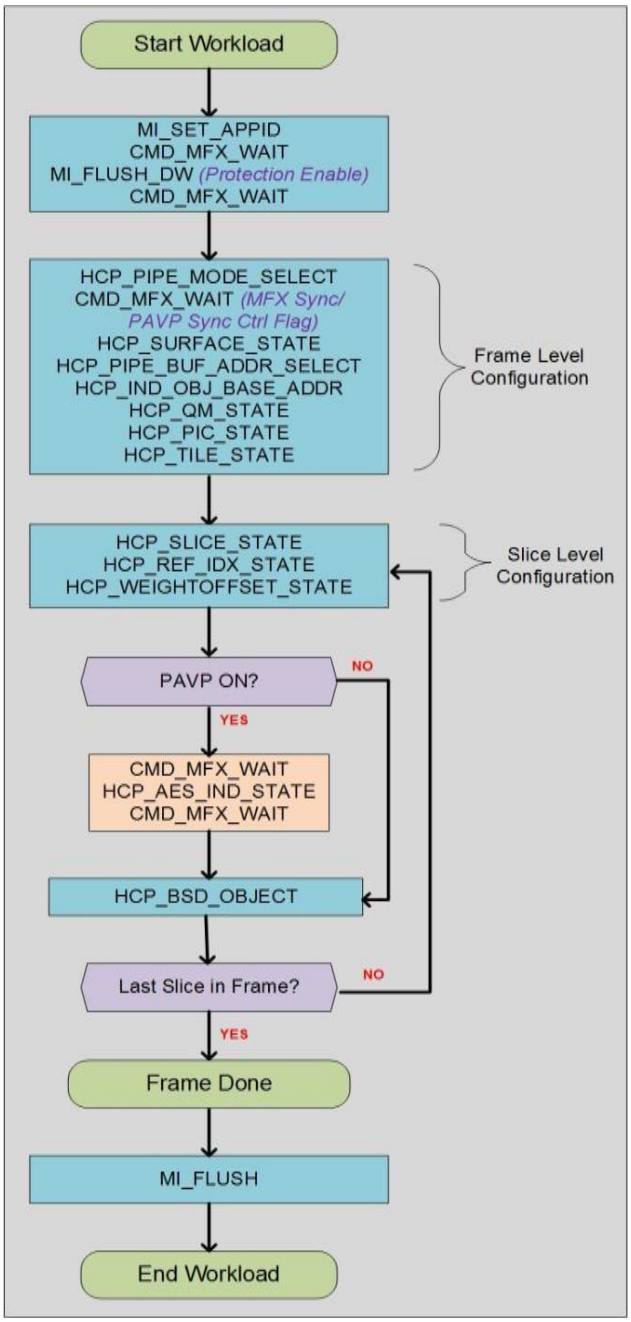
HCP Media Instruction Commands (Opcode=7h)

Media Instruction Command	Command DWord0 [22:16]	Gen9 Mode	Scope
HCP_PIPE_MODE_SELECT	0h	Enc/Dec	Picture
HCP_SURFACE_STATE	1h	Enc/Dec	Picture
HCP_PIPE_BUF_ADDR_STATE	2h	Enc/Dec	Picture
HCP_IND_OBJ_BASE_ADDR_STATE	3h	Enc/Dec	Picture
HCP_QM_STATE	4h	Enc/Dec	Picture
HCP_FQM_STATE (encoder only)	5h	Enc	Picture
Reserved	8h-Fh		
HCP_PIC_STATE	10h	Enc/Dec	Picture
HCP_TILE_STATE	11h	Dec	Picture
HCP_REF_IDX_STATE	12h	Enc/Dec	Slice
HCP_WEIGHTOFFSET	13h	Enc/Dec	Slice
HCP_SLICE_STATE	14h	Enc/Dec	Slice
Reserved	15h-1Fh		
HCP_BSD_OBJECT_STATE (decoder only)	20h	Dec	Slice
HCP_PAK_OBJECT (encoder only)	21h	Enc	LCU
HCP_INSERT_PAK_OBJECT (encoder only)	22h	Enc	Bitstream

HCP Decoder Command Sequence

The long format workload for the HCP is based upon a single frame decode. There are no states saved between frame decodes in the HCP. Once the bit stream DMA is configured with the HCP_BSD_OBJECT command, and the bit stream is presented to the HCP, the frame decode will begin.

HCP Long Format Decode Workload Flowchart



HCP Encoder Command Sequence

For a single frame encoding process (w/o multiple slices per frame), the command sequence is listed below. There are no states saved between frame encoded in the HCP. There should be no other commands or context switch within a group of PAK OBJECT Commands, representing a complete slice. HCP and MFX share the same VCS, but there is no common encoding and decoding command that can be executed in both pipes mi_flush and MMIO commands.

------ Per Frame Level Commands

HCP_PIPE_MODE_SELECT

HCP_SURFACE_STATE

HCP_PIPE_BUF_ADDR_STATE

HCP_IND_OBJ_BASE_ADDR_STATE

HCP_FQM_STATE – issue n number of times

HCP_QM_STATE – issue n number of times

HCP_PIC_STATE

------- Per Slice Level Commands (2 cases)

------- A Frame with only 1 Slice:

HCP_REF_IDX_STATE – set to provide L0 list for a P or B-Slice

HCP_REF_IDX_STATE – set to provide L1 list for a B-Slice

HCP_WEIGHTOFFSET_STATE Command – set to provide for L0 of a P or B-Slice

HCP_WEIGHTOFFSET_STATE Command - set to provide for L1 of a B-Slice

HCP_SLICE_STATE

HCP_PAK_INSERT_OBJECT – if header present at 1st slice start

------- A group of LCUs Per Slice

HCP_PAK_OBJECT

…

HCP_PAK_INSERT_OBJECT – if tail present at frame end

MI_FLUSH – when the frame is done

------ A Frame with Multiple Slices:

HCP_REF_IDX_STATE – set to provide L0 list for a P or B-Slice

HCP_REF_IDX_STATE – set to provide L1 list for a B-Slice

HCP_WEIGHTOFFSET_STATE Command – set to provide for L0 of a P or B-Slice

HCP_WEIGHTOFFSET_STATE Command - set to provide for L1 of a B-Slice

HCP_SLICE_STATE

HCP_PAK_INSERT_OBJECT – if header present at 1st slice start of a frame

HCP_PAK_OBJECT - a group of LCUs for a slice or a frame

…

HCP_PAK_INSERT_OBJECT – if tail present at slice or frame end

HCP_REF_IDX_STATE – set to provide L0 list for a P or B-Slice

HCP_REF_IDX_STATE – set to provide L1 list for a B-Slice

HCP_WEIGHTOFFSET_STATE Command – set to provide for L0 of a P or B-Slice

HCP_WEIGHTOFFSET_STATE Command - set to provide for L1 of a B-Slice

HCP_SLICE_STATE

HCP_PAK_INSERT_OBJECT – if header present at slice start

HCP_PAK_OBJECT - a group of LCUs for a slice or a frame

…

HCP_PAK_INSERT_OBJECT – if tail present at last slice end (frame end)

MI_FLUSH – when the frame is done

MFX_STITCH_OBJECT – a generic bitstream stitching command from MFX pipe

MI_FLUSH

MI_FLUSH is not allowed between Slices. HEVC CABAC has simplified its operation from AVC. There is no longer a BSP_BUF_BASE_ADDR_STATE Command, as only a small local internal buffer is needed for BSP/BSE row store. THE HCP PAK_INSERT_OBJECT has been designed to support both inline and indirectly payload. Nevertheless, the MFX_STITCH_OBJECT command can still be used to stitch HEVC bitstreams together, and is run in the MFX pipe. No HEVC specific STITCH command is implemented. The SURFACE_STATE command for HEVC is redesigned and much simplified from that of MFX pipe.

Memory Address Attributes

This section defines the memory address attributes for the third DWord of the HCP command buffer address.

NOTE: The first DWord defines the lower address range and the second Dword defines the upper address range in the HCP command buffer address.

MemoryAddressAttributes

HCP Pipe Common Commands

The HCP Pipe Common Commands specify the HEVC Decoder pipeline level configuration.

Commands
HCP_PIPE_MODE_SELECT (VideoCS)
HCP_SURFACE_STATE (VideoCS)
HCP_PIPE_BUF_ADDR_STATE (VideoCS)

Buffer Name	Minimum Size in CLs	Notes
Deblocking Filter Line Buffer	((picture_width_in_pixels + 31) & (-32)) » 3	Eq. ensures multiple of 4
Deblocking Filter Tile Line Buffer	((picture_width_in_pixels + 31) & (-32)) » 3	Eq. ensures multiple of 4
Deblocking Filter Tile Column Buffer	((picture_height_in_pixels + 6*pic_height_in_ctb + 31) & (-32)) » 3	Eq. ensures multiple of 4
Metadata Line Buffer (all intra slices)	(picture_width_in_pixels + pic_width_in_lcu*8 + 1023) » 9	Eq. ensures multiple of 2
Metadata Tile Line Buffer (all intra slices)	(picture_width_in_pixels + pic_width_in_lcu *16 + 1023) » 9	Eq. ensures multiple of 2
Metadata Tile Column Buffer (all intra slices)	(picture_height_in_pixels + picture_height_in_pixels *8 + 1023) » 9	Eq. ensures multiple of 2
Metadata Line Buffer (some inter slices)	(((picture_width_in_pixels+15)»4)*188 + pic_width_in_lcu*9 + 1023) » 9	Eq. ensures multiple of 2
Metadata Tile Line Buffer (some inter slices)	(((picture_width_in_pixels +15)»4)*172 + pic_width_in_lcu *9 + 1023) » 9	Eq. ensures multiple of 2
Metadata Tile Column Buffer (some inter slices)	(((picture_height_in_pixels +15)»4)*176 + picture_height_in_lcu *89 + 1023) » 9	Eq. ensures multiple of 2
SAO Line Buffer	(((picture_width_in_pixels » 1) + pic_width_in_ctb * 3)+15) & (-16)) » 3	Eq. ensures multiple of 2
SAO Tile Line Buffer	(((picture_width_in_pixels » 1) + picture_width_in_ctb * 6)+15) & (-16)) » 3	Eq. ensures multiple of 2
SAO Tile Column Buffer	(((picture_height_in_pixels » 1) + pic_height_in_ctb * 6)+15) & (-16)) » 3	Eq. ensures multiple of 2

Buffer Name	Minimum Size in CLs	Notes
Current and Collocated Motion Vector Temporal Buffer (lcu=16x16)	(((picture_width_in_pixels+63)»6)*((picture_height_in_pixels+15)»4)	Eq. ensures multiple of 2
Current and Collocated Motion Vector Temporal Buffer (lcu>16x16)	(((picture_width_in_pixels+31)»5)*((picture_height_in_pixels+31)»5)	Eq. ensures multiple of 2

Internal Media Rowstore Table

If the internal Media Rowstore exists, driver should use the storage as the following table indicates.

HEVC Pipeline	Frame Width	DAT	DF	SAO	DAT Addr	DF Addr	SAO Addr
HEVC	<= 2048	Y	Y	Y	0	64	320
	2048 < x <= 4096	Y	Y	N	0	128	N/A
	4096 < x <=8196	Y	N	N	0	N/A	N/A

Commands
HCP_IND_OBJ_BASE_ADDR_STATE (VideoCS)
HCP_QM_STATE (VideoCS)
HCP_FQM_STATE VideoCS

Buffer Size Requirements

HEVC Buffer Size Requirements (8 bit)

Buffer Name	Minimum Size in CLs	Notes
Deblocking Filter Line Buffer	((picture_width_in_pixels + 31) & (-32)) » 3	Eq. ensures multiple of 4
Deblocking Filter Tile Line Buffer	((picture_width_in_pixels + 31) & (-32)) » 3	Eq. ensures multiple of 4
Deblocking Filter Tile Column Buffer	((picture_height_in_pixels + 6*pic_height_in_ctb + 31) & (-32)) » 3	Eq. ensures multiple of 4
Metadata Line Buffer (all intra slices)	(picture_width_in_pixels + pic_width_in_lcu*8 + 1023) » 9	Eq. ensures multiple of 2
Metadata Tile Line Buffer (all intra slices)	(picture_width_in_pixels + pic_width_in_lcu *8 + 1023) » 9	Eq. ensures multiple of 2
Metadata Tile Column Buffer (all intra slices)	(picture_height_in_pixels + picture_height_in_lcu * 16 + 1023) » 9	Eq. ensures multiple of 2
Metadata Line Buffer (some inter slices)	(((picture_width_in_pixels+15)»4)*188 + pic_width_in_lcu * 9 + 1023) » 9	Eq. ensures multiple of 2
Metadata Tile Line Buffer (some inter slices)	(((picture_width_in_pixels +15)»4)*172 + pic_width_in_lcu * 9 + 1023) » 9	Eq. ensures multiple of 2

Buffer Name	Minimum Size in CLs	Notes
Metadata Tile Column Buffer (some inter slices)	**Equation:** (((picture_height_in_pixels +15)»4)*176 + picture_height_in_lcu * 89 + 1023) » 9	Eq. ensures multiple of 2
SAO Line Buffer	(((picture_width_in_pixels » 1) + pic_width_in_ctb * 3)+15) & (-16)) » 3	Eq. ensures multiple of 2
SAO Tile Line Buffer	(((picture_width_in_pixels » 1) + picture_width_in_ctb * 6)+15) & (-16)) » 3	Eq. ensures multiple of 2
SAO Tile Column Buffer	(((picture_height_in_pixels » 1) + pic_height_in_ctb * 6)+15) & (-16)) » 3	Eq. ensures multiple of 2
Current and Collocated Motion Vector Temporal Buffer (lcu=16x16)	(((picture_width_in_pixels+63)»6)*((picture_height_in_pixels+15)»4)	Eq. ensures multiple of 2
Current and Collocated Motion Vector Temporal Buffer (lcu>16x16)	(((picture_width_in_pixels+31)»5)*((picture_height_in_pixels+31)»5)	Eq. ensures multiple of 2
SSE Line Buffer	(Picture_width_in_lcu + 2) « 4	

HEVC 10 bit Buffer Size Requirements

Buffer Name	Minimum Size in CLs	Notes
Deblocking Filter Line Buffer	((picture_width_in_pixels + 31) & (-32)) » **2**	Eq. ensures multiple of 4
Deblocking Filter Tile Line Buffer	((picture_width_in_pixels + 31) & (-32)) » **2**	Eq. ensures multiple of 4
Deblocking Filter Tile Column Buffer	((picture_height_in_pixels + 6*pic_height_in_ctb + 31) & (-32)) » **2**	Eq. ensures multiple of 4
Metadata Line Buffer (all intra slices)	(picture_width_in_pixels + pic_width_in_lcu*8 + 1023) » 9	Eq. ensures multiple of 2
Metadata Tile Line Buffer (all intra slices)	(picture_width_in_pixels + pic_width_in_lcu *8 + 1023) » 9	Eq. ensures multiple of 2
Metadata Tile Column Buffer (all intra slices)	(picture_height_in_pixels + picture_height_in_lcu * 16 + 1023) » 9	Eq. ensures multiple of 2
Metadata Line Buffer (some inter slices)	(((picture_width_in_pixels+15)»4)*188 + pic_width_in_lcu*9 + 1023) » 9	Eq. ensures multiple of 2
Metadata Tile Line Buffer (some inter slices)	(((picture_width_in_pixels +15)»4)*172 + pic_width_in_lcu *9 + 1023) » 9	Eq. ensures multiple of 2
Metadata Tile Column Buffer (some inter slices)	(((picture_height_in_pixels +15)»4)*176 + picture_height_in_lcu * 89 + 1023) » 9	Eq. ensures multiple of 2
SAO Line Buffer	(((picture_width_in_pixels » 1) + pic_width_in_ctb * 3)+15) & (-16)) » **2**	Eq. ensures multiple of 2

Buffer Name	Minimum Size in CLs	Notes
SAO Tile Line Buffer	(((picture_width_in_pixels » 1) + picture_width_in_ctb * 6)+15) & (-16)) » **2**	Eq. ensures multiple of 2
SAO Tile Column Buffer	(((picture_height_in_pixels » 1) + pic_height_in_ctb * 6)+15) & (-16)) » **2**	Eq. ensures multiple of 2
Current and Collocated Motion Vector Temporal Buffer (lcu=16x16)	(((picture_width_in_pixels+63)»6)*((picture_height_in_pixels+15)»4)	Eq. ensures multiple of 2
Current and Collocated Motion Vector Temporal Buffer (lcu>16x16)	(((picture_width_in_pixels+31)»5)*((picture_height_in_pixels+31)»5)	Eq. ensures multiple of 2
SSE Line Buffer	(Picture_width_in_lcu + 2) « 4	

Internal Media Rowstore Table

If the internal Media Rowstore exists, driver should use the storage as the following table indicates.

HEVC Pipeline	Frame Width	DAT	DF	SAO	DAT Addr	DF Addr	SAO Addr
HEVC	<= 2048	Y	Y	Y	0	64	320
	2048 < x <= 4096	Y	Y	N	0	128	N/A
	4096 < x <=8196	Y	N	N	0	N/A	N/A

VP9 Common Commands

Commands
HCP_PIPE_MODE_SELECT
HCP_SURFACE_STATE
HCP_PIPE_BUF_ADDR_STATE
HCP_IND_OBJ_BASE_ADDR_STATE
HCP_VP9_SEGMENT_STATE
HCP_VP9_PIC_STATE

HCP Common Commands

HCP_PIC_STATE (VideoCS)

HCP_TILE_STATE (VideoCS)

HCP_REF_IDX_STATE (VideoCS)

HCP_WEIGHTOFFSET_STATE (VideoCS)

HCP_SLICE_STATE (VideoCS)

HEVC_VP9_RDOQ_STATE

VP9 Commands

HCP_BSD_OBJECT (triggers HW start)

HCP_VP9_PAK_OBJECT

Tile Size and CU Stream-out Records

CU statistics record (individual PUs per record down to 8x8 only) (Note: For Advanced BRC but not supported in HW yet)

Fields	Bits	
Skip	3:0	Indicates Skip flag Group 4 4x4s -> 4 bits
InterMode	11:4	InterMode: 0 NEARESTMV, 1 NEARMV, 2 ZEROMV, 3NEWMV Group 4 4x4s total 8 bits
Reserved	15:12	
NZ coeff count	28:16	Number of non-zero coeffs; sum of YUV, 13bits
Reserved	31:29	
NumBitsforCoeffs	47:32	Number of Bits for coefficients per block, 16bits
NumBitsforBlock	63:48	Number of Bits in block

Stream-in Probability Table

In Encoder mode, two sets of this table will be streamed out: one for the current frame probability update and one for future frame.

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT		State counter EBB Address	Coefficient counter EBB Address							
												4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
CL aligned	0	1	tx_probs_8x8 [0] [0..0]	100	100	0	0	0	0	MODE COUNTERS (counts tx)	0-17								
	1	1	tx_probs_8x8 [1] [0..0]	66	66	0	1	1											
	2	2	tx_probs_16x16 [0] [0..1]	20, 152	20, 152	0	2	2											
	4	2	tx_probs_16x16 [1] [0..1]	15, 101	15, 101	0	4	4											
	6	3	tx_probs_32x32 [0] [0..2]	3, 136, 37	3, 136, 37	0	6	6											
	9	3	tx_probs_32x32 [1] [0..2]	5, 52, 13	5, 52, 13	0	9	9											
	12	52	DUMMY	0, 0, 0, 0	0, 0, 0, 0	52	12												
CL aligned	64	3	coef_probs_4x4 [0] [0] [0] [0]	195, 29, 183	195,	0	12		8	COEFF COUNTERS (coeff_count_mod		0-28							

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT		State counter EBB Address	Coefficient counter EBB Address							
												4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
			[0..2]		29, 183					el_coeff)		7							
	67	3	coef_probs_4x4 [0] [0] [0] [1] [0..2]	84, 49, 136	84, 49, 136	0	15												
	70	3	coef_probs_4x4 [0] [0] [0] [2] [0..2]	8, 42, 71	8, 42, 71	0	18												
	73	3	coef_probs_4x4 [0] [0] [1] [0] [0..2]	31, 107, 169	31, 107, 169	0	21												
	76	3	coef_probs_4x4 [0] [0] [1] [1] [0..2]	35, 99, 159	35, 99, 159	0	24												
	79	3	coef_probs_4x4 [0] [0] [1] [2] [0..2]	17, 82, 140	17, 82, 140	0	27												
	82	3	coef_probs_4x4 [0] [0] [1] [3] [0..2]	8, 66, 114	8, 66, 11	0	30												

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
					4													
	85	3	coef_probs_4x4 [0] [0] [1] [4] [0..2]	2, 44, 76	2, 44, 76	0	33											
	88	3	coef_probs_4x4 [0] [0] [1] [5] [0..2]	1, 19, 32	1, 19, 32	0	36											
	91	3	coef_probs_4x4 [0] [0] [2] [0] [0..2]	40, 132, 201	40, 132, 201	0	39											
	94	3	coef_probs_4x4 [0] [0] [2] [1] [0..2]	29, 114, 187	29, 114, 187	0	42											
	97	3	coef_probs_4x4 [0] [0] [2] [2] [0..2]	13, 91, 157	13, 91, 157	0	45											
	100	3	coef_probs_4x4 [0] [0] [2] [3] [0..2]	7, 75, 127	7, 75, 127	0	48											
	103	3	coef_probs_4x4	3, 58,	3,	0	51											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
			[0] [0] [2] [4] [0..2]	95	58, 95													
	106	3	coef_probs_4x4 [0] [0] [2] [5] [0..2]	1, 28, 47	1, 28, 47	0	54											
	109	3	coef_probs_4x4 [0] [0] [3] [0] [0..2]	69, 142, 221	69, 142, 221	0	57											
	112	3	coef_probs_4x4 [0] [0] [3] [1] [0..2]	42, 122, 201	42, 122, 201	0	60											
	115	3	coef_probs_4x4 [0] [0] [3] [2] [0..2]	15, 91, 159	15, 91, 159	0	63											
	118	3	coef_probs_4x4 [0] [0] [3] [3] [0..2]	6, 67, 121	6, 67, 121	0	66											
	121	3	coef_probs_4x4 [0] [0] [3] [4] [0..2]	1, 42, 77	1, 42, 77	0	69											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
	124	3	coef_probs_4x4 [0] [0] [3] [5] [0..2]	1, 17, 31	1, 17, 31	0	72											
	127	3	coef_probs_4x4 [0] [0] [4] [0] [0..2]	102, 148, 228	102, 148, 228	0	75											
	130	3	coef_probs_4x4 [0] [0] [4] [1] [0..2]	67, 117, 204	67, 117, 204	0	78											
	133	3	coef_probs_4x4 [0] [0] [4] [2] [0..2]	17, 82, 154	17, 82, 154	0	81											
	136	3	coef_probs_4x4 [0] [0] [4] [3] [0..2]	6, 59, 114	6, 59, 114	0	84											
	139	3	coef_probs_4x4 [0] [0] [4] [4] [0..2]	2, 39, 75	2, 39, 75	0	87											
	142	3	coef_probs_4x4	1, 15,	1,	0	90											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
			[0] [0] [4] [5] [0..2]	29	15, 29													
	145	3	coef_probs_4x4 [0] [0] [5] [0] [0..2]	156, 57, 233	156, 57, 233	0	93											
	148	3	coef_probs_4x4 [0] [0] [5] [1] [0..2]	119, 57, 212	119, 57, 212	0	96											
	151	3	coef_probs_4x4 [0] [0] [5] [2] [0..2]	58, 48, 163	58, 48, 163	0	99											
	154	3	coef_probs_4x4 [0] [0] [5] [3] [0..2]	29, 40, 124	29, 40, 124	0	102											
	157	3	coef_probs_4x4 [0] [0] [5] [4] [0..2]	12, 30, 81	12, 30, 81	0	105											
	160	3	coef_probs_4x4 [0] [0] [5] [5] [0..2]	3, 12, 31	3, 12, 31	0	108											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
	163	3	coef_probs_4x4 [0] [1] [0] [0] [0..2]	191, 107, 226	191, 107, 226	0	111											
	166	3	coef_probs_4x4 [0] [1] [0] [1] [0..2]	124, 117, 204	124, 117, 204	0	114											
	169	3	coef_probs_4x4 [0] [1] [0] [2] [0..2]	25, 99, 155	25, 99, 155	0	117											
	172	3	coef_probs_4x4 [0] [1] [1] [0] [0..2]	29, 148, 210	29, 148, 210	0	120											
	175	3	coef_probs_4x4 [0] [1] [1] [1] [0..2]	37, 126, 194	37, 126, 194	0	123											
	178	3	coef_probs_4x4	8, 93,	8,	0	12											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
			[0] [1] [1] [2] [0..2]	157	93, 157		6											
	181	3	coef_probs_4x4 [0] [1] [1] [3] [0..2]	2, 68, 118	2, 68, 118	0	129											
	184	3	coef_probs_4x4 [0] [1] [1] [4] [0..2]	1, 39, 69	1, 39, 69	0	132											
	187	3	coef_probs_4x4 [0] [1] [1] [5] [0..2]	1, 17, 33	1, 17, 33	0	135											
	190	3	coef_probs_4x4 [0] [1] [2] [0] [0..2]	41, 151, 213	41, 151, 213	0	138											
	193	3	coef_probs_4x4 [0] [1] [2] [1] [0..2]	27, 123, 193	27, 123, 193	0	141											
	196	3	coef_probs_4x4 [0] [1] [2] [2] [0..2]	3, 82, 144	3, 82, 14	0	144											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults					Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
												4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
					4														
	199	3	coef_probs_4x4 [0] [1] [2] [3] [0..2]	1, 58, 105	1, 58, 105	0	147												
	202	3	coef_probs_4x4 [0] [1] [2] [4] [0..2]	1, 32, 60	1, 32, 60	0	150												
	205	3	coef_probs_4x4 [0] [1] [2] [5] [0..2]	1, 13, 26	1, 13, 26	0	153												
	208	3	coef_probs_4x4 [0] [1] [3] [0] [0..2]	59, 159, 220	59, 159, 220	0	156												
	211	3	coef_probs_4x4 [0] [1] [3] [1] [0..2]	23, 126, 198	23, 126, 198	0	159												
	214	3	coef_probs_4x4 [0] [1] [3] [2] [0..2]	4, 88, 151	4, 88, 151	0	162												
	217	3	coef_probs_4x4	1, 66,	1,	0	16												

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
			[0] [1] [3] [3] [0..2]	114	66, 114		5											
	220	3	coef_probs_4x4 [0] [1] [3] [4] [0..2]	1, 38, 71	1, 38, 71	0	168											
	223	3	coef_probs_4x4 [0] [1] [3] [5] [0..2]	1, 18, 34	1, 18, 34	0	171											
	226	3	coef_probs_4x4 [0] [1] [4] [0] [0..2]	114, 136, 232	114, 136, 232	0	174											
	229	3	coef_probs_4x4 [0] [1] [4] [1] [0..2]	51, 114, 207	51, 114, 207	0	177											
	232	3	coef_probs_4x4 [0] [1] [4] [2] [0..2]	11, 83, 155	11, 83, 155	0	180											
	235	3	coef_probs_4x4 [0] [1] [4] [3]	3, 56, 105	3, 56,	0	183											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
			[0..2]		105													
	238	3	coef_probs_4x4 [0] [1] [4] [4] [0..2]	1, 33, 65	1, 33, 65	0	186											
	241	3	coef_probs_4x4 [0] [1] [4] [5] [0..2]	1, 17, 34	1, 17, 34	0	189											
	244	3	coef_probs_4x4 [0] [1] [5] [0] [0..2]	149, 65, 234	149, 65, 234	0	192											
	247	3	coef_probs_4x4 [0] [1] [5] [1] [0..2]	121, 57, 215	121, 57, 215	0	195											
	250	3	coef_probs_4x4 [0] [1] [5] [2] [0..2]	61, 49, 166	61, 49, 166	0	198											
	253	3	coef_probs_4x4 [0] [1] [5] [3] [0..2]	28, 36, 114	28, 36, 114	0	201											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
	256	3	coef_probs_4x4 [0] [1] [5] [4] [0..2]	12, 25, 76	12, 25, 76	0	204											
	259	3	coef_probs_4x4 [0] [1] [5] [5] [0..2]	3, 16, 42	3, 16, 42	0	207											
	262	3	coef_probs_4x4 [1] [0] [0] [0] [0..2]	214, 49, 220	214, 49, 220	0	210					0-287						
	265	3	coef_probs_4x4 [1] [0] [0] [1] [0..2]	132, 63, 188	132, 63, 188	0	213											
	268	3	coef_probs_4x4 [1] [0] [0] [2] [0..2]	42, 65, 137	42, 65, 137	0	216											
	271	3	coef_probs_4x4 [1] [0] [1] [0] [0..2]	85, 137, 221	85, 137, 221	0	219											
	274	3	coef_probs_4x4	104,	10	0	22											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
			[1] [0] [1] [1] [0..2]	131, 216	4, 131, 216		2											
	277	3	coef_probs_4x4 [1] [0] [1] [2] [0..2]	49, 111, 192	49, 111, 192	0	225											
	280	3	coef_probs_4x4 [1] [0] [1] [3] [0..2]	21, 87, 155	21, 87, 155	0	228											
	283	3	coef_probs_4x4 [1] [0] [1] [4] [0..2]	2, 49, 87	2, 49, 87	0	231											
	286	3	coef_probs_4x4 [1] [0] [1] [5] [0..2]	1, 16, 28	1, 16, 28	0	234											
	289	3	coef_probs_4x4 [1] [0] [2] [0] [0..2]	89, 163, 230	89, 163, 230	0	237											
	292	3	coef_probs_4x4	90,	90,	0	24											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
			[1] [0] [2] [1] [0..2]	137, 220	137, 220		0											
	295	3	coef_probs_4x4 [1] [0] [2] [2] [0..2]	29, 100, 183	29, 100, 183	0	243											
	298	3	coef_probs_4x4 [1] [0] [2] [3] [0..2]	10, 70, 135	10, 70, 135	0	246											
	301	3	coef_probs_4x4 [1] [0] [2] [4] [0..2]	2, 42, 81	2, 42, 81	0	249											
	304	3	coef_probs_4x4 [1] [0] [2] [5] [0..2]	1, 17, 33	1, 17, 33	0	252											
	307	3	coef_probs_4x4 [1] [0] [3] [0] [0..2]	108, 167, 237	108, 167, 237	0	255											
	310	3	coef_probs_4x4	55,	55,	0	25											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
			[1] [0] [3] [1] [0..2]	133, 222	133, 222		8											
	313	3	coef_probs_4x4 [1] [0] [3] [2] [0..2]	15, 97, 179	15, 97, 179	0	261											
	316	3	coef_probs_4x4 [1] [0] [3] [3] [0..2]	4, 72, 135	4, 72, 135	0	264											
	319	3	coef_probs_4x4 [1] [0] [3] [4] [0..2]	1, 45, 85	1, 45, 85	0	267											
	322	3	coef_probs_4x4 [1] [0] [3] [5] [0..2]	1, 19, 38	1, 19, 38	0	270											
	325	3	coef_probs_4x4 [1] [0] [4] [0] [0..2]	124, 146, 240	124, 146, 240	0	273											
	328	3	coef_probs_4x4 [1] [0] [4] [1]	66, 124,	66, 12	0	276											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
			[0..2]	224	4, 224													
	331	3	coef_probs_4x4 [1] [0] [4] [2] [0..2]	17, 88, 175	17, 88, 175	0	279											
	334	3	coef_probs_4x4 [1] [0] [4] [3] [0..2]	4, 58, 122	4, 58, 122	0	282											
	337	3	coef_probs_4x4 [1] [0] [4] [4] [0..2]	1, 36, 75	1, 36, 75	0	285											
	340	3	coef_probs_4x4 [1] [0] [4] [5] [0..2]	1, 18, 37	1, 18, 37	0	288											
	343	3	coef_probs_4x4 [1] [0] [5] [0] [0..2]	141, 79, 241	141, 79, 241	0	291											
	346	3	coef_probs_4x4 [1] [0] [5] [1] [0..2]	126, 70, 227	126, 70, 22	0	294											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
					7													
	349	3	coef_probs_4x4 [1] [0] [5] [2] [0..2]	66, 58, 182	66, 58, 182	0	297											
	352	3	coef_probs_4x4 [1] [0] [5] [3] [0..2]	30, 44, 136	30, 44, 136	0	300											
	355	3	coef_probs_4x4 [1] [0] [5] [4] [0..2]	12, 34, 96	12, 34, 96	0	303											
	358	3	coef_probs_4x4 [1] [0] [5] [5] [0..2]	2, 20, 47	2, 20, 47	0	306											
	361	3	coef_probs_4x4 [1] [1] [0] [0] [0..2]	229, 99, 249	229, 99, 249	0	309											
	364	3	coef_probs_4x4 [1] [1] [0] [1] [0..2]	143, 111, 235	143, 111, 235	0	312											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
	367	3	coef_probs_4x4 [1] [1] [0] [2] [0..2]	46, 109, 192	46, 109, 192	0	315											
	370	3	coef_probs_4x4 [1] [1] [1] [0] [0..2]	82, 158, 236	82, 158, 236	0	318											
	373	3	coef_probs_4x4 [1] [1] [1] [1] [0..2]	94, 146, 224	94, 146, 224	0	321											
	376	3	coef_probs_4x4 [1] [1] [1] [2] [0..2]	25, 117, 191	25, 117, 191	0	324											
	379	3	coef_probs_4x4 [1] [1] [1] [3] [0..2]	9, 87, 149	9, 87, 149	0	327											
	382	3	coef_probs_4x4 [1] [1] [1] [4] [0..2]	3, 56, 99	3, 56, 99	0	330											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
	385	3	coef_probs_4x4 [1] [1] [1] [5] [0..2]	1, 33, 57	1, 33, 57	0	333											
	388	3	coef_probs_4x4 [1] [1] [2] [0] [0..2]	83, 167, 237	83, 167, 237	0	336											
	391	3	coef_probs_4x4 [1] [1] [2] [1] [0..2]	68, 145, 222	68, 145, 222	0	339											
	394	3	coef_probs_4x4 [1] [1] [2] [2] [0..2]	10, 103, 177	10, 103, 177	0	342											
	397	3	coef_probs_4x4 [1] [1] [2] [3] [0..2]	2, 72, 131	2, 72, 131	0	345											
	400	3	coef_probs_4x4 [1] [1] [2] [4] [0..2]	1, 41, 79	1, 41, 79	0	348											
	403	3	coef_probs_4x4	1, 20,	1,	0	35											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults			Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
										4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
			[1] [1] [2] [5] [0..2]	39	20, 39		1											
	406	3	coef_probs_4x4 [1] [1] [3] [0] [0..2]	99, 167, 239	99, 167, 239	0	354											
	409	3	coef_probs_4x4 [1] [1] [3] [1] [0..2]	47, 141, 224	47, 141, 224	0	357											
	412	3	coef_probs_4x4 [1] [1] [3] [2] [0..2]	10, 104, 178	10, 104, 178	0	360											
	415	3	coef_probs_4x4 [1] [1] [3] [3] [0..2]	2, 73, 133	2, 73, 133	0	363											
	418	3	coef_probs_4x4 [1] [1] [3] [4] [0..2]	1, 44, 85	1, 44, 85	0	366											
	421	3	coef_probs_4x4 [1] [1] [3] [5]	1, 22, 47	1, 22,	0	369											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
			[0..2]		47													
	424	3	coef_probs_4x4 [1] [1] [4] [0] [0..2]	127, 145, 243	127, 145, 243	0	372											
	427	3	coef_probs_4x4 [1] [1] [4] [1] [0..2]	71, 129, 228	71, 129, 228	0	375											
	430	3	coef_probs_4x4 [1] [1] [4] [2] [0..2]	17, 93, 177	17, 93, 177	0	378											
	433	3	coef_probs_4x4 [1] [1] [4] [3] [0..2]	3, 61, 124	3, 61, 124	0	381											
	436	3	coef_probs_4x4 [1] [1] [4] [4] [0..2]	1, 41, 84	1, 41, 84	0	384											
	439	3	coef_probs_4x4 [1] [1] [4] [5] [0..2]	1, 21, 52	1, 21, 52	0	387											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
	442	3	coef_probs_4x4 [1] [1] [5] [0] [0..2]	157, 78, 244	157, 78, 244	0	390											
	445	3	coef_probs_4x4 [1] [1] [5] [1] [0..2]	140, 72, 231	140, 72, 231	0	393											
	448	3	coef_probs_4x4 [1] [1] [5] [2] [0..2]	69, 58, 184	69, 58, 184	0	396											
	451	3	coef_probs_4x4 [1] [1] [5] [3] [0..2]	31, 44, 137	31, 44, 137	0	399											
	454	3	coef_probs_4x4 [1] [1] [5] [4] [0..2]	14, 38, 105	14, 38, 105	0	402											
	457	3	coef_probs_4x4 [1] [1] [5] [5] [0..2]	8, 23, 61	8, 23, 61	0	405											
	460	3	coef_probs_8x8	125,	12	0	40		57.				0-					

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
			[0] [0] [0] [0] [0..2]	34, 187	5, 34, 187		8		5				287					
	463	3	coef_probs_8x8 [0] [0] [0] [1] [0..2]	52, 41, 133	52, 41, 133	0	411											
	466	3	coef_probs_8x8 [0] [0] [0] [2] [0..2]	6, 31, 56	6, 31, 56	0	414											
	469	3	coef_probs_8x8 [0] [0] [1] [0] [0..2]	37, 109, 153	37, 109, 153	0	417											
	472	3	coef_probs_8x8 [0] [0] [1] [1] [0..2]	51, 102, 147	51, 102, 147	0	420											
	475	3	coef_probs_8x8 [0] [0] [1] [2] [0..2]	23, 87, 128	23, 87, 128	0	423											
	478	3	coef_probs_8x8	8, 67,	8,	0	42											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
			[0] [0] [1] [3] [0..2]	101	67, 101		6											
	481	3	coef_probs_8x8 [0] [0] [1] [4] [0..2]	1, 41, 63	1, 41, 63	0	429											
	484	3	coef_probs_8x8 [0] [0] [1] [5] [0..2]	1, 19, 29	1, 19, 29	0	432											
	487	3	coef_probs_8x8 [0] [0] [2] [0] [0..2]	31, 154, 185	31, 154, 185	0	435											
	490	3	coef_probs_8x8 [0] [0] [2] [1] [0..2]	17, 127, 175	17, 127, 175	0	438											
	493	3	coef_probs_8x8 [0] [0] [2] [2] [0..2]	6, 96, 145	6, 96, 145	0	441											
	496	3	coef_probs_8x8 [0] [0] [2] [3] [0..2]	2, 73, 114	2, 73, 11	0	444											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
					4													
	499	3	coef_probs_8x8 [0] [0] [2] [4] [0..2]	1, 51, 82	1, 51, 82	0	447											
	502	3	coef_probs_8x8 [0] [0] [2] [5] [0..2]	1, 28, 45	1, 28, 45	0	450											
	505	3	coef_probs_8x8 [0] [0] [3] [0] [0..2]	23, 163, 200	23, 163, 200	0	453											
	508	3	coef_probs_8x8 [0] [0] [3] [1] [0..2]	10, 131, 185	10, 131, 185	0	456											
	511	3	coef_probs_8x8 [0] [0] [3] [2] [0..2]	2, 93, 148	2, 93, 148	0	459											
	514	3	coef_probs_8x8 [0] [0] [3] [3] [0..2]	1, 67, 111	1, 67, 111	0	462											
	517	3	coef_probs_8x8	1, 41,	1,	0	46											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
			[0] [0] [3] [4] [0..2]	69	41, 69		5											
	520	3	coef_probs_8x8 [0] [0] [3] [5] [0..2]	1, 14, 24	1, 14, 24	0	468											
	523	3	coef_probs_8x8 [0] [0] [4] [0] [0..2]	29, 176, 217	29, 176, 217	0	471											
	526	3	coef_probs_8x8 [0] [0] [4] [1] [0..2]	12, 145, 201	12, 145, 201	0	474											
	529	3	coef_probs_8x8 [0] [0] [4] [2] [0..2]	3, 101, 156	3, 101, 156	0	477											
	532	3	coef_probs_8x8 [0] [0] [4] [3] [0..2]	1, 69, 111	1, 69, 111	0	480											
	535	3	coef_probs_8x8 [0] [0] [4] [4]	1, 39, 63	1, 39,	0	483											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
			[0..2]		63													
	538	3	coef_probs_8x8 [0] [0] [4] [5] [0..2]	1, 14, 23	1, 14, 23	0	486											
	541	3	coef_probs_8x8 [0] [0] [5] [0] [0..2]	57, 192, 233	57, 192, 233	0	489											
	544	3	coef_probs_8x8 [0] [0] [5] [1] [0..2]	25, 154, 215	25, 154, 215	0	492											
	547	3	coef_probs_8x8 [0] [0] [5] [2] [0..2]	6, 109, 167	6, 109, 167	0	495											
	550	3	coef_probs_8x8 [0] [0] [5] [3] [0..2]	3, 78, 118	3, 78, 118	0	498											
	553	3	coef_probs_8x8 [0] [0] [5] [4] [0..2]	1, 48, 69	1, 48, 69	0	501											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
	556	3	coef_probs_8x8 [0] [0] [5] [5] [0..2]	1, 21, 29	1, 21, 29	0	504											
	559	3	coef_probs_8x8 [0] [1] [0] [0] [0..2]	202, 105, 245	202, 105, 245	0	507											
	562	3	coef_probs_8x8 [0] [1] [0] [1] [0..2]	108, 106, 216	108, 106, 216	0	510											
	565	3	coef_probs_8x8 [0] [1] [0] [2] [0..2]	18, 90, 144	18, 90, 144	0	513											
	568	3	coef_probs_8x8 [0] [1] [1] [0] [0..2]	33, 172, 219	33, 172, 219	0	516											
	571	3	coef_probs_8x8 [0] [1] [1] [1] [0..2]	64, 149, 206	64, 149,	0	519											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
					206													
	574	3	coef_probs_8x8 [0] [1] [1] [2] [0..2]	14, 117, 177	14, 117, 177	0	522											
	577	3	coef_probs_8x8 [0] [1] [1] [3] [0..2]	5, 90, 141	5, 90, 141	0	525											
	580	3	coef_probs_8x8 [0] [1] [1] [4] [0..2]	2, 61, 95	2, 61, 95	0	528											
	583	3	coef_probs_8x8 [0] [1] [1] [5] [0..2]	1, 37, 57	1, 37, 57	0	531											
	586	3	coef_probs_8x8 [0] [1] [2] [0] [0..2]	33, 179, 220	33, 179, 220	0	534											
	589	3	coef_probs_8x8 [0] [1] [2] [1] [0..2]	11, 140, 198	11, 140, 19	0	537											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
					8													
	592	3	coef_probs_8x8 [0] [1] [2] [2] [0..2]	1, 89, 148	1, 89, 148	0	540											
	595	3	coef_probs_8x8 [0] [1] [2] [3] [0..2]	1, 60, 104	1, 60, 104	0	543											
	598	3	coef_probs_8x8 [0] [1] [2] [4] [0..2]	1, 33, 57	1, 33, 57	0	546											
	601	3	coef_probs_8x8 [0] [1] [2] [5] [0..2]	1, 12, 21	1, 12, 21	0	549											
	604	3	coef_probs_8x8 [0] [1] [3] [0] [0..2]	30, 181, 221	30, 181, 221	0	552											
	607	3	coef_probs_8x8 [0] [1] [3] [1] [0..2]	8, 141, 198	8, 141, 198	0	555											
	610	3	coef_probs_8x8	1, 87,	1,	0	55											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
			[0] [1] [3] [2] [0..2]	145	87, 145		8											
	613	3	coef_probs_8x8 [0] [1] [3] [3] [0..2]	1, 58, 100	1, 58, 100	0	561											
	616	3	coef_probs_8x8 [0] [1] [3] [4] [0..2]	1, 31, 55	1, 31, 55	0	564											
	619	3	coef_probs_8x8 [0] [1] [3] [5] [0..2]	1, 12, 20	1, 12, 20	0	567											
	622	3	coef_probs_8x8 [0] [1] [4] [0] [0..2]	32, 186, 224	32, 186, 224	0	570											
	625	3	coef_probs_8x8 [0] [1] [4] [1] [0..2]	7, 142, 198	7, 142, 198	0	573											
	628	3	coef_probs_8x8 [0] [1] [4] [2] [0..2]	1, 86, 143	1, 86, 14	0	576											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
					3													
	631	3	coef_probs_8x8 [0] [1] [4] [3] [0..2]	1, 58, 100	1, 58, 100	0	579											
	634	3	coef_probs_8x8 [0] [1] [4] [4] [0..2]	1, 31, 55	1, 31, 55	0	582											
	637	3	coef_probs_8x8 [0] [1] [4] [5] [0..2]	1, 12, 22	1, 12, 22	0	585											
	640	3	coef_probs_8x8 [0] [1] [5] [0] [0..2]	57, 192, 227	57, 192, 227	0	588											
	643	3	coef_probs_8x8 [0] [1] [5] [1] [0..2]	20, 143, 204	20, 143, 204	0	591											
	646	3	coef_probs_8x8 [0] [1] [5] [2] [0..2]	3, 96, 154	3, 96, 154	0	594											
	649	3	coef_probs_8x8	1, 68,	1,	0	59											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
			[0] [1] [5] [3] [0..2]	112	68, 112		7											
	652	3	coef_probs_8x8 [0] [1] [5] [4] [0..2]	1, 42, 69	1, 42, 69	0	600											
	655	3	coef_probs_8x8 [0] [1] [5] [5] [0..2]	1, 19, 32	1, 19, 32	0	603											
	658	3	coef_probs_8x8 [1] [0] [0] [0] [0..2]	212, 35, 215	212, 35, 215	0	606								0-287			
	661	3	coef_probs_8x8 [1] [0] [0] [1] [0..2]	113, 47, 169	113, 47, 169	0	609											
	664	3	coef_probs_8x8 [1] [0] [0] [2] [0..2]	29, 48, 105	29, 48, 105	0	612											
	667	3	coef_probs_8x8 [1] [0] [1] [0] [0..2]	74, 129, 203	74, 129,	0	615											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
					203													
	670	3	coef_probs_8x8 [1] [0] [1] [1] [0..2]	106, 120, 203	106, 120, 203	0	618											
	673	3	coef_probs_8x8 [1] [0] [1] [2] [0..2]	49, 107, 178	49, 107, 178	0	621											
	676	3	coef_probs_8x8 [1] [0] [1] [3] [0..2]	19, 84, 144	19, 84, 144	0	624											
	679	3	coef_probs_8x8 [1] [0] [1] [4] [0..2]	4, 50, 84	4, 50, 84	0	627											
	682	3	coef_probs_8x8 [1] [0] [1] [5] [0..2]	1, 15, 25	1, 15, 25	0	630											
	685	3	coef_probs_8x8 [1] [0] [2] [0] [0..2]	71, 172, 217	71, 172,	0	633											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
					217													
	688	3	coef_probs_8x8 [1] [0] [2] [1] [0..2]	44, 141, 209	44, 141, 209	0	636											
	691	3	coef_probs_8x8 [1] [0] [2] [2] [0..2]	15, 102, 173	15, 102, 173	0	639											
	694	3	coef_probs_8x8 [1] [0] [2] [3] [0..2]	6, 76, 133	6, 76, 133	0	642											
	697	3	coef_probs_8x8 [1] [0] [2] [4] [0..2]	2, 51, 89	2, 51, 89	0	645											
	700	3	coef_probs_8x8 [1] [0] [2] [5] [0..2]	1, 24, 42	1, 24, 42	0	648											
	703	3	coef_probs_8x8 [1] [0] [3] [0] [0..2]	64, 185, 231	64, 185, 23	0	651											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
					1													
	706	3	coef_probs_8x8 [1] [0] [3] [1] [0..2]	31, 148, 216	31, 148, 216	0	654											
	709	3	coef_probs_8x8 [1] [0] [3] [2] [0..2]	8, 103, 175	8, 103, 175	0	657											
	712	3	coef_probs_8x8 [1] [0] [3] [3] [0..2]	3, 74, 131	3, 74, 131	0	660											
	715	3	coef_probs_8x8 [1] [0] [3] [4] [0..2]	1, 46, 81	1, 46, 81	0	663											
	718	3	coef_probs_8x8 [1] [0] [3] [5] [0..2]	1, 18, 30	1, 18, 30	0	666											
	721	3	coef_probs_8x8 [1] [0] [4] [0] [0..2]	65, 196, 235	65, 196, 235	0	669											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
	724	3	coef_probs_8x8 [1] [0] [4] [1] [0..2]	25, 157, 221	25, 157, 221	0	672											
	727	3	coef_probs_8x8 [1] [0] [4] [2] [0..2]	5, 105, 174	5, 105, 174	0	675											
	730	3	coef_probs_8x8 [1] [0] [4] [3] [0..2]	1, 67, 120	1, 67, 120	0	678											
	733	3	coef_probs_8x8 [1] [0] [4] [4] [0..2]	1, 38, 69	1, 38, 69	0	681											
	736	3	coef_probs_8x8 [1] [0] [4] [5] [0..2]	1, 15, 30	1, 15, 30	0	684											
	739	3	coef_probs_8x8 [1] [0] [5] [0] [0..2]	65, 204, 238	65, 204, 238	0	687											
	742	3	coef_probs_8x8	30,	30,	0	69											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
			[1] [0] [5] [1] [0..2]	156, 224	156, 224		0											
	745	3	coef_probs_8x8 [1] [0] [5] [2] [0..2]	7, 107, 177	7, 107, 177	0	693											
	748	3	coef_probs_8x8 [1] [0] [5] [3] [0..2]	2, 70, 124	2, 70, 124	0	696											
	751	3	coef_probs_8x8 [1] [0] [5] [4] [0..2]	1, 42, 73	1, 42, 73	0	699											
	754	3	coef_probs_8x8 [1] [0] [5] [5] [0..2]	1, 18, 34	1, 18, 34	0	702											
	757	3	coef_probs_8x8 [1] [1] [0] [0] [0..2]	225, 86, 251	225, 86, 251	0	705											
	760	3	coef_probs_8x8 [1] [1] [0] [1]	144, 104,	144,	0	708											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
			[0..2]	235	104, 235													
	763	3	coef_probs_8x8 [1] [1] [0] [2] [0..2]	42, 99, 181	42, 99, 181	0	711											
	766	3	coef_probs_8x8 [1] [1] [1] [0] [0..2]	85, 175, 239	85, 175, 239	0	714											
	769	3	coef_probs_8x8 [1] [1] [1] [1] [0..2]	112, 165, 229	112, 165, 229	0	717											
	772	3	coef_probs_8x8 [1] [1] [1] [2] [0..2]	29, 136, 200	29, 136, 200	0	720											
	775	3	coef_probs_8x8 [1] [1] [1] [3] [0..2]	12, 103, 162	12, 103,	0	723											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
					162													
	778	3	coef_probs_8x8 [1] [1] [1] [4] [0..2]	6, 77, 123	6, 77, 123	0	726											
	781	3	coef_probs_8x8 [1] [1] [1] [5] [0..2]	2, 53, 84	2, 53, 84	0	729											
	784	3	coef_probs_8x8 [1] [1] [2] [0] [0..2]	75, 183, 239	75, 183, 239	0	732											
	787	3	coef_probs_8x8 [1] [1] [2] [1] [0..2]	30, 155, 221	30, 155, 221	0	735											
	790	3	coef_probs_8x8 [1] [1] [2] [2] [0..2]	3, 106, 171	3, 106, 171	0	738											
	793	3	coef_probs_8x8 [1] [1] [2] [3]	1, 74, 128	1, 74,	0	741											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
			[0..2]		128													
	796	3	coef_probs_8x8 [1] [1] [2] [4] [0..2]	1, 44, 76	1, 44, 76	0	744											
	799	3	coef_probs_8x8 [1] [1] [2] [5] [0..2]	1, 17, 28	1, 17, 28	0	747											
	802	3	coef_probs_8x8 [1] [1] [3] [0] [0..2]	73, 185, 240	73, 185, 240	0	750											
	805	3	coef_probs_8x8 [1] [1] [3] [1] [0..2]	27, 159, 222	27, 159, 222	0	753											
	808	3	coef_probs_8x8 [1] [1] [3] [2] [0..2]	2, 107, 172	2, 107, 172	0	756											
	811	3	coef_probs_8x8 [1] [1] [3] [3] [0..2]	1, 75, 127	1, 75, 12	0	759											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
					7													
	814	3	coef_probs_8x8 [1] [1] [3] [4] [0..2]	1, 42, 73	1, 42, 73	0	762											
	817	3	coef_probs_8x8 [1] [1] [3] [5] [0..2]	1, 17, 29	1, 17, 29	0	765											
	820	3	coef_probs_8x8 [1] [1] [4] [0] [0..2]	62, 190, 238	62, 190, 238	0	768											
	823	3	coef_probs_8x8 [1] [1] [4] [1] [0..2]	21, 159, 222	21, 159, 222	0	771											
	826	3	coef_probs_8x8 [1] [1] [4] [2] [0..2]	2, 107, 172	2, 107, 172	0	774											
	829	3	coef_probs_8x8 [1] [1] [4] [3] [0..2]	1, 72, 122	1, 72, 122	0	777											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
	832	3	coef_probs_8x8 [1] [1] [4] [4] [0..2]	1, 40, 71	1, 40, 71	0	780											
	835	3	coef_probs_8x8 [1] [1] [4] [5] [0..2]	1, 18, 32	1, 18, 32	0	783											
	838	3	coef_probs_8x8 [1] [1] [5] [0] [0..2]	61, 199, 240	61, 199, 240	0	786											
	841	3	coef_probs_8x8 [1] [1] [5] [1] [0..2]	27, 161, 226	27, 161, 226	0	789											
	844	3	coef_probs_8x8 [1] [1] [5] [2] [0..2]	4, 113, 180	4, 113, 180	0	792											
	847	3	coef_probs_8x8 [1] [1] [5] [3] [0..2]	1, 76, 129	1, 76, 129	0	795											
	850	3	coef_probs_8x8	1, 46,	1,	0	79											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
			[1] [1] [5] [4] [0..2]	80	46, 80		8											
	853	3	coef_probs_8x8 [1] [1] [5] [5] [0..2]	1, 23, 41	1, 23, 41	0	801											
	856	3	coef_probs_16x16 [0] [0] [0] [0] [0..2]	7, 27, 153	7, 27, 153	0	804		107						0-287			
	859	3	coef_probs_16x16 [0] [0] [0] [1] [0..2]	5, 30, 95	5, 30, 95	0	807											
	862	3	coef_probs_16x16 [0] [0] [0] [2] [0..2]	1, 16, 30	1, 16, 30	0	810											
	865	3	coef_probs_16x16 [0] [0] [1] [0] [0..2]	50, 75, 127	50, 75, 127	0	813											
	868	3	coef_probs_16x16 [0] [0] [1] [1] [0..2]	57, 75, 124	57, 75, 124	0	816											
	871	3	coef_probs_16x1	27, 67,	27,	0	81											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults			Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
										4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
			6 [0] [0] [1] [2] [0..2]	108	67, 108		9											
	874	3	coef_probs_16x16 [0] [0] [1] [3] [0..2]	10, 54, 86	10, 54, 86	0	822											
	877	3	coef_probs_16x16 [0] [0] [1] [4] [0..2]	1, 33, 52	1, 33, 52	0	825											
	880	3	coef_probs_16x16 [0] [0] [1] [5] [0..2]	1, 12, 18	1, 12, 18	0	828											
	883	3	coef_probs_16x16 [0] [0] [2] [0] [0..2]	43, 125, 151	43, 125, 151	0	831											
	886	3	coef_probs_16x16 [0] [0] [2] [1] [0..2]	26, 108, 148	26, 108, 148	0	834											
	889	3	coef_probs_16x1	7, 83,	7,	0	83											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
			6 [0] [0] [2] [2] [0..2]	122	83, 122		7											
	892	3	coef_probs_16x16 [0] [0] [2] [3] [0..2]	2, 59, 89	2, 59, 89	0	840											
	895	3	coef_probs_16x16 [0] [0] [2] [4] [0..2]	1, 38, 60	1, 38, 60	0	843											
	898	3	coef_probs_16x16 [0] [0] [2] [5] [0..2]	1, 17, 27	1, 17, 27	0	846											
	901	3	coef_probs_16x16 [0] [0] [3] [0] [0..2]	23, 144, 163	23, 144, 163	0	849											
	904	3	coef_probs_16x16 [0] [0] [3] [1] [0..2]	13, 112, 154	13, 112, 154	0	852											
	907	3	coef_probs_16x1	2, 75,	2,	0	85											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
			6 [0] [0] [3] [2] [0..2]	117	75, 117		5											
	910	3	coef_probs_16x16 [0] [0] [3] [3] [0..2]	1, 50, 81	1, 50, 81	0	858											
	913	3	coef_probs_16x16 [0] [0] [3] [4] [0..2]	1, 31, 51	1, 31, 51	0	861											
	916	3	coef_probs_16x16 [0] [0] [3] [5] [0..2]	1, 14, 23	1, 14, 23	0	864											
	919	3	coef_probs_16x16 [0] [0] [4] [0] [0..2]	18, 162, 185	18, 162, 185	0	867											
	922	3	coef_probs_16x16 [0] [0] [4] [1] [0..2]	6, 123, 171	6, 123, 171	0	870											
	925	3	coef_probs_16x1	1, 78,	1,	0	87											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
			6 [0] [0] [4] [2] [0..2]	125	78, 125		3											
	928	3	coef_probs_16x16 [0] [0] [4] [3] [0..2]	1, 51, 86	1, 51, 86	0	876											
	931	3	coef_probs_16x16 [0] [0] [4] [4] [0..2]	1, 31, 54	1, 31, 54	0	879											
	934	3	coef_probs_16x16 [0] [0] [4] [5] [0..2]	1, 14, 23	1, 14, 23	0	882											
	937	3	coef_probs_16x16 [0] [0] [5] [0] [0..2]	15, 199, 227	15, 199, 227	0	885											
	940	3	coef_probs_16x16 [0] [0] [5] [1] [0..2]	3, 150, 204	3, 150, 204	0	888											
	943	3	coef_probs_16x1	1, 91,	1,	0	89											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
			6 [0] [0] [5] [2] [0..2]	146	91, 146		1											
	946	3	coef_probs_16x16 [0] [0] [5] [3] [0..2]	1, 55, 95	1, 55, 95	0	894											
	949	3	coef_probs_16x16 [0] [0] [5] [4] [0..2]	1, 30, 53	1, 30, 53	0	897											
	952	3	coef_probs_16x16 [0] [0] [5] [5] [0..2]	1, 11, 20	1, 11, 20	0	900											
	955	3	coef_probs_16x16 [0] [1] [0] [0] [0..2]	19, 55, 240	19, 55, 240	0	903											
	958	3	coef_probs_16x16 [0] [1] [0] [1] [0..2]	19, 59, 196	19, 59, 196	0	906											
	961	3	coef_probs_16x16 [0] [1] [0] [2]	3, 52, 105	3, 52, 10	0	909											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
			[0..2]		5													
	964	3	coef_probs_16x16 [0] [1] [1] [0] [0..2]	41, 166, 207	41, 166, 207	0	912											
	967	3	coef_probs_16x16 [0] [1] [1] [1] [0..2]	104, 153, 199	104, 153, 199	0	915											
	970	3	coef_probs_16x16 [0] [1] [1] [2] [0..2]	31, 123, 181	31, 123, 181	0	918											
	973	3	coef_probs_16x16 [0] [1] [1] [3] [0..2]	14, 101, 152	14, 101, 152	0	921											
	976	3	coef_probs_16x16 [0] [1] [1] [4] [0..2]	5, 72, 106	5, 72, 106	0	924											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
	979	3	coef_probs_16x16 [0] [1] [1] [5] [0..2]	1, 36, 52	1, 36, 52	0	927											
	982	3	coef_probs_16x16 [0] [1] [2] [0] [0..2]	35, 176, 211	35, 176, 211	0	930											
	985	3	coef_probs_16x16 [0] [1] [2] [1] [0..2]	12, 131, 190	12, 131, 190	0	933											
	988	3	coef_probs_16x16 [0] [1] [2] [2] [0..2]	2, 88, 144	2, 88, 144	0	936											
	991	3	coef_probs_16x16 [0] [1] [2] [3] [0..2]	1, 60, 101	1, 60, 101	0	939											
	994	3	coef_probs_16x16 [0] [1] [2] [4] [0..2]	1, 36, 60	1, 36, 60	0	942											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
	997	3	coef_probs_16x16 [0] [1] [2] [5] [0..2]	1, 16, 28	1, 16, 28	0	945											
	1000	3	coef_probs_16x16 [0] [1] [3] [0] [0..2]	28, 183, 213	28, 183, 213	0	948											
	1003	3	coef_probs_16x16 [0] [1] [3] [1] [0..2]	8, 134, 191	8, 134, 191	0	951											
	1006	3	coef_probs_16x16 [0] [1] [3] [2] [0..2]	1, 86, 142	1, 86, 142	0	954											
	1009	3	coef_probs_16x16 [0] [1] [3] [3] [0..2]	1, 56, 96	1, 56, 96	0	957											
	1012	3	coef_probs_16x16 [0] [1] [3] [4] [0..2]	1, 30, 53	1, 30, 53	0	960											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults					Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
												4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
	1015	3	coef_probs_16x16 [0] [1] [3] [5] [0..2]	1, 12, 20	1, 12, 20	0	963												
	1018	3	coef_probs_16x16 [0] [1] [4] [0] [0..2]	20, 190, 215	20, 190, 215	0	966												
	1021	3	coef_probs_16x16 [0] [1] [4] [1] [0..2]	4, 135, 192	4, 135, 192	0	969												
	1024	3	coef_probs_16x16 [0] [1] [4] [2] [0..2]	1, 84, 139	1, 84, 139	0	972												
	1027	3	coef_probs_16x16 [0] [1] [4] [3] [0..2]	1, 53, 91	1, 53, 91	0	975												
	1030	3	coef_probs_16x16 [0] [1] [4] [4] [0..2]	1, 28, 49	1, 28, 49	0	978												

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
	1033	3	coef_probs_16x16 [0] [1] [4] [5] [0..2]	1, 11, 20	1, 11, 20	0	981											
	1036	3	coef_probs_16x16 [0] [1] [5] [0] [0..2]	13, 196, 216	13, 196, 216	0	984											
	1039	3	coef_probs_16x16 [0] [1] [5] [1] [0..2]	2, 137, 192	2, 137, 192	0	987											
	1042	3	coef_probs_16x16 [0] [1] [5] [2] [0..2]	1, 86, 143	1, 86, 143	0	990											
	1045	3	coef_probs_16x16 [0] [1] [5] [3] [0..2]	1, 57, 99	1, 57, 99	0	993											
	1048	3	coef_probs_16x16 [0] [1] [5] [4] [0..2]	1, 32, 56	1, 32, 56	0	996											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
	1051	3	coef_probs_16x16 [0] [1] [5] [5] [0..2]	1, 13, 24	1, 13, 24	0	999											
	1054	3	coef_probs_16x16 [1] [0] [0] [0] [0..2]	211, 29, 217	211, 29, 217	0	1002										0-287	
	1057	3	coef_probs_16x16 [1] [0] [0] [1] [0..2]	96, 47, 156	96, 47, 156	0	1005											
	1060	3	coef_probs_16x16 [1] [0] [0] [2] [0..2]	22, 43, 87	22, 43, 87	0	1008											
	1063	3	coef_probs_16x16 [1] [0] [1] [0] [0..2]	78, 120, 193	78, 120, 193	0	1011											
	1066	3	coef_probs_16x16 [1] [0] [1] [1] [0..2]	111, 116, 186	111, 116, 18	0	1014											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
					6													
	1069	3	coef_probs_16x16 [1] [0] [1] [2] [0..2]	46, 102, 164	46, 102, 164	0	1017											
	1072	3	coef_probs_16x16 [1] [0] [1] [3] [0..2]	15, 80, 128	15, 80, 128	0	1020											
	1075	3	coef_probs_16x16 [1] [0] [1] [4] [0..2]	2, 49, 76	2, 49, 76	0	1023											
	1078	3	coef_probs_16x16 [1] [0] [1] [5] [0..2]	1, 18, 28	1, 18, 28	0	1026											
	1081	3	coef_probs_16x16 [1] [0] [2] [0] [0..2]	71, 161, 203	71, 161, 203	0	1029											
	1084	3	coef_probs_16x16 [1] [0] [2] [1]	42, 132, 192	42, 132,	0	1032											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
			[0..2]		192													
	1087	3	coef_probs_16x16 [1] [0] [2] [2] [0..2]	10, 98, 150	10, 98, 150	0	1035											
	1090	3	coef_probs_16x16 [1] [0] [2] [3] [0..2]	3, 69, 109	3, 69, 109	0	1038											
	1093	3	coef_probs_16x16 [1] [0] [2] [4] [0..2]	1, 44, 70	1, 44, 70	0	1041											
	1096	3	coef_probs_16x16 [1] [0] [2] [5] [0..2]	1, 18, 29	1, 18, 29	0	1044											
	1099	3	coef_probs_16x16 [1] [0] [3] [0] [0..2]	57, 186, 211	57, 186, 211	0	1047											
	1102	3	coef_probs_16x16 [1] [0] [3] [1]	30, 140, 196	30, 140,	0	1050											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
			[0..2]		196													
	1105	3	coef_probs_16x16 [1] [0] [3] [2] [0..2]	4, 93, 146	4, 93, 146	0	1053											
	1108	3	coef_probs_16x16 [1] [0] [3] [3] [0..2]	1, 62, 102	1, 62, 102	0	1056											
	1111	3	coef_probs_16x16 [1] [0] [3] [4] [0..2]	1, 38, 65	1, 38, 65	0	1059											
	1114	3	coef_probs_16x16 [1] [0] [3] [5] [0..2]	1, 16, 27	1, 16, 27	0	1062											
	1117	3	coef_probs_16x16 [1] [0] [4] [0] [0..2]	47, 199, 217	47, 199, 217	0	1065											
	1120	3	coef_probs_16x16 [1] [0] [4] [1]	14, 145, 196	14, 145,	0	1068											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
			[0..2]		196													
	1123	3	coef_probs_16x16 [1] [0] [4] [2] [0..2]	1, 88, 142	1, 88, 142	0	1071											
	1126	3	coef_probs_16x16 [1] [0] [4] [3] [0..2]	1, 57, 98	1, 57, 98	0	1074											
	1129	3	coef_probs_16x16 [1] [0] [4] [4] [0..2]	1, 36, 62	1, 36, 62	0	1077											
	1132	3	coef_probs_16x16 [1] [0] [4] [5] [0..2]	1, 15, 26	1, 15, 26	0	1080											
	1135	3	coef_probs_16x16 [1] [0] [5] [0] [0..2]	26, 219, 229	26, 219, 229	0	1083											
	1138	3	coef_probs_16x16 [1] [0] [5] [1]	5, 155, 207	5, 155,	0	1086											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
			[0..2]		207													
	1141	3	coef_probs_16x16 [1] [0] [5] [2] [0..2]	1, 94, 151	1, 94, 151	0	1089											
	1144	3	coef_probs_16x16 [1] [0] [5] [3] [0..2]	1, 60, 104	1, 60, 104	0	1092											
	1147	3	coef_probs_16x16 [1] [0] [5] [4] [0..2]	1, 36, 62	1, 36, 62	0	1095											
	1150	3	coef_probs_16x16 [1] [0] [5] [5] [0..2]	1, 16, 28	1, 16, 28	0	1098											
	1153	3	coef_probs_16x16 [1] [1] [0] [0] [0..2]	233, 29, 248	233, 29, 248	0	1101											
	1156	3	coef_probs_16x16 [1] [1] [0] [1]	146, 47, 220	146, 47,	0	1104											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
			[0..2]		220													
	1159	3	coef_probs_16x16 [1] [1] [0] [2] [0..2]	43, 52, 140	43, 52, 140	0	1107											
	1162	3	coef_probs_16x16 [1] [1] [1] [0] [0..2]	100, 163, 232	100, 163, 232	0	1110											
	1165	3	coef_probs_16x16 [1] [1] [1] [1] [0..2]	179, 161, 222	179, 161, 222	0	1113											
	1168	3	coef_probs_16x16 [1] [1] [1] [2] [0..2]	63, 142, 204	63, 142, 204	0	1116											
	1171	3	coef_probs_16x16 [1] [1] [1] [3] [0..2]	37, 113, 174	37, 113, 17	0	1119											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
					4													
	1174	3	coef_probs_16x16 [1] [1] [1] [4] [0..2]	26, 89, 137	26, 89, 137	0	1122											
	1177	3	coef_probs_16x16 [1] [1] [1] [5] [0..2]	18, 68, 97	18, 68, 97	0	1125											
	1180	3	coef_probs_16x16 [1] [1] [2] [0] [0..2]	85, 181, 230	85, 181, 230	0	1128											
	1183	3	coef_probs_16x16 [1] [1] [2] [1] [0..2]	32, 146, 209	32, 146, 209	0	1131											
	1186	3	coef_probs_16x16 [1] [1] [2] [2] [0..2]	7, 100, 164	7, 100, 164	0	1134											
	1189	3	coef_probs_16x16	3, 71, 121	3, 71,	0	1137											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
			[1] [1] [2] [3] [0..2]		121													
	1192	3	coef_probs_16x16 [1] [1] [2] [4] [0..2]	1, 45, 77	1, 45, 77	0	1140											
	1195	3	coef_probs_16x16 [1] [1] [2] [5] [0..2]	1, 18, 30	1, 18, 30	0	1143											
	1198	3	coef_probs_16x16 [1] [1] [3] [0] [0..2]	65, 187, 230	65, 187, 230	0	1146											
	1201	3	coef_probs_16x16 [1] [1] [3] [1] [0..2]	20, 148, 207	20, 148, 207	0	1149											
	1204	3	coef_probs_16x16 [1] [1] [3] [2] [0..2]	2, 97, 159	2, 97, 159	0	1152											
	1207	3	coef_probs_16x16	1, 68, 116	1, 68,	0	1155											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
			[1] [1] [3] [3] [0..2]		116													
	1210	3	coef_probs_16x16 [1] [1] [3] [4] [0..2]	1, 40, 70	1, 40, 70	0	1158											
	1213	3	coef_probs_16x16 [1] [1] [3] [5] [0..2]	1, 14, 29	1, 14, 29	0	1161											
	1216	3	coef_probs_16x16 [1] [1] [4] [0] [0..2]	40, 194, 227	40, 194, 227	0	1164											
	1219	3	coef_probs_16x16 [1] [1] [4] [1] [0..2]	8, 147, 204	8, 147, 204	0	1167											
	1222	3	coef_probs_16x16 [1] [1] [4] [2] [0..2]	1, 94, 155	1, 94, 155	0	1170											
	1225	3	coef_probs_16x16	1, 65, 112	1, 65,	0	1173											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
			[1] [1] [4] [3] [0..2]		112													
	1228	3	coef_probs_16x16 [1] [1] [4] [4] [0..2]	1, 39, 66	1, 39, 66	0	1176											
	1231	3	coef_probs_16x16 [1] [1] [4] [5] [0..2]	1, 14, 26	1, 14, 26	0	1179											
	1234	3	coef_probs_16x16 [1] [1] [5] [0] [0..2]	16, 208, 228	16, 208, 228	0	1182											
	1237	3	coef_probs_16x16 [1] [1] [5] [1] [0..2]	3, 151, 207	3, 151, 207	0	1185											
	1240	3	coef_probs_16x16 [1] [1] [5] [2] [0..2]	1, 98, 160	1, 98, 160	0	1188											
	1243	3	coef_probs_16x16	1, 67, 117	1, 67,	0	1191											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT		State counter EBB Address	Coefficient counter EBB Address							
												4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
			[1] [1] [5] [3] [0..2]		117														
	1246	3	coef_probs_16x16 [1] [1] [5] [4] [0..2]	1, 41, 74	1, 41, 74	0	1194												
	1249	3	coef_probs_16x16 [1] [1] [5] [5] [0..2]	1, 17, 31	1, 17, 31	0	1197												
	1252	3	coef_probs_32x32 [0] [0] [0] [0] [0..2]	17, 38, 140	17, 38, 140	0	1200		156.5									0-287	
	1255	3	coef_probs_32x32 [0] [0] [0] [1] [0..2]	7, 34, 80	7, 34, 80	0	1203												
	1258	3	coef_probs_32x32 [0] [0] [0] [2] [0..2]	1, 17, 29	1, 17, 29	0	1206												
	1261	3	coef_probs_32x32 [0] [0] [1] [0] [0..2]	37, 75, 128	37, 75, 128	0	1209												

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
	1264	3	coef_probs_32x32 [0] [0] [1] [1] [0..2]	41, 76, 128	41, 76, 128	0	1212											
	1267	3	coef_probs_32x32 [0] [0] [1] [2] [0..2]	26, 66, 116	26, 66, 116	0	1215											
	1270	3	coef_probs_32x32 [0] [0] [1] [3] [0..2]	12, 52, 94	12, 52, 94	0	1218											
	1273	3	coef_probs_32x32 [0] [0] [1] [4] [0..2]	2, 32, 55	2, 32, 55	0	1221											
	1276	3	coef_probs_32x32 [0] [0] [1] [5] [0..2]	1, 10, 16	1, 10, 16	0	1224											
	1279	3	coef_probs_32x32 [0] [0] [2] [0] [0..2]	50, 127, 154	50, 127, 154	0	1227											
	128	3	coef_probs_32x3	37,	37,	0	12											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
	2		2 [0] [0] [2] [1] [0..2]	109, 152	109, 152		30											
	1285	3	coef_probs_32x32 [0] [0] [2] [2] [0..2]	16, 82, 121	16, 82, 121	0	1233											
	1288	3	coef_probs_32x32 [0] [0] [2] [3] [0..2]	5, 59, 85	5, 59, 85	0	1236											
	1291	3	coef_probs_32x32 [0] [0] [2] [4] [0..2]	1, 35, 54	1, 35, 54	0	1239											
	1294	3	coef_probs_32x32 [0] [0] [2] [5] [0..2]	1, 13, 20	1, 13, 20	0	1242											
	1297	3	coef_probs_32x32 [0] [0] [3] [0] [0..2]	40, 142, 167	40, 142, 167	0	1245											
	130	3	coef_probs_32x3	17,	17,	0	12											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
	0		2 [0] [0] [3] [1] [0..2]	110, 157	110, 157		48											
	1303	3	coef_probs_32x32 [0] [0] [3] [2] [0..2]	2, 71, 112	2, 71, 112	0	1251											
	1306	3	coef_probs_32x32 [0] [0] [3] [3] [0..2]	1, 44, 72	1, 44, 72	0	1254											
	1309	3	coef_probs_32x32 [0] [0] [3] [4] [0..2]	1, 27, 45	1, 27, 45	0	1257											
	1312	3	coef_probs_32x32 [0] [0] [3] [5] [0..2]	1, 11, 17	1, 11, 17	0	1260											
	1315	3	coef_probs_32x32 [0] [0] [4] [0] [0..2]	30, 175, 188	30, 175, 188	0	1263											
	131	3	coef_probs_32x3	9, 124,	9,	0	12											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
	8		2 [0] [0] [4] [1] [0..2]	169	124, 169		66											
	1321	3	coef_probs_32x32 [0] [0] [4] [2] [0..2]	1, 74, 116	1, 74, 116	0	1269											
	1324	3	coef_probs_32x32 [0] [0] [4] [3] [0..2]	1, 48, 78	1, 48, 78	0	1272											
	1327	3	coef_probs_32x32 [0] [0] [4] [4] [0..2]	1, 30, 49	1, 30, 49	0	1275											
	1330	3	coef_probs_32x32 [0] [0] [4] [5] [0..2]	1, 11, 18	1, 11, 18	0	1278											
	1333	3	coef_probs_32x32 [0] [0] [5] [0] [0..2]	10, 222, 223	10, 222, 223	0	1281											
	133	3	coef_probs_32x3	2, 150,	2,	0	12											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
	6		2 [0] [0] [5] [1] [0..2]	194	150, 194		84											
	1339	3	coef_probs_32x32 [0] [0] [5] [2] [0..2]	1, 83, 128	1, 83, 128	0	1287											
	1342	3	coef_probs_32x32 [0] [0] [5] [3] [0..2]	1, 48, 79	1, 48, 79	0	1290											
	1345	3	coef_probs_32x32 [0] [0] [5] [4] [0..2]	1, 27, 45	1, 27, 45	0	1293											
	1348	3	coef_probs_32x32 [0] [0] [5] [5] [0..2]	1, 11, 17	1, 11, 17	0	1296											
	1351	3	coef_probs_32x32 [0] [1] [0] [0] [0..2]	36, 41, 235	36, 41, 235	0	1299											
	1354	3	coef_probs_32x32	29, 36, 193	29, 36,	0	1302											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
			[0] [1] [0] [1] [0..2]		193													
	1357	3	coef_probs_32x32 [0] [1] [0] [2] [0..2]	10, 27, 111	10, 27, 111	0	1305											
	1360	3	coef_probs_32x32 [0] [1] [1] [0] [0..2]	85, 165, 222	85, 165, 222	0	1308											
	1363	3	coef_probs_32x32 [0] [1] [1] [1] [0..2]	177, 162, 215	177, 162, 215	0	1311											
	1366	3	coef_probs_32x32 [0] [1] [1] [2] [0..2]	110, 135, 195	110, 135, 195	0	1314											
	1369	3	coef_probs_32x32 [0] [1] [1] [3] [0..2]	57, 113, 168	57, 113, 16	0	1317											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
					8													
	1372	3	coef_probs_32x32 [0] [1] [1] [4] [0..2]	23, 83, 120	23, 83, 120	0	1320											
	1375	3	coef_probs_32x32 [0] [1] [1] [5] [0..2]	10, 49, 61	10, 49, 61	0	1323											
	1378	3	coef_probs_32x32 [0] [1] [2] [0] [0..2]	85, 190, 223	85, 190, 223	0	1326											
	1381	3	coef_probs_32x32 [0] [1] [2] [1] [0..2]	36, 139, 200	36, 139, 200	0	1329											
	1384	3	coef_probs_32x32 [0] [1] [2] [2] [0..2]	5, 90, 146	5, 90, 146	0	1332											
	1387	3	coef_probs_32x32 [0] [1] [2] [3]	1, 60, 103	1, 60, 10	0	1335											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
			[0..2]		3													
	1390	3	coef_probs_32x32 [0] [1] [2] [4] [0..2]	1, 38, 65	1, 38, 65	0	1338											
	1393	3	coef_probs_32x32 [0] [1] [2] [5] [0..2]	1, 18, 30	1, 18, 30	0	1341											
	1396	3	coef_probs_32x32 [0] [1] [3] [0] [0..2]	72, 202, 223	72, 202, 223	0	1344											
	1399	3	coef_probs_32x32 [0] [1] [3] [1] [0..2]	23, 141, 199	23, 141, 199	0	1347											
	1402	3	coef_probs_32x32 [0] [1] [3] [2] [0..2]	2, 86, 140	2, 86, 140	0	1350											
	1405	3	coef_probs_32x32 [0] [1] [3] [3]	1, 56, 97	1, 56, 97	0	1353											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
			[0..2]															
	1408	3	coef_probs_32x32 [0] [1] [3] [4] [0..2]	1, 36, 61	1, 36, 61	0	1356											
	1411	3	coef_probs_32x32 [0] [1] [3] [5] [0..2]	1, 16, 27	1, 16, 27	0	1359											
	1414	3	coef_probs_32x32 [0] [1] [4] [0] [0..2]	55, 218, 225	55, 218, 225	0	1362											
	1417	3	coef_probs_32x32 [0] [1] [4] [1] [0..2]	13, 145, 200	13, 145, 200	0	1365											
	1420	3	coef_probs_32x32 [0] [1] [4] [2] [0..2]	1, 86, 141	1, 86, 141	0	1368											
	1423	3	coef_probs_32x32 [0] [1] [4] [3]	1, 57, 99	1, 57, 99	0	1371											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
			[0..2]															
	1426	3	coef_probs_32x32 [0] [1] [4] [4] [0..2]	1, 35, 61	1, 35, 61	0	1374											
	1429	3	coef_probs_32x32 [0] [1] [4] [5] [0..2]	1, 13, 22	1, 13, 22	0	1377											
	1432	3	coef_probs_32x32 [0] [1] [5] [0] [0..2]	15, 235, 212	15, 235, 212	0	1380											
	1435	3	coef_probs_32x32 [0] [1] [5] [1] [0..2]	1, 132, 184	1, 132, 184	0	1383											
	1438	3	coef_probs_32x32 [0] [1] [5] [2] [0..2]	1, 84, 139	1, 84, 139	0	1386											
	1441	3	coef_probs_32x32 [0] [1] [5] [3]	1, 57, 97	1, 57, 97	0	1389											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
			[0..2]															
	1444	3	coef_probs_32x32 [0] [1] [5] [4] [0..2]	1, 34, 56	1, 34, 56	0	1392											
	1447	3	coef_probs_32x32 [0] [1] [5] [5] [0..2]	1, 14, 23	1, 14, 23	0	1395											
	1450	3	coef_probs_32x32 [1] [0] [0] [0] [0..2]	181, 21, 201	181, 21, 201	0	1398											0-287
	1453	3	coef_probs_32x32 [1] [0] [0] [1] [0..2]	61, 37, 123	61, 37, 123	0	1401											
	1456	3	coef_probs_32x32 [1] [0] [0] [2] [0..2]	10, 38, 71	10, 38, 71	0	1404											
	1459	3	coef_probs_32x32 [1] [0] [1] [0] [0..2]	47, 106, 172	47, 106, 17	0	1407											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
					2													
	1462	3	coef_probs_32x32 [1] [0] [1] [1] [0..2]	95, 104, 173	95, 104, 173	0	1410											
	1465	3	coef_probs_32x32 [1] [0] [1] [2] [0..2]	42, 93, 159	42, 93, 159	0	1413											
	1468	3	coef_probs_32x32 [1] [0] [1] [3] [0..2]	18, 77, 131	18, 77, 131	0	1416											
	1471	3	coef_probs_32x32 [1] [0] [1] [4] [0..2]	4, 50, 81	4, 50, 81	0	1419											
	1474	3	coef_probs_32x32 [1] [0] [1] [5] [0..2]	1, 17, 23	1, 17, 23	0	1422											
	1477	3	coef_probs_32x32 [1] [0] [2] [0] [0..2]	62, 147, 199	62, 147, 19	0	1425											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
					9													
	1480	3	coef_probs_32x32 [1] [0] [2] [1] [0..2]	44, 130, 189	44, 130, 189	0	1428											
	1483	3	coef_probs_32x32 [1] [0] [2] [2] [0..2]	28, 102, 154	28, 102, 154	0	1431											
	1486	3	coef_probs_32x32 [1] [0] [2] [3] [0..2]	18, 75, 115	18, 75, 115	0	1434											
	1489	3	coef_probs_32x32 [1] [0] [2] [4] [0..2]	2, 44, 65	2, 44, 65	0	1437											
	1492	3	coef_probs_32x32 [1] [0] [2] [5] [0..2]	1, 12, 19	1, 12, 19	0	1440											
	1495	3	coef_probs_32x32 [1] [0] [3] [0]	55, 153, 210	55, 153,	0	1443											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
			[0..2]		210													
	1498	3	coef_probs_32x32 [1] [0] [3] [1] [0..2]	24, 130, 194	24, 130, 194	0	1446											
	1501	3	coef_probs_32x32 [1] [0] [3] [2] [0..2]	3, 93, 146	3, 93, 146	0	1449											
	1504	3	coef_probs_32x32 [1] [0] [3] [3] [0..2]	1, 61, 97	1, 61, 97	0	1452											
	1507	3	coef_probs_32x32 [1] [0] [3] [4] [0..2]	1, 31, 50	1, 31, 50	0	1455											
	1510	3	coef_probs_32x32 [1] [0] [3] [5] [0..2]	1, 10, 16	1, 10, 16	0	1458											
	1513	3	coef_probs_32x32 [1] [0] [4] [0]	49, 186, 223	49, 186,	0	1461											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
			[0..2]		223													
	1516	3	coef_probs_32x32 [1] [0] [4] [1] [0..2]	17, 148, 204	17, 148, 204	0	1464											
	1519	3	coef_probs_32x32 [1] [0] [4] [2] [0..2]	1, 96, 142	1, 96, 142	0	1467											
	1522	3	coef_probs_32x32 [1] [0] [4] [3] [0..2]	1, 53, 83	1, 53, 83	0	1470											
	1525	3	coef_probs_32x32 [1] [0] [4] [4] [0..2]	1, 26, 44	1, 26, 44	0	1473											
	1528	3	coef_probs_32x32 [1] [0] [4] [5] [0..2]	1, 11, 17	1, 11, 17	0	1476											
	1531	3	coef_probs_32x32 [1] [0] [5] [0]	13, 217, 212	13, 217,	0	1479											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
			[0..2]		212													
	1534	3	coef_probs_32x32 [1] [0] [5] [1] [0..2]	2, 136, 180	2, 136, 180	0	1482											
	1537	3	coef_probs_32x32 [1] [0] [5] [2] [0..2]	1, 78, 124	1, 78, 124	0	1485											
	1540	3	coef_probs_32x32 [1] [0] [5] [3] [0..2]	1, 50, 83	1, 50, 83	0	1488											
	1543	3	coef_probs_32x32 [1] [0] [5] [4] [0..2]	1, 29, 49	1, 29, 49	0	1491											
	1546	3	coef_probs_32x32 [1] [0] [5] [5] [0..2]	1, 14, 23	1, 14, 23	0	1494											
	1549	3	coef_probs_32x32 [1] [1] [0] [0]	197, 13, 247	197, 13,	0	1497											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
			[0..2]		247													
	1552	3	coef_probs_32x32 [1] [1] [0] [1] [0..2]	82, 17, 222	82, 17, 222	0	1500											
	1555	3	coef_probs_32x32 [1] [1] [0] [2] [0..2]	25, 17, 162	25, 17, 162	0	1503											
	1558	3	coef_probs_32x32 [1] [1] [1] [0] [0..2]	126, 186, 247	126, 186, 247	0	1506											
	1561	3	coef_probs_32x32 [1] [1] [1] [1] [0..2]	234, 191, 243	234, 191, 243	0	1509											
	1564	3	coef_probs_32x32 [1] [1] [1] [2] [0..2]	176, 177, 234	176, 177, 23	0	1512											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
					4													
	1567	3	coef_probs_32x32 [1] [1] [1] [3] [0..2]	104, 158, 220	104, 158, 220	0	1515											
	1570	3	coef_probs_32x32 [1] [1] [1] [4] [0..2]	66, 128, 186	66, 128, 186	0	1518											
	1573	3	coef_probs_32x32 [1] [1] [1] [5] [0..2]	55, 90, 137	55, 90, 137	0	1521											
	1576	3	coef_probs_32x32 [1] [1] [2] [0] [0..2]	111, 197, 242	111, 197, 242	0	1524											
	1579	3	coef_probs_32x32 [1] [1] [2] [1] [0..2]	46, 158, 219	46, 158, 219	0	1527											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
	1582	3	coef_probs_32x32 [1] [1] [2] [2] [0..2]	9, 104, 171	9, 104, 171	0	1530											
	1585	3	coef_probs_32x32 [1] [1] [2] [3] [0..2]	2, 65, 125	2, 65, 125	0	1533											
	1588	3	coef_probs_32x32 [1] [1] [2] [4] [0..2]	1, 44, 80	1, 44, 80	0	1536											
	1591	3	coef_probs_32x32 [1] [1] [2] [5] [0..2]	1, 17, 91	1, 17, 91	0	1539											
	1594	3	coef_probs_32x32 [1] [1] [3] [0] [0..2]	104, 208, 245	104, 208, 245	0	1542											
	1597	3	coef_probs_32x32 [1] [1] [3] [1] [0..2]	39, 168, 224	39, 168, 22	0	1545											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
					4													
	1600	3	coef_probs_32x32 [1] [1] [3] [2] [0..2]	3, 109, 162	3, 109, 162	0	1548											
	1603	3	coef_probs_32x32 [1] [1] [3] [3] [0..2]	1, 79, 124	1, 79, 124	0	1551											
	1606	3	coef_probs_32x32 [1] [1] [3] [4] [0..2]	1, 50, 102	1, 50, 102	0	1554											
	1609	3	coef_probs_32x32 [1] [1] [3] [5] [0..2]	1, 43, 102	1, 43, 102	0	1557											
	1612	3	coef_probs_32x32 [1] [1] [4] [0] [0..2]	84, 220, 246	84, 220, 246	0	1560											
	1615	3	coef_probs_32x32 [1] [1] [4] [1]	31, 177, 231	31, 177, 7,	0	1563											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
			[0..2]		231													
	1618	3	coef_probs_32x32 [1] [1] [4] [2] [0..2]	2, 115, 180	2, 115, 180	0	1566											
	1621	3	coef_probs_32x32 [1] [1] [4] [3] [0..2]	1, 79, 134	1, 79, 134	0	1569											
	1624	3	coef_probs_32x32 [1] [1] [4] [4] [0..2]	1, 55, 77	1, 55, 77	0	1572											
	1627	3	coef_probs_32x32 [1] [1] [4] [5] [0..2]	1, 60, 79	1, 60, 79	0	1575											
	1630	3	coef_probs_32x32 [1] [1] [5] [0] [0..2]	43, 243, 240	43, 243, 240	0	1578											
	1633	3	coef_probs_32x32	8, 180, 217	8, 18	0	1581											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
			[1] [1] [5] [1] [0..2]		0, 217													
	1636	3	coef_probs_32x32 [1] [1] [5] [2] [0..2]	1, 115, 166	1, 115, 166	0	1584											
	1639	3	coef_probs_32x32 [1] [1] [5] [3] [0..2]	1, 84, 121	1, 84, 121	0	1587											
	1642	3	coef_probs_32x32 [1] [1] [5] [4] [0..2]	1, 51, 67	1, 51, 67	0	1590											
	1645	3	coef_probs_32x32 [1] [1] [5] [5] [0..2]	1, 16, 6	1, 16, 6	0	1593											
	1648	16	DUMMY	0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0	0, 0, 0, 0, 0, 0,	16	1596											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT		State counter EBB Address	Coefficient counter EBB Address							
												4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
					0, 0, 0, 0, 0, 0, 0, 0, 0														
CL aligned	1664	3	mbskip_probs [0..2]	192, 128, 64	192, 128, 64	0	1596	12	208	MODE COUNTERS (Others)	18-23								
	1667	3	inter_mode_probs [0] [0..2]	0, 0, 0	2, 173, 34	0	1599	15			24-51								
	1670	3	inter_mode_probs [1] [0..2]	0, 0, 0	7, 145, 85	0	1602	18											
	1673	3	inter_mode_probs [2] [0..2]	0, 0, 0	7, 166, 63	0	1605	21											
	167	3	inter_mode_prob	0, 0, 0	7,	0	16	24											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT		State counter EBB Address	Coefficient counter EBB Address							
												4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
	6		s [3] [0..2]		94, 66		08												
	1679	3	inter_mode_probs [4] [0..2]	0, 0, 0	8, 64, 46	0	1611	27											
	1682	3	inter_mode_probs [5] [0..2]	0, 0, 0	17, 81, 31	0	1614	30											
	1685	3	inter_mode_probs [6] [0..2]	0, 0, 0	25, 29, 30	0	1617	33											
	1688	2	switchable_interp_probs [0] [0..1]	0, 0	235, 162	0	1620	36			52-63								
	1690	2	switchable_interp_probs [1] [0..1]	0, 0	36, 255	0	1622	38											
	1692	2	switchable_interp_probs [2] [0..1]	0, 0	34, 3	0	1624	40											
	1694	2	switchable_interp_probs [3] [0..1]	0, 0	149, 14	0	1626	42											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
					4													
	1696	4	intra_inter_probs [0..3]	0, 0, 0, 0	9, 102, 187, 225	0	16	28	44	64-71								
	1700	5	comp_inter_probs [0..4]	0, 0, 0, 0, 0	239, 183, 119, 96, 41	0	16	32	48	72-81								
	1705	2	single_ref_probs [0] [0..1]	0, 0	33, 16	0	16	37	53	82-101								
	1707	2	single_ref_probs [1] [0..1]	0, 0	77, 74	0	16	39	55									
	1709	2	single_ref_probs [2] [0..1]	0, 0	142, 142	0	16	41	57									
	171	2	single_ref_probs	0, 0	17	0	16	59										

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
	1		[3] [0..1]		2, 170		43											
	1713	2	single_ref_probs [4] [0..1]	0, 0	238, 247	0	1645	61										
	1715	5	comp_ref_probs [0..4]	0, 0, 0, 0, 0	50, 126, 123, 221, 226	0	1647	63		102-111								
	1720	9	y_mode_probs [0] [0..8]	0, 0, 0, 0, 0, 0, 0, 0, 0	65, 32, 18, 144, 162, 194, 41, 51,	0	1652	68		112-151								

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
					98													
	1729	9	y_mode_probs [1] [0..8]	0, 0, 0, 0, 0, 0, 0, 0, 0	132, 68, 18, 165, 217, 196, 45, 40, 78	0	1661	77										
	1738	9	y_mode_probs [2] [0..8]	0, 0, 0, 0, 0, 0, 0, 0, 0	173, 80, 19, 176, 240, 193, 64, 35, 46	0	1670	86										

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
	1747	9	y_mode_probs [3] [0..8]	0, 0, 0, 0, 0, 0, 0, 0, 0	221, 135, 38, 194, 248, 121, 96, 85, 29	0	1679	95										
	1756	3	partition_probs [0] [0..2]	158, 97, 94	199, 122, 141	0	1688	104		152-215								
	1759	3	partition_probs [1] [0..2]	93, 24, 99	147, 63, 159	0	1691	107										
	1762	3	partition_probs [2] [0..2]	85, 119, 44	148,	0	1694	110										

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
					133, 118													
	1765	3	partition_probs [3] [0..2]	62, 59, 67	121, 104, 114	0	1697	113										
	1768	3	partition_probs [4] [0..2]	149, 53, 53	174, 73, 87	0	1700	116										
	1771	3	partition_probs [5] [0..2]	94, 20, 48	92, 41, 83	0	1703	119										
	1774	3	partition_probs [6] [0..2]	83, 53, 24	82, 99, 50	0	1706	122										
	1777	3	partition_probs [7] [0..2]	52, 18, 18	53, 39, 39	0	1709	125										
	1780	3	partition_probs [8] [0..2]	150, 40, 39	177, 58,	0	1712	128										

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT		State counter EBB Address	Coefficient counter EBB Address							
												4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
					59														
	1783	3	partition_probs [9] [0..2]	78, 12, 26	68, 26, 63	0	1715	131											
	1786	3	partition_probs [10] [0..2]	67, 33, 11	52, 79, 25	0	1718	134											
	1789	3	partition_probs [11] [0..2]	24, 7, 5	17, 14, 12	0	1721	137											
	1792	3	partition_probs [12] [0..2]	174, 35, 49	222, 34, 30	0	1724	140											
	1795	3	partition_probs [13] [0..2]	68, 11, 27	72, 16, 44	0	1727	143											
	1798	3	partition_probs [14] [0..2]	57, 15, 9	58, 32, 12	0	1730	146											
	1801	3	partition_probs [15] [0..2]	12, 3, 3	10, 7, 6	0	1733	149											
	1804	3	mvc_joints [3]	?,?,?	?,?,?	0	1736	152		MV COUNTERS	216-219								
	180	1	mv_sign	0	12	0	17	15			220-								

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
	7		[0]		8		39	5		221								
	1808	10	mv_classes [0] [0..9]	0, 0, 0, 0, 0, 0, 0, 0, 0, 0	224, 144, 192, 168, 192, 176, 192, 198, 198, 245	0	1740	156		222-232								
	1818	1	mv_class0 [0] [0..0]	0	216	0	1750	166		233-234								
	1819	10	mv_bits [0] [0..9]	0, 0, 0, 0, 0, 0, 0, 0, 0, 0	136, 140,	0	1751	167		235-254								

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT		State counter EBB Address	Coefficient counter EBB Address							
												4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
					148, 160, 176, 192, 224, 234, 234, 240														
	1829	1	mv_sign [1]	0	128	0	1761	177			255-256								
	1830	10	mv_classes [1] [0..9]	0, 0, 0, 0, 0, 0, 0, 0, 0, 0	216, 128, 176, 160, 176,	0	1762	178			257-267								

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT		State counter EBB Address	Coefficient counter EBB Address							
												4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
					176, 192, 198, 198, 208														
	1840	1	mv_class0 [1] [0..0]	0	208	0	1772	188			268-269								
	1841	10	mv_bits [1] [0..9]	0, 0, 0, 0, 0, 0, 0, 0, 0, 0	136, 140, 148, 160, 176, 192, 224, 234,	0	1773	189			270-289								

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
					234, 240													
	1851	3	mv_class0_fp [0] [0] [0..2]	0, 0, 0	128, 128, 64	0	1783	199		290-297								
	1854	3	mv_class0_fp [0] [1] [0..2]	0, 0, 0	96, 112, 64	0	1786	202										
	1863	3	mv_fp [0] [0..2]	0, 0, 0	64, 96, 64	0	1789	205		298-301								
	1857	3	mv_class0_fp [1] [0] [0..2]	0, 0, 0	128, 128, 64	0	1792	208		302-309								
	1860	3	mv_class0_fp [1] [1] [0..2]	0, 0, 0	96, 112, 64	0	1795	211										
	186	3	mv_fp	0, 0, 0	64,	0	17	21		310-								

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT		State counter EBB Address	Coefficient counter EBB Address							
												4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
	6		[1] [0..2]		96, 64		98	4			313								
	1869	2	mv_class0_hp [0..1]	0, 0	160, 160	0	1801	217			314-315								
	1871	2	mv_hp [0..1]	0, 0	128, 128	0	1803	219			316-317								
	1873	47	DUMMY	0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0	0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,	47	1805	221											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults	Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
								4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
					0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,										

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT		State counter EBB Address	Coefficient counter EBB Address							
												4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
					0, 0														
CL aligned	1920	9	uv_mode_probs [0] [0..8]	144, 11, 54, 157, 195, 130, 46, 58, 108	120, 7, 76, 176, 208, 126, 28, 54, 103	0	1805	221	240	MODE COUNTERS (Others)	318-417								
	1929	9	uv_mode_probs [1] [0..8]	118, 15, 123, 148, 131, 101, 44, 93, 131	48, 12, 154, 155, 139, 90, 34, 117,	0	1814	230											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
					119													
	1938	9	uv_mode_probs [2] [0..8]	113, 12, 23, 188, 226, 142, 26, 32, 125	67, 6, 25, 204, 243, 158, 13, 21, 96	0	1823	239										
	1947	9	uv_mode_probs [3] [0..8]	120, 11, 50, 123, 163, 135, 64, 77, 103	97, 5, 44, 131, 176, 139, 48, 68, 97	0	1832	248										
	195	9	uv_mode_probs	113, 9,	83,	0	18	25										

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
	6		[4] [0..8]	36, 155, 111, 157, 32, 44, 161	5, 42, 156, 111, 152, 26, 49, 152		41	7										
	1965	9	uv_mode_probs [5] [0..8]	116, 9, 55, 176, 76, 96, 37, 61, 149	80, 5, 58, 178, 74, 83, 33, 62, 145	0	1850	266										
	1974	9	uv_mode_probs [6] [0..8]	115, 9, 28, 141, 161, 167,	86, 5, 32, 154,	0	1859	275										

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT	State counter EBB Address	Coefficient counter EBB Address							
											4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
				21, 25, 193	192, 168, 14, 22, 163													
	1983	9	uv_mode_probs [7] [0..8]	120, 12, 32, 145, 195, 142, 32, 38, 86	85, 5, 32, 156, 216, 148, 19, 29, 73	0	1868	284										
	1992	9	uv_mode_probs [8] [0..8]	116, 12, 64, 120, 140, 125, 49, 115, 121	77, 7, 64, 116, 132, 12	0	1877	293										

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT		State counter EBB Address	Coefficient counter EBB Address							
												4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
					2, 37, 126, 120														
	2001	9	uv_mode_probs [9] [0..8]	102, 19, 66, 162, 182, 122, 35, 59, 128	101, 21, 107, 181, 192, 103, 19, 67, 125	0	1886	302											
	2010	7	seg_tree_probs [0..6]	255, 255, 255, 255, 255, 255, 255	255, 255, 255, 255, 25	0	1895	311											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT		State counter EBB Address	Coefficient counter EBB Address							
												4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
					5, 255, 255, 255														
	2017	3	seg_pred_probs [0..2]	255, 255, 255	255, 255, 255	0	1902	318											
	2020	28	DUMMY	0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0	0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0	115	1905	321											

Alignment	New Offset	# Bytes	Description	Keyframe defaults	Inter frame defaults				Capture At DV_CNT		State counter EBB Address	Coefficient counter EBB Address								
												4x4 (KF)	4x4 (INTER)	8x8 (KF)	8x8 (INTER)	16x16 (KF)	16x16 (INTER)	32x32 (KF)	32x32 (INTER)
					0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0															
CL aligned	2048																		

Stream-in formats for creating compressed header

The following memory surfaces are input to PAK for Compressed Header coding

i. Prob Diff Surface

In Probability Diff Surface, there are 1805 8-bit Probability Diffs. Each of them corresponding to a Probability Diff in Compressed Header syntax. Although, for a given compressed header, not all the Probability Diff would be coded (depends on update flag), Probability Diff Surface is fully populated with 1805 entries (1805*8 / 512 = 29 cachelines). The 1805 8-bit Probability Diffs are expected to follow Compressed Header syntax order and fully packed.

ii. Compressed Header Syntax Surface

Each of the Compressed header Coding element (described in (2)) is represented by a 4-bit field. These 4-bit fields follows Compressed Header Syntax. Each of the field has a valid, Bin_probDiff_select, Prob_select, Bin as described in the table below.

	Description
Valid	Set to 1 if this is a valid Bin OR ProbabilityDiff field to code; Set to 0 to skip coding this field
Bin_ProbDiff_select	Set to 1 if Current field is a Bin (corresponding Prob, Bin are indicated by next 2 bits); Set to 0 if Current field is Probability Diff (probability diff to be coded is located in probability surface - ReMap)
Prob_Select	If current field is Bin, set to 1 if prob is 252; set to 0 if prob is 128
Bin	if current field is Bin, this is Bin value to be encoded

Compressed Header Syntax Surface is a fixed length surface. For syntax that should not be coded, valid bit should be set to 0. Total length of Compressed Header syntax Surface has 4033 Coding elements (16132 bits in 32 cachelines):

1805 Prob Diff and Prob Update flag

4 is_coeff_updated flag (per 4x4, 8x8, 16x16, 32x32)

5 control fields (MIN (tx_mode, ALLOW_32x32), tx_mode == TX_MODE_SELECT, use_compound_pred, use_hybrid_pred)

Probability Statistics Counters Table

In VP9 encoding, statistic collection is required to utilize the Forward Adaptation feature, which can substantially improve decoding performance because no intermediate computations based on encountered tokens is necessary. After encoding a frame, the VP9 encoder writes a Statistics Counter in the memory surface (HCP_IND_OBJ_BASE_ADDR_STATE: HCP VP9 PAK Probability Counter Streamout). The counter written in the memory surface is the same order as the VP9 Compressed header format.

The Statistics Counters collect frame statistics per symbol. In the VP9 Encoder, the PAK engine is responsible for statistics counter collection. The Kernel performs probability updates based on statistics counter values.

Each counter has has an associated context according to the VP9 Specification/Model.

Probability Statistics Counters Table

Note: The following table is arranged such that each row corresponds to sixteen 32-bit counters. In other words, each row corresponds to 512 bits (1 Cacheline). The VP9 Encoder PAK engine will have a total of 193 cacheline writers in the memory surface (HCP_IND_OBJ_BASW_ADDR_STATE: HCP VP9 PAK Probability Counter Streamout) at the end of each frame.

For brevity, data in the table is abbreviated. A Context Legend table has been provided after the Probability Statistics Counters table that explains the data in more detail.

R*xxx* Value 1 row = 1 Cacheline	**16 32-bit counters**															
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**
R0	ct_tx_8x8				ct_tx_16x16						ct_tx_32x32					
	[0] [0]	[0] [1]	[1] [0]	[1] [1]	[0] [0]	[0] [1]	[0] [2]	[1] [0]	[1] [1]	[1] [2]	[0] [0]	[0] [1]	[0] [2]	[0] [3]	[1] [0]	[1] [1]
R1	ct_tx_32x32		ct_coef													
	[1] [2]	[1] [3]	[T=0] [B=0] [R=0] [CB=0] [CT=0] [N=0]	[T=0] [B=0] [R=0] [CB=0] [CT=0] [N=1]	[T=0] [B=0] [R=0] [CB=0] [CT=0] [N=2]	[T=0] [B=0] [R=0] [CB=0] [CT=0] [N=3]	[T=0] [B=0] [R=0] [CB=0] [CT=1] [N=0]	[T=0] [B=0] [R=0] [CB=0] [CT=1] [N=1]	[T=0] [B=0] [R=0] [CB=0] [CT=1] [N=2]	[T=0] [B=0] [R=0] [CB=0] [CT=1] [N=3]	[T=0] [B=0] [R=0] [CB=0] [CT=2] [N=0]	[T=0] [B=0] [R=0] [CB=0] [CT=2] [N=1]	[T=0] [B=0] [R=0] [CB=0] [CT=2] [N=2]	[T=0] [B=0] [R=0] [CB=0] [CT=2] [N=3]	[T=0] [B=0] [R=0] [CB=1] [CT=0] [N=0]	[T=0] [B=0] [R=0] [CB=1] [CT=0] [N=1]
R2	ct_coef															
	[T=0] [B=0] [R=0] [CB=1] [CT=0] [N=2]	[T=0] [B=0] [R=0] [CB=1] [CT=0] [N=3]	[T=0] [B=0] [R=0] [CB=1] [CT=1] [N=0]	[T=0] [B=0] [R=0] [CB=1] [CT=1] [N=1]	[T=0] [B=0] [R=0] [CB=1] [CT=1] [N=2]	[T=0] [B=0] [R=0] [CB=1] [CT=1] [N=3]	[T=0] [B=0] [R=0] [CB=1] [CT=2] [N=0]	[T=0] [B=0] [R=0] [CB=1] [CT=2] [N=1]	[T=0] [B=0] [R=0] [CB=1] [CT=2] [N=2]	[T=0] [B=0] [R=0] [CB=1] [CT=2] [N=3]	[T=0] [B=0] [R=0] [CB=1] [CT=3] [N=0]	[T=0] [B=0] [R=0] [CB=1] [CT=3] [N=1]	[T=0] [B=0] [R=0] [CB=1] [CT=3] [N=2]	[T=0] [B=0] [R=0] [CB=1] [CT=3] [N=3]	[T=0] [B=0] [R=0] [CB=1] [CT=4] [N=0]	[T=0] [B=0] [R=0] [CB=1] [CT=4] [N=1]

Rxxx Value 1 row = 1 Cacheline	16 32-bit counters															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R3	ct_coef															
	[T=0] [B=0] [R=0] [CB=1] [CT=4] [N=2]	[T=0] [B=0] [R=0] [CB=1] [CT=4] [N=3]	[T=0] [B=0] [R=0] [CB=1] [CT=5] [N=0]	[T=0] [B=0] [R=0] [CB=1] [CT=5] [N=1]	[T=0] [B=0] [R=0] [CB=1] [CT=5] [N=2]	[T=0] [B=0] [R=0] [CB=1] [CT=5] [N=3]	[T=0] [B=0] [R=0] [CB=2] [CT=0] [N=0]	[T=0] [B=0] [R=0] [CB=2] [CT=0] [N=1]	[T=0] [B=0] [R=0] [CB=2] [CT=0] [N=2]	[T=0] [B=0] [R=0] [CB=2] [CT=0] [N=3]	[T=0] [B=0] [R=0] [CB=2] [CT=1] [N=0]	[T=0] [B=0] [R=0] [CB=2] [CT=1] [N=1]	[T=0] [B=0] [R=0] [CB=2] [CT=1] [N=2]	[T=0] [B=0] [R=0] [CB=2] [CT=1] [N=3]	[T=0] [B=0] [R=0] [CB=2] [CT=2] [N=0]	[T=0] [B=0] [R=0] [CB=2] [CT=2] [N=1]
R4	ct_coef															
	[T=0] [B=0] [R=0] [CB=2] [CT=2] [N=2]	[T=0] [B=0] [R=0] [CB=2] [CT=2] [N=3]	[T=0] [B=0] [R=0] [CB=2] [CT=3] [N=0]	[T=0] [B=0] [R=0] [CB=2] [CT=3] [N=1]	[T=0] [B=0] [R=0] [CB=2] [CT=3] [N=2]	[T=0] [B=0] [R=0] [CB=2] [CT=3] [N=3]	[T=0] [B=0] [R=0] [CB=2] [CT=4] [N=0]	[T=0] [B=0] [R=0] [CB=2] [CT=4] [N=1]	[T=0] [B=0] [R=0] [CB=2] [CT=4] [N=2]	[T=0] [B=0] [R=0] [CB=2] [CT=4] [N=3]	[T=0] [B=0] [R=0] [CB=2] [CT=5] [N=0]	[T=0] [B=0] [R=0] [CB=2] [CT=5] [N=1]	[T=0] [B=0] [R=0] [CB=2] [CT=5] [N=2]	[T=0] [B=0] [R=0] [CB=2] [CT=5] [N=3]	[T=0] [B=0] [R=0] [CB=3] [CT=0] [N=0]	[T=0] [B=0] [R=0] [CB=3] [CT=0] [N=1]
R5	ct_coef															
	[T=0] [B=0] [R=0] [CB=3] [CT=0] [N=2]	[T=0] [B=0] [R=0] [CB=3] [CT=0] [N=3]	[T=0] [B=0] [R=0] [CB=3] [CT=1] [N=0]	[T=0] [B=0] [R=0] [CB=3] [CT=1] [N=1]	[T=0] [B=0] [R=0] [CB=3] [CT=1] [N=2]	[T=0] [B=0] [R=0] [CB=3] [CT=1] [N=3]	[T=0] [B=0] [R=0] [CB=3] [CT=2] [N=0]	[T=0] [B=0] [R=0] [CB=3] [CT=2] [N=1]	[T=0] [B=0] [R=0] [CB=3] [CT=2] [N=2]	[T=0] [B=0] [R=0] [CB=3] [CT=2] [N=3]	[T=0] [B=0] [R=0] [CB=3] [CT=3] [N=0]	[T=0] [B=0] [R=0] [CB=3] [CT=3] [N=1]	[T=0] [B=0] [R=0] [CB=3] [CT=3] [N=2]	[T=0] [B=0] [R=0] [CB=3] [CT=3] [N=3]	[T=0] [B=0] [R=0] [CB=3] [CT=4] [N=0]	[T=0] [B=0] [R=0] [CB=3] [CT=4] [N=1]
R6	ct_coef															
	[T=0]	[T=0]	[T=0]	[T=0]	[T=0]	[T=0]	[T=0]	[T=0]	[T=0]	[T=0]	[T=0]	[T=0]	[T=0]	[T=0]	[T=0]	[T=0]

Rxxx Value 1 row = 1 Cacheline	16 32-bit counters															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	[B=0] [R=0] [CB=3] [CT=4] [N=2]	[B=0] [R=0] [CB=3] [CT=4] [N=3]	[B=0] [R=0] [CB=3] [CT=5] [N=0]	[B=0] [R=0] [CB=3] [CT=5] [N=1]	[B=0] [R=0] [CB=3] [CT=5] [N=2]	[B=0] [R=0] [CB=3] [CT=5] [N=3]	[B=0] [R=0] [CB=4] [CT=0] [N=0]	[B=0] [R=0] [CB=4] [CT=0] [N=1]	[B=0] [R=0] [CB=4] [CT=0] [N=2]	[B=0] [R=0] [CB=4] [CT=0] [N=3]	[B=0] [R=0] [CB=4] [CT=1] [N=0]	[B=0] [R=0] [CB=4] [CT=1] [N=1]	[B=0] [R=0] [CB=4] [CT=1] [N=2]	[B=0] [R=0] [CB=4] [CT=1] [N=3]	[B=0] [R=0] [CB=4] [CT=2] [N=0]	[B=0] [R=0] [CB=4] [CT=2] [N=1]
R7	ct_coef															
	[T=0] [B=0] [R=0] [CB=4] [CT=2] [N=2]	[T=0] [B=0] [R=0] [CB=4] [CT=2] [N=3]	[T=0] [B=0] [R=0] [CB=4] [CT=3] [N=0]	[T=0] [B=0] [R=0] [CB=4] [CT=3] [N=1]	[T=0] [B=0] [R=0] [CB=4] [CT=3] [N=2]	[T=0] [B=0] [R=0] [CB=4] [CT=3] [N=3]	[T=0] [B=0] [R=0] [CB=4] [CT=4] [N=0]	[T=0] [B=0] [R=0] [CB=4] [CT=4] [N=1]	[T=0] [B=0] [R=0] [CB=4] [CT=4] [N=2]	[T=0] [B=0] [R=0] [CB=4] [CT=4] [N=3]	[T=0] [B=0] [R=0] [CB=4] [CT=5] [N=0]	[T=0] [B=0] [R=0] [CB=4] [CT=5] [N=1]	[T=0] [B=0] [R=0] [CB=4] [CT=5] [N=2]	[T=0] [B=0] [R=0] [CB=4] [CT=5] [N=3]	[T=0] [B=0] [R=0] [CB=5] [CT=0] [N=0]	[T=0] [B=0] [R=0] [CB=5] [CT=0] [N=1]
R8	ct_coef															
	[T=0] [B=0] [R=0] [CB=5] [CT=0] [N=2]	[T=0] [B=0] [R=0] [CB=5] [CT=0] [N=3]	[T=0] [B=0] [R=0] [CB=5] [CT=1] [N=0]	[T=0] [B=0] [R=0] [CB=5] [CT=1] [N=1]	[T=0] [B=0] [R=0] [CB=5] [CT=1] [N=2]	[T=0] [B=0] [R=0] [CB=5] [CT=1] [N=3]	[T=0] [B=0] [R=0] [CB=5] [CT=2] [N=0]	[T=0] [B=0] [R=0] [CB=5] [CT=2] [N=1]	[T=0] [B=0] [R=0] [CB=5] [CT=2] [N=2]	[T=0] [B=0] [R=0] [CB=5] [CT=2] [N=3]	[T=0] [B=0] [R=0] [CB=5] [CT=3] [N=0]	[T=0] [B=0] [R=0] [CB=5] [CT=3] [N=1]	[T=0] [B=0] [R=0] [CB=5] [CT=3] [N=2]	[T=0] [B=0] [R=0] [CB=5] [CT=3] [N=3]	[T=0] [B=0] [R=0] [CB=5] [CT=4] [N=0]	[T=0] [B=0] [R=0] [CB=5] [CT=4] [N=1]
R9	ct_coef															
	[T=0] [B=0] [R=0]	[T=0] [B=0] [R=0]	[T=0] [B=0] [R=0]	[T=0] [B=0] [R=0]	[T=0] [B=0] [R=0]	[T=0] [B=0] [R=0]	[T=0] [B=0] [R=1]	[T=0] [B=0] [R=1]	[T=0] [B=0] [R=1]	[T=0] [B=0] [R=1]	[T=0] [B=0] [R=1]	[T=0] [B=0] [R=1]	[T=0] [B=0] [R=1]	[T=0] [B=0] [R=1]	[T=0] [B=0] [R=1]	[T=0] [B=0] [R=1]

Rxxx Value 1 row = 1 Cacheline	16 32-bit counters															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	[CB=5] [CT=4] [N=2]	[CB=5] [CT=4] [N=3]	[CB=5] [CT=5] [N=0]	[CB=5] [CT=5] [N=1]	[CB=5] [CT=5] [N=2]	[CB=5] [CT=5] [N=3]	[CB=0] [CT=0] [N=0]	[CB=0] [CT=0] [N=1]	[CB=0] [CT=0] [N=2]	[CB=0] [CT=0] [N=3]	[CB=0] [CT=1] [N=0]	[CB=0] [CT=1] [N=1]	[CB=0] [CT=1] [N=2]	[CB=0] [CT=1] [N=3]	[CB=0] [CT=2] [N=0]	[CB=0] [CT=2] [N=1]
R10	ct_coef															
	[T=0] [B=0] [R=1] [CB=0] [CT=2] [N=2]	[T=0] [B=0] [R=1] [CB=0] [CT=2] [N=3]	[T=0] [B=0] [R=1] [CB=1] [CT=0] [N=0]	[T=0] [B=0] [R=1] [CB=1] [CT=0] [N=1]	[T=0] [B=0] [R=1] [CB=1] [CT=0] [N=2]	[T=0] [B=0] [R=1] [CB=1] [CT=0] [N=3]	[T=0] [B=0] [R=1] [CB=1] [CT=1] [N=0]	[T=0] [B=0] [R=1] [CB=1] [CT=1] [N=1]	[T=0] [B=0] [R=1] [CB=1] [CT=1] [N=2]	[T=0] [B=0] [R=1] [CB=1] [CT=1] [N=3]	[T=0] [B=0] [R=1] [CB=1] [CT=2] [N=0]	[T=0] [B=0] [R=1] [CB=1] [CT=2] [N=1]	[T=0] [B=0] [R=1] [CB=1] [CT=2] [N=2]	[T=0] [B=0] [R=1] [CB=1] [CT=2] [N=3]	[T=0] [B=0] [R=1] [CB=1] [CT=3] [N=0]	[T=0] [B=0] [R=1] [CB=1] [CT=3] [N=1]
R11	ct_coef															
	[T=0] [B=0] [R=1] [CB=1] [CT=3] [N=2]	[T=0] [B=0] [R=1] [CB=1] [CT=3] [N=3]	[T=0] [B=0] [R=1] [CB=1] [CT=4] [N=0]	[T=0] [B=0] [R=1] [CB=1] [CT=4] [N=1]	[T=0] [B=0] [R=1] [CB=1] [CT=4] [N=2]	[T=0] [B=0] [R=1] [CB=1] [CT=4] [N=3]	[T=0] [B=0] [R=1] [CB=1] [CT=5] [N=0]	[T=0] [B=0] [R=1] [CB=1] [CT=5] [N=1]	[T=0] [B=0] [R=1] [CB=1] [CT=5] [N=2]	[T=0] [B=0] [R=1] [CB=1] [CT=5] [N=3]	[T=0] [B=0] [R=1] [CB=2] [CT=0] [N=0]	[T=0] [B=0] [R=1] [CB=2] [CT=0] [N=1]	[T=0] [B=0] [R=1] [CB=2] [CT=0] [N=2]	[T=0] [B=0] [R=1] [CB=2] [CT=0] [N=3]	[T=0] [B=0] [R=1] [CB=2] [CT=1] [N=0]	[T=0] [B=0] [R=1] [CB=2] [CT=1] [N=1]
R12	ct_coef															
	[T=0] [B=0] [R=1] [CB=2] [CT=1]	[T=0] [B=0] [R=1] [CB=2]	[T=0] [B=0] [R=1] [CB=2]	[T=0] [B=0] [R=1] [CB=2]	[T=0] [B=0] [R=1] [CB=2]	[T=0] [B=0] [R=1] [CB=2]	[T=0] [B=0] [R=1] [CB=2]	[T=0] [B=0] [R=1] [CB=2]	[T=0] [B=0] [R=1] [CB=2]	[T=0] [B=0] [R=1] [CB=2]	[T=0] [B=0] [R=1] [CB=2]	[T=0] [B=0] [R=1] [CB=2]	[T=0] [B=0] [R=1] [CB=2]	[T=0] [B=0] [R=1] [CB=2]	[T=0] [B=0] [R=1] [CB=2]	[T=0] [B=0] [R=1] [CB=2] [CT=5]

Rxxx Value 1 row = 1 Cacheline	16 32-bit counters															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	[N=2]	[CT=1] [N=3]	[CT=2] [N=0]	[CT=2] [N=1]	[CT=2] [N=2]	[CT=2] [N=3]	[CT=3] [N=0]	[CT=3] [N=1]	[CT=3] [N=2]	[CT=3] [N=3]	[CT=4] [N=0]	[CT=4] [N=1]	[CT=4] [N=2]	[CT=4] [N=3]	[CT=5] [N=0]	[N=1]
R13	ct_coef															
	[T=0] [B=0] [R=1] [CB=2] [CT=5] [N=2]	[T=0] [B=0] [R=1] [CB=2] [CT=5] [N=3]	[T=0] [B=0] [R=1] [CB=3] [CT=0] [N=0]	[T=0] [B=0] [R=1] [CB=3] [CT=0] [N=1]	[T=0] [B=0] [R=1] [CB=3] [CT=0] [N=2]	[T=0] [B=0] [R=1] [CB=3] [CT=0] [N=3]	[T=0] [B=0] [R=1] [CB=3] [CT=1] [N=0]	[T=0] [B=0] [R=1] [CB=3] [CT=1] [N=1]	[T=0] [B=0] [R=1] [CB=3] [CT=1] [N=2]	[T=0] [B=0] [R=1] [CB=3] [CT=1] [N=3]	[T=0] [B=0] [R=1] [CB=3] [CT=2] [N=0]	[T=0] [B=0] [R=1] [CB=3] [CT=2] [N=1]	[T=0] [B=0] [R=1] [CB=3] [CT=2] [N=2]	[T=0] [B=0] [R=1] [CB=3] [CT=2] [N=3]	[T=0] [B=0] [R=1] [CB=3] [CT=3] [N=0]	[T=0] [B=0] [R=1] [CB=3] [CT=3] [N=1]
R14	ct_coef															
	[T=0] [B=0] [R=1] [CB=3] [CT=3] [N=2]	[T=0] [B=0] [R=1] [CB=3] [CT=3] [N=3]	[T=0] [B=0] [R=1] [CB=3] [CT=4] [N=0]	[T=0] [B=0] [R=1] [CB=3] [CT=4] [N=1]	[T=0] [B=0] [R=1] [CB=3] [CT=4] [N=2]	[T=0] [B=0] [R=1] [CB=3] [CT=4] [N=3]	[T=0] [B=0] [R=1] [CB=3] [CT=5] [N=0]	[T=0] [B=0] [R=1] [CB=3] [CT=5] [N=1]	[T=0] [B=0] [R=1] [CB=3] [CT=5] [N=2]	[T=0] [B=0] [R=1] [CB=3] [CT=5] [N=3]	[T=0] [B=0] [R=1] [CB=4] [CT=0] [N=0]	[T=0] [B=0] [R=1] [CB=4] [CT=0] [N=1]	[T=0] [B=0] [R=1] [CB=4] [CT=0] [N=2]	[T=0] [B=0] [R=1] [CB=4] [CT=0] [N=3]	[T=0] [B=0] [R=1] [CB=4] [CT=1] [N=0]	[T=0] [B=0] [R=1] [CB=4] [CT=1] [N=1]
R15	ct_coef															
	[T=0] [B=0] [R=1] [CB=4] [CT=1] [N=2]	[T=0] [B=0] [R=1] [CB=4] [CT=1]	[T=0] [B=0] [R=1] [CB=4] [CT=2]	[T=0] [B=0] [R=1] [CB=4] [CT=2]	[T=0] [B=0] [R=1] [CB=4] [CT=2]	[T=0] [B=0] [R=1] [CB=4] [CT=2]	[T=0] [B=0] [R=1] [CB=4] [CT=3]	[T=0] [B=0] [R=1] [CB=4] [CT=3]	[T=0] [B=0] [R=1] [CB=4] [CT=3]	[T=0] [B=0] [R=1] [CB=4] [CT=3]	[T=0] [B=0] [R=1] [CB=4] [CT=4] [N=0]	[T=0] [B=0] [R=1] [CB=4] [CT=4] [N=1]	[T=0] [B=0] [R=1] [CB=4] [CT=4]	[T=0] [B=0] [R=1] [CB=4] [CT=4]	[T=0] [B=0] [R=1] [CB=4] [CT=5]	[T=0] [B=0] [R=1] [CB=4] [CT=5] [N=1]

Rxxx Value 1 row = 1 Cacheline	16 32-bit counters															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		[N=3]	[N=0]	[N=1]	[N=2]	[N=3]	[N=0]	[N=1]	[N=2]	[N=3]			[N=2]	[N=3]	[N=0]	
R16	ct_coef															
	[T=0] [B=0] [R=1] [CB=4] [CT=5] [N=2]	[T=0] [B=0] [R=1] [CB=4] [CT=5] [N=3]	[T=0] [B=0] [R=1] [CB=5] [CT=0] [N=0]	[T=0] [B=0] [R=1] [CB=5] [CT=0] [N=1]	[T=0] [B=0] [R=1] [CB=5] [CT=0] [N=2]	[T=0] [B=0] [R=1] [CB=5] [CT=0] [N=3]	[T=0] [B=0] [R=1] [CB=5] [CT=1] [N=0]	[T=0] [B=0] [R=1] [CB=5] [CT=1] [N=1]	[T=0] [B=0] [R=1] [CB=5] [CT=1] [N=2]	[T=0] [B=0] [R=1] [CB=5] [CT=1] [N=3]	[T=0] [B=0] [R=1] [CB=5] [CT=2] [N=0]	[T=0] [B=0] [R=1] [CB=5] [CT=2] [N=1]	[T=0] [B=0] [R=1] [CB=5] [CT=2] [N=2]	[T=0] [B=0] [R=1] [CB=5] [CT=2] [N=3]	[T=0] [B=0] [R=1] [CB=5] [CT=3] [N=0]	[T=0] [B=0] [R=1] [CB=5] [CT=3] [N=1]
R17	ct_coef															
	[T=0] [B=0] [R=1] [CB=5] [CT=3] [N=2]	[T=0] [B=0] [R=1] [CB=5] [CT=3] [N=3]	[T=0] [B=0] [R=1] [CB=5] [CT=4] [N=0]	[T=0] [B=0] [R=1] [CB=5] [CT=4] [N=1]	[T=0] [B=0] [R=1] [CB=5] [CT=4] [N=2]	[T=0] [B=0] [R=1] [CB=5] [CT=4] [N=3]	[T=0] [B=0] [R=1] [CB=5] [CT=5] [N=0]	[T=0] [B=0] [R=1] [CB=5] [CT=5] [N=1]	[T=0] [B=0] [R=1] [CB=5] [CT=5] [N=2]	[T=0] [B=0] [R=1] [CB=5] [CT=5] [N=3]	[T=0] [B=1] [R=0] [CB=0] [CT=0] [N=0]	[T=0] [B=1] [R=0] [CB=0] [CT=0] [N=1]	[T=0] [B=1] [R=0] [CB=0] [CT=0] [N=2]	[T=0] [B=1] [R=0] [CB=0] [CT=0] [N=3]	[T=0] [B=1] [R=0] [CB=0] [CT=1] [N=0]	[T=0] [B=1] [R=0] [CB=0] [CT=1] [N=1]
R18	ct_coef															
	[T=0] [B=1] [R=0] [CB=0] [CT=1] [N=2]	[T=0] [B=1] [R=0] [CB=0] [CT=1] [N=3]	[T=0] [B=1] [R=0] [CB=0] [CT=2] [N=0]	[T=0] [B=1] [R=0] [CB=0] [CT=2] [N=1]	[T=0] [B=1] [R=0] [CB=0] [CT=2] [N=2]	[T=0] [B=1] [R=0] [CB=0] [CT=2] [N=3]	[T=0] [B=1] [R=0] [CB=1] [CT=0] [N=0]	[T=0] [B=1] [R=0] [CB=1] [CT=0] [N=1]	[T=0] [B=1] [R=0] [CB=1] [CT=0] [N=2]	[T=0] [B=1] [R=0] [CB=1] [CT=0] [N=3]	[T=0] [B=1] [R=0] [CB=1] [CT=1] [N=0]	[T=0] [B=1] [R=0] [CB=1] [CT=1] [N=1]	[T=0] [B=1] [R=0] [CB=1] [CT=1] [N=2]	[T=0] [B=1] [R=0] [CB=1] [CT=1] [N=3]	[T=0] [B=1] [R=0] [CB=1] [CT=2] [N=0]	[T=0] [B=1] [R=0] [CB=1] [CT=2] [N=1]
R19	ct_coef															

Rxxx Value 1 row = 1 Cacheline	16 32-bit counters															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	[T=0] [B=1] [R=0] [CB=1] [CT=2] [N=2]	[T=0] [B=1] [R=0] [CB=1] [CT=2] [N=3]	[T=0] [B=1] [R=0] [CB=1] [CT=3] [N=0]	[T=0] [B=1] [R=0] [CB=1] [CT=3] [N=1]	[T=0] [B=1] [R=0] [CB=1] [CT=3] [N=2]	[T=0] [B=1] [R=0] [CB=1] [CT=3] [N=3]	[T=0] [B=1] [R=0] [CB=1] [CT=4] [N=0]	[T=0] [B=1] [R=0] [CB=1] [CT=4] [N=1]	[T=0] [B=1] [R=0] [CB=1] [CT=4] [N=2]	[T=0] [B=1] [R=0] [CB=1] [CT=4] [N=3]	[T=0] [B=1] [R=0] [CB=1] [CT=5] [N=0]	[T=0] [B=1] [R=0] [CB=1] [CT=5] [N=1]	[T=0] [B=1] [R=0] [CB=1] [CT=5] [N=2]	[T=0] [B=1] [R=0] [CB=1] [CT=5] [N=3]	[T=0] [B=1] [R=0] [CB=2] [CT=0] [N=0]	[T=0] [B=1] [R=0] [CB=2] [CT=0] [N=1]
R20	ct_coef															
	[T=0] [B=1] [R=0] [CB=2] [CT=0] [N=2]	[T=0] [B=1] [R=0] [CB=2] [CT=0] [N=3]	[T=0] [B=1] [R=0] [CB=2] [CT=1] [N=0]	[T=0] [B=1] [R=0] [CB=2] [CT=1] [N=1]	[T=0] [B=1] [R=0] [CB=2] [CT=1] [N=2]	[T=0] [B=1] [R=0] [CB=2] [CT=1] [N=3]	[T=0] [B=1] [R=0] [CB=2] [CT=2] [N=0]	[T=0] [B=1] [R=0] [CB=2] [CT=2] [N=1]	[T=0] [B=1] [R=0] [CB=2] [CT=2] [N=2]	[T=0] [B=1] [R=0] [CB=2] [CT=2] [N=3]	[T=0] [B=1] [R=0] [CB=2] [CT=3] [N=0]	[T=0] [B=1] [R=0] [CB=2] [CT=3] [N=1]	[T=0] [B=1] [R=0] [CB=2] [CT=3] [N=2]	[T=0] [B=1] [R=0] [CB=2] [CT=3] [N=3]	[T=0] [B=1] [R=0] [CB=2] [CT=4] [N=0]	[T=0] [B=1] [R=0] [CB=2] [CT=4] [N=1]
R21	ct_coef															
	[T=0] [B=1] [R=0] [CB=2] [CT=4] [N=2]	[T=0] [B=1] [R=0] [CB=2] [CT=4] [N=3]	[T=0] [B=1] [R=0] [CB=2] [CT=5] [N=0]	[T=0] [B=1] [R=0] [CB=2] [CT=5] [N=1]	[T=0] [B=1] [R=0] [CB=2] [CT=5] [N=2]	[T=0] [B=1] [R=0] [CB=2] [CT=5] [N=3]	[T=0] [B=1] [R=0] [CB=3] [CT=0] [N=0]	[T=0] [B=1] [R=0] [CB=3] [CT=0] [N=1]	[T=0] [B=1] [R=0] [CB=3] [CT=0] [N=2]	[T=0] [B=1] [R=0] [CB=3] [CT=0] [N=3]	[T=0] [B=1] [R=0] [CB=3] [CT=1] [N=0]	[T=0] [B=1] [R=0] [CB=3] [CT=1] [N=1]	[T=0] [B=1] [R=0] [CB=3] [CT=1] [N=2]	[T=0] [B=1] [R=0] [CB=3] [CT=1] [N=3]	[T=0] [B=1] [R=0] [CB=3] [CT=2] [N=0]	[T=0] [B=1] [R=0] [CB=3] [CT=2] [N=1]
R22	ct_coef															
	[T=0] [B=1]	[T=0] [B=1]	[T=0] [B=1]	[T=0] [B=1]	[T=0] [B=1]	[T=0] [B=1]	[T=0] [B=1]	[T=0] [B=1]	[T=0] [B=1]	[T=0] [B=1]	[T=0] [B=1]	[T=0] [B=1]	[T=0] [B=1]	[T=0] [B=1]	[T=0] [B=1]	[T=0] [B=1]

Rxxx Value 1 row = 1 Cacheline	16 32-bit counters															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	[R=0] [CB=3] [CT=2] [N=2]	[R=0] [CB=3] [CT=2] [N=3]	[R=0] [CB=3] [CT=3] [N=0]	[R=0] [CB=3] [CT=3] [N=1]	[R=0] [CB=3] [CT=3] [N=2]	[R=0] [CB=3] [CT=3] [N=3]	[R=0] [CB=3] [CT=4] [N=0]	[R=0] [CB=3] [CT=4] [N=1]	[R=0] [CB=3] [CT=4] [N=2]	[R=0] [CB=3] [CT=4] [N=3]	[R=0] [CB=3] [CT=5] [N=0]	[R=0] [CB=3] [CT=5] [N=1]	[R=0] [CB=3] [CT=5] [N=2]	[R=0] [CB=3] [CT=5] [N=3]	[R=0] [CB=4] [CT=0] [N=0]	[R=0] [CB=4] [CT=0] [N=1]
R23	ct_coef															
	[T=0] [B=1] [R=0] [CB=4] [CT=0] [N=2]	[T=0] [B=1] [R=0] [CB=4] [CT=0] [N=3]	[T=0] [B=1] [R=0] [CB=4] [CT=1] [N=0]	[T=0] [B=1] [R=0] [CB=4] [CT=1] [N=1]	[T=0] [B=1] [R=0] [CB=4] [CT=1] [N=2]	[T=0] [B=1] [R=0] [CB=4] [CT=1] [N=3]	[T=0] [B=1] [R=0] [CB=4] [CT=2] [N=0]	[T=0] [B=1] [R=0] [CB=4] [CT=2] [N=1]	[T=0] [B=1] [R=0] [CB=4] [CT=2] [N=2]	[T=0] [B=1] [R=0] [CB=4] [CT=2] [N=3]	[T=0] [B=1] [R=0] [CB=4] [CT=3] [N=0]	[T=0] [B=1] [R=0] [CB=4] [CT=3] [N=1]	[T=0] [B=1] [R=0] [CB=4] [CT=3] [N=2]	[T=0] [B=1] [R=0] [CB=4] [CT=3] [N=3]	[T=0] [B=1] [R=0] [CB=4] [CT=4] [N=0]	[T=0] [B=1] [R=0] [CB=4] [CT=4] [N=1]
R24	ct_coef															
	[T=0] [B=1] [R=0] [CB=4] [CT=4] [N=2]	[T=0] [B=1] [R=0] [CB=4] [CT=4] [N=3]	[T=0] [B=1] [R=0] [CB=4] [CT=5] [N=0]	[T=0] [B=1] [R=0] [CB=4] [CT=5] [N=1]	[T=0] [B=1] [R=0] [CB=4] [CT=5] [N=2]	[T=0] [B=1] [R=0] [CB=4] [CT=5] [N=3]	[T=0] [B=1] [R=0] [CB=5] [CT=0] [N=0]	[T=0] [B=1] [R=0] [CB=5] [CT=0] [N=1]	[T=0] [B=1] [R=0] [CB=5] [CT=0] [N=2]	[T=0] [B=1] [R=0] [CB=5] [CT=0] [N=3]	[T=0] [B=1] [R=0] [CB=5] [CT=1] [N=0]	[T=0] [B=1] [R=0] [CB=5] [CT=1] [N=1]	[T=0] [B=1] [R=0] [CB=5] [CT=1] [N=2]	[T=0] [B=1] [R=0] [CB=5] [CT=1] [N=3]	[T=0] [B=1] [R=0] [CB=5] [CT=2] [N=0]	[T=0] [B=1] [R=0] [CB=5] [CT=2] [N=1]
R25	ct_coef															
	[T=0] [B=1] [R=0] [CB=5]	[T=0] [B=1] [R=0]	[T=0] [B=1] [R=0]	[T=0] [B=1] [R=0]	[T=0] [B=1] [R=0]	[T=0] [B=1] [R=0]	[T=0] [B=1] [R=0]	[T=0] [B=1] [R=0]	[T=0] [B=1] [R=0]	[T=0] [B=1] [R=0]	[T=0] [B=1] [R=0]	[T=0] [B=1] [R=0]	[T=0] [B=1] [R=0]	[T=0] [B=1] [R=0]	[T=0] [B=1] [R=1]	[T=0] [B=1] [R=1] [CB=0]

Rxxx Value 1 row = 1 Cacheline	16 32-bit counters															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	[CT=2] [N=2]	[CB=5] [CT=2] [N=3]	[CB=5] [CT=3] [N=0]	[CB=5] [CT=3] [N=1]	[CB=5] [CT=3] [N=2]	[CB=5] [CT=3] [N=3]	[CB=5] [CT=4] [N=0]	[CB=5] [CT=4] [N=1]	[CB=5] [CT=4] [N=2]	[CB=5] [CT=4] [N=3]	[CB=5] [CT=5] [N=0]	[CB=5] [CT=5] [N=1]	[CB=5] [CT=5] [N=2]	[CB=5] [CT=5] [N=3]	[CB=0] [CT=0] [N=0]	[CT=0] [N=1]
R26	ct_coef															
	[T=0] [B=1] [R=1] [CB=0] [CT=0] [N=2]	[T=0] [B=1] [R=1] [CB=0] [CT=0] [N=3]	[T=0] [B=1] [R=1] [CB=0] [CT=1] [N=0]	[T=0] [B=1] [R=1] [CB=0] [CT=1] [N=1]	[T=0] [B=1] [R=1] [CB=0] [CT=1] [N=2]	[T=0] [B=1] [R=1] [CB=0] [CT=1] [N=3]	[T=0] [B=1] [R=1] [CB=0] [CT=2] [N=0]	[T=0] [B=1] [R=1] [CB=0] [CT=2] [N=1]	[T=0] [B=1] [R=1] [CB=0] [CT=2] [N=2]	[T=0] [B=1] [R=1] [CB=0] [CT=2] [N=3]	[T=0] [B=1] [R=1] [CB=1] [CT=0] [N=0]	[T=0] [B=1] [R=1] [CB=1] [CT=0] [N=1]	[T=0] [B=1] [R=1] [CB=1] [CT=0] [N=2]	[T=0] [B=1] [R=1] [CB=1] [CT=0] [N=3]	[T=0] [B=1] [R=1] [CB=1] [CT=1] [N=0]	[T=0] [B=1] [R=1] [CB=1] [CT=1] [N=1]
R27	ct_coef															
	[T=0] [B=1] [R=1] [CB=1] [CT=1] [N=2]	[T=0] [B=1] [R=1] [CB=1] [CT=1] [N=3]	[T=0] [B=1] [R=1] [CB=1] [CT=2] [N=0]	[T=0] [B=1] [R=1] [CB=1] [CT=2] [N=1]	[T=0] [B=1] [R=1] [CB=1] [CT=2] [N=2]	[T=0] [B=1] [R=1] [CB=1] [CT=2] [N=3]	[T=0] [B=1] [R=1] [CB=1] [CT=3] [N=0]	[T=0] [B=1] [R=1] [CB=1] [CT=3] [N=1]	[T=0] [B=1] [R=1] [CB=1] [CT=3] [N=2]	[T=0] [B=1] [R=1] [CB=1] [CT=3] [N=3]	[T=0] [B=1] [R=1] [CB=1] [CT=4] [N=0]	[T=0] [B=1] [R=1] [CB=1] [CT=4] [N=1]	[T=0] [B=1] [R=1] [CB=1] [CT=4] [N=2]	[T=0] [B=1] [R=1] [CB=1] [CT=4] [N=3]	[T=0] [B=1] [R=1] [CB=1] [CT=5] [N=0]	[T=0] [B=1] [R=1] [CB=1] [CT=5] [N=1]
R28	ct_coef															
	[T=0] [B=1] [R=1] [CB=1] [CT=5] [N=2]	[T=0] [B=1] [R=1] [CB=1]	[T=0] [B=1] [R=1] [CB=2]	[T=0] [B=1] [R=1] [CB=2]	[T=0] [B=1] [R=1] [CB=2]	[T=0] [B=1] [R=1] [CB=2]	[T=0] [B=1] [R=1] [CB=2]	[T=0] [B=1] [R=1] [CB=2]	[T=0] [B=1] [R=1] [CB=2]	[T=0] [B=1] [R=1] [CB=2]	[T=0] [B=1] [R=1] [CB=2] [CT=2]	[T=0] [B=1] [R=1] [CB=2] [CT=2]	[T=0] [B=1] [R=1] [CB=2]	[T=0] [B=1] [R=1] [CB=2]	[T=0] [B=1] [R=1] [CB=2]	[T=0] [B=1] [R=1] [CB=2] [CT=3] [N=1]

Rxxx Value 1 row = 1 Cacheline	16 32-bit counters															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		[CT=5] [N=3]	[CT=0] [N=0]	[CT=0] [N=1]	[CT=0] [N=2]	[CT=0] [N=3]	[CT=1] [N=0]	[CT=1] [N=1]	[CT=1] [N=2]	[CT=1] [N=3]	[N=0]	[N=1]	[CT=2] [N=2]	[CT=2] [N=3]	[CT=3] [N=0]	
R29	ct_coef															
	[T=0] [B=1] [R=1] [CB=2] [CT=3] [N=2]	[T=0] [B=1] [R=1] [CB=2] [CT=3] [N=3]	[T=0] [B=1] [R=1] [CB=2] [CT=4] [N=0]	[T=0] [B=1] [R=1] [CB=2] [CT=4] [N=1]	[T=0] [B=1] [R=1] [CB=2] [CT=4] [N=2]	[T=0] [B=1] [R=1] [CB=2] [CT=4] [N=3]	[T=0] [B=1] [R=1] [CB=2] [CT=5] [N=0]	[T=0] [B=1] [R=1] [CB=2] [CT=5] [N=1]	[T=0] [B=1] [R=1] [CB=2] [CT=5] [N=2]	[T=0] [B=1] [R=1] [CB=2] [CT=5] [N=3]	[T=0] [B=1] [R=1] [CB=3] [CT=0] [N=0]	[T=0] [B=1] [R=1] [CB=3] [CT=0] [N=1]	[T=0] [B=1] [R=1] [CB=3] [CT=0] [N=2]	[T=0] [B=1] [R=1] [CB=3] [CT=0] [N=3]	[T=0] [B=1] [R=1] [CB=3] [CT=1] [N=0]	[T=0] [B=1] [R=1] [CB=3] [CT=1] [N=1]
R30	ct_coef															
	[T=0] [B=1] [R=1] [CB=3] [CT=1] [N=2]	[T=0] [B=1] [R=1] [CB=3] [CT=1] [N=3]	[T=0] [B=1] [R=1] [CB=3] [CT=2] [N=0]	[T=0] [B=1] [R=1] [CB=3] [CT=2] [N=1]	[T=0] [B=1] [R=1] [CB=3] [CT=2] [N=2]	[T=0] [B=1] [R=1] [CB=3] [CT=2] [N=3]	[T=0] [B=1] [R=1] [CB=3] [CT=3] [N=0]	[T=0] [B=1] [R=1] [CB=3] [CT=3] [N=1]	[T=0] [B=1] [R=1] [CB=3] [CT=3] [N=2]	[T=0] [B=1] [R=1] [CB=3] [CT=3] [N=3]	[T=0] [B=1] [R=1] [CB=3] [CT=4] [N=0]	[T=0] [B=1] [R=1] [CB=3] [CT=4] [N=1]	[T=0] [B=1] [R=1] [CB=3] [CT=4] [N=2]	[T=0] [B=1] [R=1] [CB=3] [CT=4] [N=3]	[T=0] [B=1] [R=1] [CB=3] [CT=5] [N=0]	[T=0] [B=1] [R=1] [CB=3] [CT=5] [N=1]
R31	ct_coef															
	[T=0] [B=1] [R=1] [CB=3] [CT=5] [N=2]	[T=0] [B=1] [R=1] [CB=3] [CT=5] [N=3]	[T=0] [B=1] [R=1] [CB=4] [CT=0] [N=0]	[T=0] [B=1] [R=1] [CB=4] [CT=0] [N=1]	[T=0] [B=1] [R=1] [CB=4] [CT=0] [N=2]	[T=0] [B=1] [R=1] [CB=4] [CT=0] [N=3]	[T=0] [B=1] [R=1] [CB=4] [CT=1] [N=0]	[T=0] [B=1] [R=1] [CB=4] [CT=1] [N=1]	[T=0] [B=1] [R=1] [CB=4] [CT=1] [N=2]	[T=0] [B=1] [R=1] [CB=4] [CT=1] [N=3]	[T=0] [B=1] [R=1] [CB=4] [CT=2] [N=0]	[T=0] [B=1] [R=1] [CB=4] [CT=2] [N=1]	[T=0] [B=1] [R=1] [CB=4] [CT=2] [N=2]	[T=0] [B=1] [R=1] [CB=4] [CT=2] [N=3]	[T=0] [B=1] [R=1] [CB=4] [CT=3] [N=0]	[T=0] [B=1] [R=1] [CB=4] [CT=3] [N=1]

Rxxx Value 1 row = 1 Cacheline	16 32-bit counters															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R32	ct_coef															
	[T=0] [B=1] [R=1] [CB=4] [CT=3] [N=2]	[T=0] [B=1] [R=1] [CB=4] [CT=3] [N=3]	[T=0] [B=1] [R=1] [CB=4] [CT=4] [N=0]	[T=0] [B=1] [R=1] [CB=4] [CT=4] [N=1]	[T=0] [B=1] [R=1] [CB=4] [CT=4] [N=2]	[T=0] [B=1] [R=1] [CB=4] [CT=4] [N=3]	[T=0] [B=1] [R=1] [CB=4] [CT=5] [N=0]	[T=0] [B=1] [R=1] [CB=4] [CT=5] [N=1]	[T=0] [B=1] [R=1] [CB=4] [CT=5] [N=2]	[T=0] [B=1] [R=1] [CB=4] [CT=5] [N=3]	[T=0] [B=1] [R=1] [CB=5] [CT=0] [N=0]	[T=0] [B=1] [R=1] [CB=5] [CT=0] [N=1]	[T=0] [B=1] [R=1] [CB=5] [CT=0] [N=2]	[T=0] [B=1] [R=1] [CB=5] [CT=0] [N=3]	[T=0] [B=1] [R=1] [CB=5] [CT=1] [N=0]	[T=0] [B=1] [R=1] [CB=5] [CT=1] [N=1]
R33	ct_coef															
	[T=0] [B=1] [R=1] [CB=5] [CT=1] [N=2]	[T=0] [B=1] [R=1] [CB=5] [CT=1] [N=3]	[T=0] [B=1] [R=1] [CB=5] [CT=2] [N=0]	[T=0] [B=1] [R=1] [CB=5] [CT=2] [N=1]	[T=0] [B=1] [R=1] [CB=5] [CT=2] [N=2]	[T=0] [B=1] [R=1] [CB=5] [CT=2] [N=3]	[T=0] [B=1] [R=1] [CB=5] [CT=3] [N=0]	[T=0] [B=1] [R=1] [CB=5] [CT=3] [N=1]	[T=0] [B=1] [R=1] [CB=5] [CT=3] [N=2]	[T=0] [B=1] [R=1] [CB=5] [CT=3] [N=3]	[T=0] [B=1] [R=1] [CB=5] [CT=4] [N=0]	[T=0] [B=1] [R=1] [CB=5] [CT=4] [N=1]	[T=0] [B=1] [R=1] [CB=5] [CT=4] [N=2]	[T=0] [B=1] [R=1] [CB=5] [CT=4] [N=3]	[T=0] [B=1] [R=1] [CB=5] [CT=5] [N=0]	[T=0] [B=1] [R=1] [CB=5] [CT=5] [N=1]
R34	ct_coef															
	[T=0] [B=1] [R=1] [CB=5] [CT=5] [N=2]	[T=0] [B=1] [R=1] [CB=5] [CT=5] [N=3]	[T=1] [B=0] [R=0] [CB=0] [CT=0] [N=0]	[T=1] [B=0] [R=0] [CB=0] [CT=0] [N=1]	[T=1] [B=0] [R=0] [CB=0] [CT=0] [N=2]	[T=1] [B=0] [R=0] [CB=0] [CT=0] [N=3]	[T=1] [B=0] [R=0] [CB=0] [CT=1] [N=0]	[T=1] [B=0] [R=0] [CB=0] [CT=1] [N=1]	[T=1] [B=0] [R=0] [CB=0] [CT=1] [N=2]	[T=1] [B=0] [R=0] [CB=0] [CT=1] [N=3]	[T=1] [B=0] [R=0] [CB=0] [CT=2] [N=0]	[T=1] [B=0] [R=0] [CB=0] [CT=2] [N=1]	[T=1] [B=0] [R=0] [CB=0] [CT=2] [N=2]	[T=1] [B=0] [R=0] [CB=0] [CT=2] [N=3]	[T=1] [B=0] [R=0] [CB=1] [CT=0] [N=0]	[T=1] [B=0] [R=0] [CB=1] [CT=0] [N=1]
R35	ct_coef															
	[T=1]	[T=1]	[T=1]	[T=1]	[T=1]	[T=1]	[T=1]	[T=1]	[T=1]	[T=1]	[T=1]	[T=1]	[T=1]	[T=1]	[T=1]	[T=1]

Rxxx Value 1 row = 1 Cacheline	16 32-bit counters															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	[B=0] [R=0] [CB=1] [CT=0] [N=2]	[B=0] [R=0] [CB=1] [CT=0] [N=3]	[B=0] [R=0] [CB=1] [CT=1] [N=0]	[B=0] [R=0] [CB=1] [CT=1] [N=1]	[B=0] [R=0] [CB=1] [CT=1] [N=2]	[B=0] [R=0] [CB=1] [CT=1] [N=3]	[B=0] [R=0] [CB=1] [CT=2] [N=0]	[B=0] [R=0] [CB=1] [CT=2] [N=1]	[B=0] [R=0] [CB=1] [CT=2] [N=2]	[B=0] [R=0] [CB=1] [CT=2] [N=3]	[B=0] [R=0] [CB=1] [CT=3] [N=0]	[B=0] [R=0] [CB=1] [CT=3] [N=1]	[B=0] [R=0] [CB=1] [CT=3] [N=2]	[B=0] [R=0] [CB=1] [CT=3] [N=3]	[B=0] [R=0] [CB=1] [CT=4] [N=0]	[B=0] [R=0] [CB=1] [CT=4] [N=1]
R36	ct_coef															
	[T=1] [B=0] [R=0] [CB=1] [CT=4] [N=2]	[T=1] [B=0] [R=0] [CB=1] [CT=4] [N=3]	[T=1] [B=0] [R=0] [CB=1] [CT=5] [N=0]	[T=1] [B=0] [R=0] [CB=1] [CT=5] [N=1]	[T=1] [B=0] [R=0] [CB=1] [CT=5] [N=2]	[T=1] [B=0] [R=0] [CB=1] [CT=5] [N=3]	[T=1] [B=0] [R=0] [CB=2] [CT=0] [N=0]	[T=1] [B=0] [R=0] [CB=2] [CT=0] [N=1]	[T=1] [B=0] [R=0] [CB=2] [CT=0] [N=2]	[T=1] [B=0] [R=0] [CB=2] [CT=0] [N=3]	[T=1] [B=0] [R=0] [CB=2] [CT=1] [N=0]	[T=1] [B=0] [R=0] [CB=2] [CT=1] [N=1]	[T=1] [B=0] [R=0] [CB=2] [CT=1] [N=2]	[T=1] [B=0] [R=0] [CB=2] [CT=1] [N=3]	[T=1] [B=0] [R=0] [CB=2] [CT=2] [N=0]	[T=1] [B=0] [R=0] [CB=2] [CT=2] [N=1]
R37	ct_coef															
	[T=1] [B=0] [R=0] [CB=2] [CT=2] [N=2]	[T=1] [B=0] [R=0] [CB=2] [CT=2] [N=3]	[T=1] [B=0] [R=0] [CB=2] [CT=3] [N=0]	[T=1] [B=0] [R=0] [CB=2] [CT=3] [N=1]	[T=1] [B=0] [R=0] [CB=2] [CT=3] [N=2]	[T=1] [B=0] [R=0] [CB=2] [CT=3] [N=3]	[T=1] [B=0] [R=0] [CB=2] [CT=4] [N=0]	[T=1] [B=0] [R=0] [CB=2] [CT=4] [N=1]	[T=1] [B=0] [R=0] [CB=2] [CT=4] [N=2]	[T=1] [B=0] [R=0] [CB=2] [CT=4] [N=3]	[T=1] [B=0] [R=0] [CB=2] [CT=5] [N=0]	[T=1] [B=0] [R=0] [CB=2] [CT=5] [N=1]	[T=1] [B=0] [R=0] [CB=2] [CT=5] [N=2]	[T=1] [B=0] [R=0] [CB=2] [CT=5] [N=3]	[T=1] [B=0] [R=0] [CB=3] [CT=0] [N=0]	[T=1] [B=0] [R=0] [CB=3] [CT=0] [N=1]
R38	ct_coef															
	[T=1] [B=0] [R=0]	[T=1] [B=0] [R=0]	[T=1] [B=0] [R=0]	[T=1] [B=0] [R=0]	[T=1] [B=0] [R=0]	[T=1] [B=0] [R=0]	[T=1] [B=0] [R=0]	[T=1] [B=0] [R=0]	[T=1] [B=0] [R=0]	[T=1] [B=0] [R=0]	[T=1] [B=0] [R=0]	[T=1] [B=0] [R=0]	[T=1] [B=0] [R=0]	[T=1] [B=0] [R=0]	[T=1] [B=0] [R=0]	[T=1] [B=0] [R=0]

Rxxx Value 1 row = 1 Cacheline	16 32-bit counters															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	[CB=3] [CT=0] [N=2]	[CB=3] [CT=0] [N=3]	[CB=3] [CT=1] [N=0]	[CB=3] [CT=1] [N=1]	[CB=3] [CT=1] [N=2]	[CB=3] [CT=1] [N=3]	[CB=3] [CT=2] [N=0]	[CB=3] [CT=2] [N=1]	[CB=3] [CT=2] [N=2]	[CB=3] [CT=2] [N=3]	[CB=3] [CT=3] [N=0]	[CB=3] [CT=3] [N=1]	[CB=3] [CT=3] [N=2]	[CB=3] [CT=3] [N=3]	[CB=3] [CT=4] [N=0]	[CB=3] [CT=4] [N=1]
R39	ct_coef															
	[T=1] [B=0] [R=0] [CB=3] [CT=4] [N=2]	[T=1] [B=0] [R=0] [CB=3] [CT=4] [N=3]	[T=1] [B=0] [R=0] [CB=3] [CT=5] [N=0]	[T=1] [B=0] [R=0] [CB=3] [CT=5] [N=1]	[T=1] [B=0] [R=0] [CB=3] [CT=5] [N=2]	[T=1] [B=0] [R=0] [CB=3] [CT=5] [N=3]	[T=1] [B=0] [R=0] [CB=4] [CT=0] [N=0]	[T=1] [B=0] [R=0] [CB=4] [CT=0] [N=1]	[T=1] [B=0] [R=0] [CB=4] [CT=0] [N=2]	[T=1] [B=0] [R=0] [CB=4] [CT=0] [N=3]	[T=1] [B=0] [R=0] [CB=4] [CT=1] [N=0]	[T=1] [B=0] [R=0] [CB=4] [CT=1] [N=1]	[T=1] [B=0] [R=0] [CB=4] [CT=1] [N=2]	[T=1] [B=0] [R=0] [CB=4] [CT=1] [N=3]	[T=1] [B=0] [R=0] [CB=4] [CT=2] [N=0]	[T=1] [B=0] [R=0] [CB=4] [CT=2] [N=1]
R40	ct_coef															
	[T=1] [B=0] [R=0] [CB=4] [CT=2] [N=2]	[T=1] [B=0] [R=0] [CB=4] [CT=2] [N=3]	[T=1] [B=0] [R=0] [CB=4] [CT=3] [N=0]	[T=1] [B=0] [R=0] [CB=4] [CT=3] [N=1]	[T=1] [B=0] [R=0] [CB=4] [CT=3] [N=2]	[T=1] [B=0] [R=0] [CB=4] [CT=3] [N=3]	[T=1] [B=0] [R=0] [CB=4] [CT=4] [N=0]	[T=1] [B=0] [R=0] [CB=4] [CT=4] [N=1]	[T=1] [B=0] [R=0] [CB=4] [CT=4] [N=2]	[T=1] [B=0] [R=0] [CB=4] [CT=4] [N=3]	[T=1] [B=0] [R=0] [CB=4] [CT=5] [N=0]	[T=1] [B=0] [R=0] [CB=4] [CT=5] [N=1]	[T=1] [B=0] [R=0] [CB=4] [CT=5] [N=2]	[T=1] [B=0] [R=0] [CB=4] [CT=5] [N=3]	[T=1] [B=0] [R=0] [CB=5] [CT=0] [N=0]	[T=1] [B=0] [R=0] [CB=5] [CT=0] [N=1]
R41	ct_coef															
	[T=1] [B=0] [R=0] [CB=5] [CT=0]	[T=1] [B=0] [R=0] [CB=5]	[T=1] [B=0] [R=0] [CB=5]	[T=1] [B=0] [R=0] [CB=5]	[T=1] [B=0] [R=0] [CB=5]	[T=1] [B=0] [R=0] [CB=5]	[T=1] [B=0] [R=0] [CB=5]	[T=1] [B=0] [R=0] [CB=5]	[T=1] [B=0] [R=0] [CB=5]	[T=1] [B=0] [R=0] [CB=5]	[T=1] [B=0] [R=0] [CB=5]	[T=1] [B=0] [R=0] [CB=5]	[T=1] [B=0] [R=0] [CB=5]	[T=1] [B=0] [R=0] [CB=5]	[T=1] [B=0] [R=0] [CB=5]	[T=1] [B=0] [R=0] [CB=5] [CT=4]

Rxxx Value 1 row = 1 Cacheline	16 32-bit counters															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	[N=2]	[CT=0] [N=3]	[CT=1] [N=0]	[CT=1] [N=1]	[CT=1] [N=2]	[CT=1] [N=3]	[CT=2] [N=0]	[CT=2] [N=1]	[CT=2] [N=2]	[CT=2] [N=3]	[CT=3] [N=0]	[CT=3] [N=1]	[CT=3] [N=2]	[CT=3] [N=3]	[CT=4] [N=0]	[N=1]
R42	ct_coef															
	[T=1] [B=0] [R=0] [CB=5] [CT=4] [N=2]	[T=1] [B=0] [R=0] [CB=5] [CT=4] [N=3]	[T=1] [B=0] [R=0] [CB=5] [CT=5] [N=0]	[T=1] [B=0] [R=0] [CB=5] [CT=5] [N=1]	[T=1] [B=0] [R=0] [CB=5] [CT=5] [N=2]	[T=1] [B=0] [R=0] [CB=5] [CT=5] [N=3]	[T=1] [B=0] [R=1] [CB=0] [CT=0] [N=0]	[T=1] [B=0] [R=1] [CB=0] [CT=0] [N=1]	[T=1] [B=0] [R=1] [CB=0] [CT=0] [N=2]	[T=1] [B=0] [R=1] [CB=0] [CT=0] [N=3]	[T=1] [B=0] [R=1] [CB=0] [CT=1] [N=0]	[T=1] [B=0] [R=1] [CB=0] [CT=1] [N=1]	[T=1] [B=0] [R=1] [CB=0] [CT=1] [N=2]	[T=1] [B=0] [R=1] [CB=0] [CT=1] [N=3]	[T=1] [B=0] [R=1] [CB=0] [CT=2] [N=0]	[T=1] [B=0] [R=1] [CB=0] [CT=2] [N=1]
R43	ct_coef															
	[T=1] [B=0] [R=1] [CB=0] [CT=2] [N=2]	[T=1] [B=0] [R=1] [CB=0] [CT=2] [N=3]	[T=1] [B=0] [R=1] [CB=1] [CT=0] [N=0]	[T=1] [B=0] [R=1] [CB=1] [CT=0] [N=1]	[T=1] [B=0] [R=1] [CB=1] [CT=0] [N=2]	[T=1] [B=0] [R=1] [CB=1] [CT=0] [N=3]	[T=1] [B=0] [R=1] [CB=1] [CT=1] [N=0]	[T=1] [B=0] [R=1] [CB=1] [CT=1] [N=1]	[T=1] [B=0] [R=1] [CB=1] [CT=1] [N=2]	[T=1] [B=0] [R=1] [CB=1] [CT=1] [N=3]	[T=1] [B=0] [R=1] [CB=1] [CT=2] [N=0]	[T=1] [B=0] [R=1] [CB=1] [CT=2] [N=1]	[T=1] [B=0] [R=1] [CB=1] [CT=2] [N=2]	[T=1] [B=0] [R=1] [CB=1] [CT=2] [N=3]	[T=1] [B=0] [R=1] [CB=1] [CT=3] [N=0]	[T=1] [B=0] [R=1] [CB=1] [CT=3] [N=1]
R44	ct_coef															
	[T=1] [B=0] [R=1] [CB=1] [CT=3] [N=2]	[T=1] [B=0] [R=1] [CB=1] [CT=3]	[T=1] [B=0] [R=1] [CB=1] [CT=4]	[T=1] [B=0] [R=1] [CB=1] [CT=4]	[T=1] [B=0] [R=1] [CB=1] [CT=4]	[T=1] [B=0] [R=1] [CB=1] [CT=4]	[T=1] [B=0] [R=1] [CB=1] [CT=5]	[T=1] [B=0] [R=1] [CB=1] [CT=5]	[T=1] [B=0] [R=1] [CB=1] [CT=5]	[T=1] [B=0] [R=1] [CB=1] [CT=5]	[T=1] [B=0] [R=1] [CB=2] [CT=0] [N=0]	[T=1] [B=0] [R=1] [CB=2] [CT=0] [N=1]	[T=1] [B=0] [R=1] [CB=2] [CT=0]	[T=1] [B=0] [R=1] [CB=2] [CT=0]	[T=1] [B=0] [R=1] [CB=2] [CT=1]	[T=1] [B=0] [R=1] [CB=2] [CT=1] [N=1]

Rxxx Value 1 row = 1 Cacheline	16 32-bit counters															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		[N=3]	[N=0]	[N=1]	[N=2]	[N=3]	[N=0]	[N=1]	[N=2]	[N=3]			[N=2]	[N=3]	[N=0]	
R45	ct_coef															
	[T=1] [B=0] [R=1] [CB=2] [CT=1] [N=2]	[T=1] [B=0] [R=1] [CB=2] [CT=1] [N=3]	[T=1] [B=0] [R=1] [CB=2] [CT=2] [N=0]	[T=1] [B=0] [R=1] [CB=2] [CT=2] [N=1]	[T=1] [B=0] [R=1] [CB=2] [CT=2] [N=2]	[T=1] [B=0] [R=1] [CB=2] [CT=2] [N=3]	[T=1] [B=0] [R=1] [CB=2] [CT=3] [N=0]	[T=1] [B=0] [R=1] [CB=2] [CT=3] [N=1]	[T=1] [B=0] [R=1] [CB=2] [CT=3] [N=2]	[T=1] [B=0] [R=1] [CB=2] [CT=3] [N=3]	[T=1] [B=0] [R=1] [CB=2] [CT=4] [N=0]	[T=1] [B=0] [R=1] [CB=2] [CT=4] [N=1]	[T=1] [B=0] [R=1] [CB=2] [CT=4] [N=2]	[T=1] [B=0] [R=1] [CB=2] [CT=4] [N=3]	[T=1] [B=0] [R=1] [CB=2] [CT=5] [N=0]	[T=1] [B=0] [R=1] [CB=2] [CT=5] [N=1]
R46	ct_coef															
	[T=1] [B=0] [R=1] [CB=2] [CT=5] [N=2]	[T=1] [B=0] [R=1] [CB=2] [CT=5] [N=3]	[T=1] [B=0] [R=1] [CB=3] [CT=0] [N=0]	[T=1] [B=0] [R=1] [CB=3] [CT=0] [N=1]	[T=1] [B=0] [R=1] [CB=3] [CT=0] [N=2]	[T=1] [B=0] [R=1] [CB=3] [CT=0] [N=3]	[T=1] [B=0] [R=1] [CB=3] [CT=1] [N=0]	[T=1] [B=0] [R=1] [CB=3] [CT=1] [N=1]	[T=1] [B=0] [R=1] [CB=3] [CT=1] [N=2]	[T=1] [B=0] [R=1] [CB=3] [CT=1] [N=3]	[T=1] [B=0] [R=1] [CB=3] [CT=2] [N=0]	[T=1] [B=0] [R=1] [CB=3] [CT=2] [N=1]	[T=1] [B=0] [R=1] [CB=3] [CT=2] [N=2]	[T=1] [B=0] [R=1] [CB=3] [CT=2] [N=3]	[T=1] [B=0] [R=1] [CB=3] [CT=3] [N=0]	[T=1] [B=0] [R=1] [CB=3] [CT=3] [N=1]
R47	ct_coef															
	[T=1] [B=0] [R=1] [CB=3] [CT=3] [N=2]	[T=1] [B=0] [R=1] [CB=3] [CT=3] [N=3]	[T=1] [B=0] [R=1] [CB=3] [CT=4] [N=0]	[T=1] [B=0] [R=1] [CB=3] [CT=4] [N=1]	[T=1] [B=0] [R=1] [CB=3] [CT=4] [N=2]	[T=1] [B=0] [R=1] [CB=3] [CT=4] [N=3]	[T=1] [B=0] [R=1] [CB=3] [CT=5] [N=0]	[T=1] [B=0] [R=1] [CB=3] [CT=5] [N=1]	[T=1] [B=0] [R=1] [CB=3] [CT=5] [N=2]	[T=1] [B=0] [R=1] [CB=3] [CT=5] [N=3]	[T=1] [B=0] [R=1] [CB=4] [CT=0] [N=0]	[T=1] [B=0] [R=1] [CB=4] [CT=0] [N=1]	[T=1] [B=0] [R=1] [CB=4] [CT=0] [N=2]	[T=1] [B=0] [R=1] [CB=4] [CT=0] [N=3]	[T=1] [B=0] [R=1] [CB=4] [CT=1] [N=0]	[T=1] [B=0] [R=1] [CB=4] [CT=1] [N=1]
R48	ct_coef															

Rxxx Value 1 row = 1 Cacheline	16 32-bit counters															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	[T=1] [B=0] [R=1] [CB=4] [CT=1] [N=2]	[T=1] [B=0] [R=1] [CB=4] [CT=1] [N=3]	[T=1] [B=0] [R=1] [CB=4] [CT=2] [N=0]	[T=1] [B=0] [R=1] [CB=4] [CT=2] [N=1]	[T=1] [B=0] [R=1] [CB=4] [CT=2] [N=2]	[T=1] [B=0] [R=1] [CB=4] [CT=2] [N=3]	[T=1] [B=0] [R=1] [CB=4] [CT=3] [N=0]	[T=1] [B=0] [R=1] [CB=4] [CT=3] [N=1]	[T=1] [B=0] [R=1] [CB=4] [CT=3] [N=2]	[T=1] [B=0] [R=1] [CB=4] [CT=3] [N=3]	[T=1] [B=0] [R=1] [CB=4] [CT=4] [N=0]	[T=1] [B=0] [R=1] [CB=4] [CT=4] [N=1]	[T=1] [B=0] [R=1] [CB=4] [CT=4] [N=2]	[T=1] [B=0] [R=1] [CB=4] [CT=4] [N=3]	[T=1] [B=0] [R=1] [CB=4] [CT=5] [N=0]	[T=1] [B=0] [R=1] [CB=4] [CT=5] [N=1]
R49	ct_coef															
	[T=1] [B=0] [R=1] [CB=4] [CT=5] [N=2]	[T=1] [B=0] [R=1] [CB=4] [CT=5] [N=3]	[T=1] [B=0] [R=1] [CB=5] [CT=0] [N=0]	[T=1] [B=0] [R=1] [CB=5] [CT=0] [N=1]	[T=1] [B=0] [R=1] [CB=5] [CT=0] [N=2]	[T=1] [B=0] [R=1] [CB=5] [CT=0] [N=3]	[T=1] [B=0] [R=1] [CB=5] [CT=1] [N=0]	[T=1] [B=0] [R=1] [CB=5] [CT=1] [N=1]	[T=1] [B=0] [R=1] [CB=5] [CT=1] [N=2]	[T=1] [B=0] [R=1] [CB=5] [CT=1] [N=3]	[T=1] [B=0] [R=1] [CB=5] [CT=2] [N=0]	[T=1] [B=0] [R=1] [CB=5] [CT=2] [N=1]	[T=1] [B=0] [R=1] [CB=5] [CT=2] [N=2]	[T=1] [B=0] [R=1] [CB=5] [CT=2] [N=3]	[T=1] [B=0] [R=1] [CB=5] [CT=3] [N=0]	[T=1] [B=0] [R=1] [CB=5] [CT=3] [N=1]
R50	ct_coef															
	[T=1] [B=0] [R=1] [CB=5] [CT=3] [N=2]	[T=1] [B=0] [R=1] [CB=5] [CT=3] [N=3]	[T=1] [B=0] [R=1] [CB=5] [CT=4] [N=0]	[T=1] [B=0] [R=1] [CB=5] [CT=4] [N=1]	[T=1] [B=0] [R=1] [CB=5] [CT=4] [N=2]	[T=1] [B=0] [R=1] [CB=5] [CT=4] [N=3]	[T=1] [B=0] [R=1] [CB=5] [CT=5] [N=0]	[T=1] [B=0] [R=1] [CB=5] [CT=5] [N=1]	[T=1] [B=0] [R=1] [CB=5] [CT=5] [N=2]	[T=1] [B=0] [R=1] [CB=5] [CT=5] [N=3]	[T=1] [B=1] [R=0] [CB=0] [CT=0] [N=0]	[T=1] [B=1] [R=0] [CB=0] [CT=0] [N=1]	[T=1] [B=1] [R=0] [CB=0] [CT=0] [N=2]	[T=1] [B=1] [R=0] [CB=0] [CT=0] [N=3]	[T=1] [B=1] [R=0] [CB=0] [CT=1] [N=0]	[T=1] [B=1] [R=0] [CB=0] [CT=1] [N=1]
R51	ct_coef															
	[T=1] [B=1]	[T=1] [B=1]	[T=1] [B=1]	[T=1] [B=1]	[T=1] [B=1]	[T=1] [B=1]	[T=1] [B=1]	[T=1] [B=1]	[T=1] [B=1]	[T=1] [B=1]	[T=1] [B=1]	[T=1] [B=1]	[T=1] [B=1]	[T=1] [B=1]	[T=1] [B=1]	[T=1] [B=1]

Rxxx Value 1 row = 1 Cacheline	16 32-bit counters															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	[R=0] [CB=0] [CT=1] [N=2]	[R=0] [CB=0] [CT=1] [N=3]	[R=0] [CB=0] [CT=2] [N=0]	[R=0] [CB=0] [CT=2] [N=1]	[R=0] [CB=0] [CT=2] [N=2]	[R=0] [CB=0] [CT=2] [N=3]	[R=0] [CB=1] [CT=0] [N=0]	[R=0] [CB=1] [CT=0] [N=1]	[R=0] [CB=1] [CT=0] [N=2]	[R=0] [CB=1] [CT=0] [N=3]	[R=0] [CB=1] [CT=1] [N=0]	[R=0] [CB=1] [CT=1] [N=1]	[R=0] [CB=1] [CT=1] [N=2]	[R=0] [CB=1] [CT=1] [N=3]	[R=0] [CB=1] [CT=2] [N=0]	[R=0] [CB=1] [CT=2] [N=1]
R52	ct_coef															
	[T=1] [B=1] [R=0] [CB=1] [CT=2] [N=2]	[T=1] [B=1] [R=0] [CB=1] [CT=2] [N=3]	[T=1] [B=1] [R=0] [CB=1] [CT=3] [N=0]	[T=1] [B=1] [R=0] [CB=1] [CT=3] [N=1]	[T=1] [B=1] [R=0] [CB=1] [CT=3] [N=2]	[T=1] [B=1] [R=0] [CB=1] [CT=3] [N=3]	[T=1] [B=1] [R=0] [CB=1] [CT=4] [N=0]	[T=1] [B=1] [R=0] [CB=1] [CT=4] [N=1]	[T=1] [B=1] [R=0] [CB=1] [CT=4] [N=2]	[T=1] [B=1] [R=0] [CB=1] [CT=4] [N=3]	[T=1] [B=1] [R=0] [CB=1] [CT=5] [N=0]	[T=1] [B=1] [R=0] [CB=1] [CT=5] [N=1]	[T=1] [B=1] [R=0] [CB=1] [CT=5] [N=2]	[T=1] [B=1] [R=0] [CB=1] [CT=5] [N=3]	[T=1] [B=1] [R=0] [CB=2] [CT=0] [N=0]	[T=1] [B=1] [R=0] [CB=2] [CT=0] [N=1]
R53	ct_coef															
	[T=1] [B=1] [R=0] [CB=2] [CT=0] [N=2]	[T=1] [B=1] [R=0] [CB=2] [CT=0] [N=3]	[T=1] [B=1] [R=0] [CB=2] [CT=1] [N=0]	[T=1] [B=1] [R=0] [CB=2] [CT=1] [N=1]	[T=1] [B=1] [R=0] [CB=2] [CT=1] [N=2]	[T=1] [B=1] [R=0] [CB=2] [CT=1] [N=3]	[T=1] [B=1] [R=0] [CB=2] [CT=2] [N=0]	[T=1] [B=1] [R=0] [CB=2] [CT=2] [N=1]	[T=1] [B=1] [R=0] [CB=2] [CT=2] [N=2]	[T=1] [B=1] [R=0] [CB=2] [CT=2] [N=3]	[T=1] [B=1] [R=0] [CB=2] [CT=3] [N=0]	[T=1] [B=1] [R=0] [CB=2] [CT=3] [N=1]	[T=1] [B=1] [R=0] [CB=2] [CT=3] [N=2]	[T=1] [B=1] [R=0] [CB=2] [CT=3] [N=3]	[T=1] [B=1] [R=0] [CB=2] [CT=4] [N=0]	[T=1] [B=1] [R=0] [CB=2] [CT=4] [N=1]
R54	ct_coef															
	[T=1] [B=1] [R=0] [CB=2]	[T=1] [B=1] [R=0]	[T=1] [B=1] [R=0]	[T=1] [B=1] [R=0]	[T=1] [B=1] [R=0]	[T=1] [B=1] [R=0]	[T=1] [B=1] [R=0]	[T=1] [B=1] [R=0]	[T=1] [B=1] [R=0]	[T=1] [B=1] [R=0]	[T=1] [B=1] [R=0]	[T=1] [B=1] [R=0]	[T=1] [B=1] [R=0]	[T=1] [B=1] [R=0]	[T=1] [B=1] [R=0]	[T=1] [B=1] [R=0] [CB=3]

Rxxx Value 1 row = 1 Cacheline	16 32-bit counters															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	[CT=4] [N=2]	[CB=2] [CT=4] [N=3]	[CB=2] [CT=5] [N=0]	[CB=2] [CT=5] [N=1]	[CB=2] [CT=5] [N=2]	[CB=2] [CT=5] [N=3]	[CB=3] [CT=0] [N=0]	[CB=3] [CT=0] [N=1]	[CB=3] [CT=0] [N=2]	[CB=3] [CT=0] [N=3]	[CB=3] [CT=1] [N=0]	[CB=3] [CT=1] [N=1]	[CB=3] [CT=1] [N=2]	[CB=3] [CT=1] [N=3]	[CB=3] [CT=2] [N=0]	[CT=2] [N=1]
R55	ct_coef															
	[T=1] [B=1] [R=0] [CB=3] [CT=2] [N=2]	[T=1] [B=1] [R=0] [CB=3] [CT=2] [N=3]	[T=1] [B=1] [R=0] [CB=3] [CT=3] [N=0]	[T=1] [B=1] [R=0] [CB=3] [CT=3] [N=1]	[T=1] [B=1] [R=0] [CB=3] [CT=3] [N=2]	[T=1] [B=1] [R=0] [CB=3] [CT=3] [N=3]	[T=1] [B=1] [R=0] [CB=3] [CT=4] [N=0]	[T=1] [B=1] [R=0] [CB=3] [CT=4] [N=1]	[T=1] [B=1] [R=0] [CB=3] [CT=4] [N=2]	[T=1] [B=1] [R=0] [CB=3] [CT=4] [N=3]	[T=1] [B=1] [R=0] [CB=3] [CT=5] [N=0]	[T=1] [B=1] [R=0] [CB=3] [CT=5] [N=1]	[T=1] [B=1] [R=0] [CB=3] [CT=5] [N=2]	[T=1] [B=1] [R=0] [CB=3] [CT=5] [N=3]	[T=1] [B=1] [R=0] [CB=4] [CT=0] [N=0]	[T=1] [B=1] [R=0] [CB=4] [CT=0] [N=1]
R56	ct_coef															
	[T=1] [B=1] [R=0] [CB=4] [CT=0] [N=2]	[T=1] [B=1] [R=0] [CB=4] [CT=0] [N=3]	[T=1] [B=1] [R=0] [CB=4] [CT=1] [N=0]	[T=1] [B=1] [R=0] [CB=4] [CT=1] [N=1]	[T=1] [B=1] [R=0] [CB=4] [CT=1] [N=2]	[T=1] [B=1] [R=0] [CB=4] [CT=1] [N=3]	[T=1] [B=1] [R=0] [CB=4] [CT=2] [N=0]	[T=1] [B=1] [R=0] [CB=4] [CT=2] [N=1]	[T=1] [B=1] [R=0] [CB=4] [CT=2] [N=2]	[T=1] [B=1] [R=0] [CB=4] [CT=2] [N=3]	[T=1] [B=1] [R=0] [CB=4] [CT=3] [N=0]	[T=1] [B=1] [R=0] [CB=4] [CT=3] [N=1]	[T=1] [B=1] [R=0] [CB=4] [CT=3] [N=2]	[T=1] [B=1] [R=0] [CB=4] [CT=3] [N=3]	[T=1] [B=1] [R=0] [CB=4] [CT=4] [N=0]	[T=1] [B=1] [R=0] [CB=4] [CT=4] [N=1]
R57	ct_coef															
	[T=1] [B=1] [R=0] [CB=4] [CT=4] [N=2]	[T=1] [B=1] [R=0] [CB=4]	[T=1] [B=1] [R=0] [CB=4]	[T=1] [B=1] [R=0] [CB=4]	[T=1] [B=1] [R=0] [CB=4]	[T=1] [B=1] [R=0] [CB=4]	[T=1] [B=1] [R=0] [CB=5]	[T=1] [B=1] [R=0] [CB=5]	[T=1] [B=1] [R=0] [CB=5]	[T=1] [B=1] [R=0] [CB=5]	[T=1] [B=1] [R=0] [CB=5] [CT=1]	[T=1] [B=1] [R=0] [CB=5] [CT=1]	[T=1] [B=1] [R=0] [CB=5]	[T=1] [B=1] [R=0] [CB=5]	[T=1] [B=1] [R=0] [CB=5]	[T=1] [B=1] [R=0] [CB=5] [CT=2] [N=1]

Rxxx Value 1 row = 1 Cacheline	16 32-bit counters															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		[CT=4] [N=3]	[CT=5] [N=0]	[CT=5] [N=1]	[CT=5] [N=2]	[CT=5] [N=3]	[CT=0] [N=0]	[CT=0] [N=1]	[CT=0] [N=2]	[CT=0] [N=3]	[N=0]	[N=1]	[CT=1] [N=2]	[CT=1] [N=3]	[CT=2] [N=0]	
R58	ct_coef															
	[T=1] [B=1] [R=0] [CB=5] [CT=2] [N=2]	[T=1] [B=1] [R=0] [CB=5] [CT=2] [N=3]	[T=1] [B=1] [R=0] [CB=5] [CT=3] [N=0]	[T=1] [B=1] [R=0] [CB=5] [CT=3] [N=1]	[T=1] [B=1] [R=0] [CB=5] [CT=3] [N=2]	[T=1] [B=1] [R=0] [CB=5] [CT=3] [N=3]	[T=1] [B=1] [R=0] [CB=5] [CT=4] [N=0]	[T=1] [B=1] [R=0] [CB=5] [CT=4] [N=1]	[T=1] [B=1] [R=0] [CB=5] [CT=4] [N=2]	[T=1] [B=1] [R=0] [CB=5] [CT=4] [N=3]	[T=1] [B=1] [R=0] [CB=5] [CT=5] [N=0]	[T=1] [B=1] [R=0] [CB=5] [CT=5] [N=1]	[T=1] [B=1] [R=0] [CB=5] [CT=5] [N=2]	[T=1] [B=1] [R=0] [CB=5] [CT=5] [N=3]	[T=1] [B=1] [R=1] [CB=0] [CT=0] [N=0]	[T=1] [B=1] [R=1] [CB=0] [CT=0] [N=1]
R59	ct_coef															
	[T=1] [B=1] [R=1] [CB=0] [CT=0] [N=2]	[T=1] [B=1] [R=1] [CB=0] [CT=0] [N=3]	[T=1] [B=1] [R=1] [CB=0] [CT=1] [N=0]	[T=1] [B=1] [R=1] [CB=0] [CT=1] [N=1]	[T=1] [B=1] [R=1] [CB=0] [CT=1] [N=2]	[T=1] [B=1] [R=1] [CB=0] [CT=1] [N=3]	[T=1] [B=1] [R=1] [CB=0] [CT=2] [N=0]	[T=1] [B=1] [R=1] [CB=0] [CT=2] [N=1]	[T=1] [B=1] [R=1] [CB=0] [CT=2] [N=2]	[T=1] [B=1] [R=1] [CB=0] [CT=2] [N=3]	[T=1] [B=1] [R=1] [CB=1] [CT=0] [N=0]	[T=1] [B=1] [R=1] [CB=1] [CT=0] [N=1]	[T=1] [B=1] [R=1] [CB=1] [CT=0] [N=2]	[T=1] [B=1] [R=1] [CB=1] [CT=0] [N=3]	[T=1] [B=1] [R=1] [CB=1] [CT=1] [N=0]	[T=1] [B=1] [R=1] [CB=1] [CT=1] [N=1]
R60	ct_coef															
	[T=1] [B=1] [R=1] [CB=1] [CT=1] [N=2]	[T=1] [B=1] [R=1] [CB=1] [CT=1] [N=3]	[T=1] [B=1] [R=1] [CB=1] [CT=2] [N=0]	[T=1] [B=1] [R=1] [CB=1] [CT=2] [N=1]	[T=1] [B=1] [R=1] [CB=1] [CT=2] [N=2]	[T=1] [B=1] [R=1] [CB=1] [CT=2] [N=3]	[T=1] [B=1] [R=1] [CB=1] [CT=3] [N=0]	[T=1] [B=1] [R=1] [CB=1] [CT=3] [N=1]	[T=1] [B=1] [R=1] [CB=1] [CT=3] [N=2]	[T=1] [B=1] [R=1] [CB=1] [CT=3] [N=3]	[T=1] [B=1] [R=1] [CB=1] [CT=4] [N=0]	[T=1] [B=1] [R=1] [CB=1] [CT=4] [N=1]	[T=1] [B=1] [R=1] [CB=1] [CT=4] [N=2]	[T=1] [B=1] [R=1] [CB=1] [CT=4] [N=3]	[T=1] [B=1] [R=1] [CB=1] [CT=5] [N=0]	[T=1] [B=1] [R=1] [CB=1] [CT=5] [N=1]

Rxxx Value 1 row = 1 Cacheline	16 32-bit counters															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R61	ct_coef															
	[T=1] [B=1] [R=1] [CB=1] [CT=5] [N=2]	[T=1] [B=1] [R=1] [CB=1] [CT=5] [N=3]	[T=1] [B=1] [R=1] [CB=2] [CT=0] [N=0]	[T=1] [B=1] [R=1] [CB=2] [CT=0] [N=1]	[T=1] [B=1] [R=1] [CB=2] [CT=0] [N=2]	[T=1] [B=1] [R=1] [CB=2] [CT=0] [N=3]	[T=1] [B=1] [R=1] [CB=2] [CT=1] [N=0]	[T=1] [B=1] [R=1] [CB=2] [CT=1] [N=1]	[T=1] [B=1] [R=1] [CB=2] [CT=1] [N=2]	[T=1] [B=1] [R=1] [CB=2] [CT=1] [N=3]	[T=1] [B=1] [R=1] [CB=2] [CT=2] [N=0]	[T=1] [B=1] [R=1] [CB=2] [CT=2] [N=1]	[T=1] [B=1] [R=1] [CB=2] [CT=2] [N=2]	[T=1] [B=1] [R=1] [CB=2] [CT=2] [N=3]	[T=1] [B=1] [R=1] [CB=2] [CT=3] [N=0]	[T=1] [B=1] [R=1] [CB=2] [CT=3] [N=1]
R62	ct_coef															
	[T=1] [B=1] [R=1] [CB=2] [CT=3] [N=2]	[T=1] [B=1] [R=1] [CB=2] [CT=3] [N=3]	[T=1] [B=1] [R=1] [CB=2] [CT=4] [N=0]	[T=1] [B=1] [R=1] [CB=2] [CT=4] [N=1]	[T=1] [B=1] [R=1] [CB=2] [CT=4] [N=2]	[T=1] [B=1] [R=1] [CB=2] [CT=4] [N=3]	[T=1] [B=1] [R=1] [CB=2] [CT=5] [N=0]	[T=1] [B=1] [R=1] [CB=2] [CT=5] [N=1]	[T=1] [B=1] [R=1] [CB=2] [CT=5] [N=2]	[T=1] [B=1] [R=1] [CB=2] [CT=5] [N=3]	[T=1] [B=1] [R=1] [CB=3] [CT=0] [N=0]	[T=1] [B=1] [R=1] [CB=3] [CT=0] [N=1]	[T=1] [B=1] [R=1] [CB=3] [CT=0] [N=2]	[T=1] [B=1] [R=1] [CB=3] [CT=0] [N=3]	[T=1] [B=1] [R=1] [CB=3] [CT=1] [N=0]	[T=1] [B=1] [R=1] [CB=3] [CT=1] [N=1]
R63	ct_coef															
	[T=1] [B=1] [R=1] [CB=3] [CT=1] [N=2]	[T=1] [B=1] [R=1] [CB=3] [CT=1] [N=3]	[T=1] [B=1] [R=1] [CB=3] [CT=2] [N=0]	[T=1] [B=1] [R=1] [CB=3] [CT=2] [N=1]	[T=1] [B=1] [R=1] [CB=3] [CT=2] [N=2]	[T=1] [B=1] [R=1] [CB=3] [CT=2] [N=3]	[T=1] [B=1] [R=1] [CB=3] [CT=3] [N=0]	[T=1] [B=1] [R=1] [CB=3] [CT=3] [N=1]	[T=1] [B=1] [R=1] [CB=3] [CT=3] [N=2]	[T=1] [B=1] [R=1] [CB=3] [CT=3] [N=3]	[T=1] [B=1] [R=1] [CB=3] [CT=4] [N=0]	[T=1] [B=1] [R=1] [CB=3] [CT=4] [N=1]	[T=1] [B=1] [R=1] [CB=3] [CT=4] [N=2]	[T=1] [B=1] [R=1] [CB=3] [CT=4] [N=3]	[T=1] [B=1] [R=1] [CB=3] [CT=5] [N=0]	[T=1] [B=1] [R=1] [CB=3] [CT=5] [N=1]
R64	ct_coef															
	[T=1]	[T=1]	[T=1]	[T=1]	[T=1]	[T=1]	[T=1]	[T=1]	[T=1]	[T=1]	[T=1]	[T=1]	[T=1]	[T=1]	[T=1]	[T=1]

Rxxx Value 1 row = 1 Cacheline	16 32-bit counters															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	[B=1] [R=1] [CB=3] [CT=5] [N=2]	[B=1] [R=1] [CB=3] [CT=5] [N=3]	[B=1] [R=1] [CB=4] [CT=0] [N=0]	[B=1] [R=1] [CB=4] [CT=0] [N=1]	[B=1] [R=1] [CB=4] [CT=0] [N=2]	[B=1] [R=1] [CB=4] [CT=0] [N=3]	[B=1] [R=1] [CB=4] [CT=1] [N=0]	[B=1] [R=1] [CB=4] [CT=1] [N=1]	[B=1] [R=1] [CB=4] [CT=1] [N=2]	[B=1] [R=1] [CB=4] [CT=1] [N=3]	[B=1] [R=1] [CB=4] [CT=2] [N=0]	[B=1] [R=1] [CB=4] [CT=2] [N=1]	[B=1] [R=1] [CB=4] [CT=2] [N=2]	[B=1] [R=1] [CB=4] [CT=2] [N=3]	[B=1] [R=1] [CB=4] [CT=3] [N=0]	[B=1] [R=1] [CB=4] [CT=3] [N=1]
R65	ct_coef															
	[T=1] [B=1] [R=1] [CB=4] [CT=3] [N=2]	[T=1] [B=1] [R=1] [CB=4] [CT=3] [N=3]	[T=1] [B=1] [R=1] [CB=4] [CT=4] [N=0]	[T=1] [B=1] [R=1] [CB=4] [CT=4] [N=1]	[T=1] [B=1] [R=1] [CB=4] [CT=4] [N=2]	[T=1] [B=1] [R=1] [CB=4] [CT=4] [N=3]	[T=1] [B=1] [R=1] [CB=4] [CT=5] [N=0]	[T=1] [B=1] [R=1] [CB=4] [CT=5] [N=1]	[T=1] [B=1] [R=1] [CB=4] [CT=5] [N=2]	[T=1] [B=1] [R=1] [CB=4] [CT=5] [N=3]	[T=1] [B=1] [R=1] [CB=5] [CT=0] [N=0]	[T=1] [B=1] [R=1] [CB=5] [CT=0] [N=1]	[T=1] [B=1] [R=1] [CB=5] [CT=0] [N=2]	[T=1] [B=1] [R=1] [CB=5] [CT=0] [N=3]	[T=1] [B=1] [R=1] [CB=5] [CT=1] [N=0]	[T=1] [B=1] [R=1] [CB=5] [CT=1] [N=1]
R66	ct_coef															
	[T=1] [B=1] [R=1] [CB=5] [CT=1] [N=2]	[T=1] [B=1] [R=1] [CB=5] [CT=1] [N=3]	[T=1] [B=1] [R=1] [CB=5] [CT=2] [N=0]	[T=1] [B=1] [R=1] [CB=5] [CT=2] [N=1]	[T=1] [B=1] [R=1] [CB=5] [CT=2] [N=2]	[T=1] [B=1] [R=1] [CB=5] [CT=2] [N=3]	[T=1] [B=1] [R=1] [CB=5] [CT=3] [N=0]	[T=1] [B=1] [R=1] [CB=5] [CT=3] [N=1]	[T=1] [B=1] [R=1] [CB=5] [CT=3] [N=2]	[T=1] [B=1] [R=1] [CB=5] [CT=3] [N=3]	[T=1] [B=1] [R=1] [CB=5] [CT=4] [N=0]	[T=1] [B=1] [R=1] [CB=5] [CT=4] [N=1]	[T=1] [B=1] [R=1] [CB=5] [CT=4] [N=2]	[T=1] [B=1] [R=1] [CB=5] [CT=4] [N=3]	[T=1] [B=1] [R=1] [CB=5] [CT=5] [N=0]	[T=1] [B=1] [R=1] [CB=5] [CT=5] [N=1]
R67	ct_coef															
	[T=1] [B=1] [R=1]	[T=1] [B=1] [R=1]	[T=2] [B=0] [R=0]	[T=2] [B=0] [R=0]	[T=2] [B=0] [R=0]	[T=2] [B=0] [R=0]	[T=2] [B=0] [R=0]	[T=2] [B=0] [R=0]	[T=2] [B=0] [R=0]	[T=2] [B=0] [R=0]	[T=2] [B=0] [R=0]	[T=2] [B=0] [R=0]	[T=2] [B=0] [R=0]	[T=2] [B=0] [R=0]	[T=2] [B=0] [R=0]	[T=2] [B=0] [R=0]

Rxxx Value 1 row = 1 Cacheline	**16 32-bit counters**															
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**
	[CB=5] [CT=5] [N=2]	[CB=5] [CT=5] [N=3]	[CB=0] [CT=0] [N=0]	[CB=0] [CT=0] [N=1]	[CB=0] [CT=0] [N=2]	[CB=0] [CT=0] [N=3]	[CB=0] [CT=1] [N=0]	[CB=0] [CT=1] [N=1]	[CB=0] [CT=1] [N=2]	[CB=0] [CT=1] [N=3]	[CB=0] [CT=2] [N=0]	[CB=0] [CT=2] [N=1]	[CB=0] [CT=2] [N=2]	[CB=0] [CT=2] [N=3]	[CB=1] [CT=0] [N=0]	[CB=1] [CT=0] [N=1]
R68	ct_coef															
	[T=2] [B=0] [R=0] [CB=1] [CT=0] [N=2]	[T=2] [B=0] [R=0] [CB=1] [CT=0] [N=3]	[T=2] [B=0] [R=0] [CB=1] [CT=1] [N=0]	[T=2] [B=0] [R=0] [CB=1] [CT=1] [N=1]	[T=2] [B=0] [R=0] [CB=1] [CT=1] [N=2]	[T=2] [B=0] [R=0] [CB=1] [CT=1] [N=3]	[T=2] [B=0] [R=0] [CB=1] [CT=2] [N=0]	[T=2] [B=0] [R=0] [CB=1] [CT=2] [N=1]	[T=2] [B=0] [R=0] [CB=1] [CT=2] [N=2]	[T=2] [B=0] [R=0] [CB=1] [CT=2] [N=3]	[T=2] [B=0] [R=0] [CB=1] [CT=3] [N=0]	[T=2] [B=0] [R=0] [CB=1] [CT=3] [N=1]	[T=2] [B=0] [R=0] [CB=1] [CT=3] [N=2]	[T=2] [B=0] [R=0] [CB=1] [CT=3] [N=3]	[T=2] [B=0] [R=0] [CB=1] [CT=4] [N=0]	[T=2] [B=0] [R=0] [CB=1] [CT=4] [N=1]
R69	ct_coef															
	[T=2] [B=0] [R=0] [CB=1] [CT=4] [N=2]	[T=2] [B=0] [R=0] [CB=1] [CT=4] [N=3]	[T=2] [B=0] [R=0] [CB=1] [CT=5] [N=0]	[T=2] [B=0] [R=0] [CB=1] [CT=5] [N=1]	[T=2] [B=0] [R=0] [CB=1] [CT=5] [N=2]	[T=2] [B=0] [R=0] [CB=1] [CT=5] [N=3]	[T=2] [B=0] [R=0] [CB=2] [CT=0] [N=0]	[T=2] [B=0] [R=0] [CB=2] [CT=0] [N=1]	[T=2] [B=0] [R=0] [CB=2] [CT=0] [N=2]	[T=2] [B=0] [R=0] [CB=2] [CT=0] [N=3]	[T=2] [B=0] [R=0] [CB=2] [CT=1] [N=0]	[T=2] [B=0] [R=0] [CB=2] [CT=1] [N=1]	[T=2] [B=0] [R=0] [CB=2] [CT=1] [N=2]	[T=2] [B=0] [R=0] [CB=2] [CT=1] [N=3]	[T=2] [B=0] [R=0] [CB=2] [CT=2] [N=0]	[T=2] [B=0] [R=0] [CB=2] [CT=2] [N=1]
R70	ct_coef															
	[T=2] [B=0] [R=0] [CB=2] [CT=2]	[T=2] [B=0] [R=0] [CB=2]	[T=2] [B=0] [R=0] [CB=2]	[T=2] [B=0] [R=0] [CB=2]	[T=2] [B=0] [R=0] [CB=2]	[T=2] [B=0] [R=0] [CB=2]	[T=2] [B=0] [R=0] [CB=2]	[T=2] [B=0] [R=0] [CB=2]	[T=2] [B=0] [R=0] [CB=2]	[T=2] [B=0] [R=0] [CB=2]	[T=2] [B=0] [R=0] [CB=2]	[T=2] [B=0] [R=0] [CB=2]	[T=2] [B=0] [R=0] [CB=2]	[T=2] [B=0] [R=0] [CB=2]	[T=2] [B=0] [R=0] [CB=3]	[T=2] [B=0] [R=0] [CB=3] [CT=0]

Rxxx Value 1 row = 1 Cacheline	16 32-bit counters															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	[N=2]	[CT=2] [N=3]	[CT=3] [N=0]	[CT=3] [N=1]	[CT=3] [N=2]	[CT=3] [N=3]	[CT=4] [N=0]	[CT=4] [N=1]	[CT=4] [N=2]	[CT=4] [N=3]	[CT=5] [N=0]	[CT=5] [N=1]	[CT=5] [N=2]	[CT=5] [N=3]	[CT=0] [N=0]	[N=1]
R71	ct_coef															
	[T=2] [B=0] [R=0] [CB=3] [CT=0] [N=2]	[T=2] [B=0] [R=0] [CB=3] [CT=0] [N=3]	[T=2] [B=0] [R=0] [CB=3] [CT=1] [N=0]	[T=2] [B=0] [R=0] [CB=3] [CT=1] [N=1]	[T=2] [B=0] [R=0] [CB=3] [CT=1] [N=2]	[T=2] [B=0] [R=0] [CB=3] [CT=1] [N=3]	[T=2] [B=0] [R=0] [CB=3] [CT=2] [N=0]	[T=2] [B=0] [R=0] [CB=3] [CT=2] [N=1]	[T=2] [B=0] [R=0] [CB=3] [CT=2] [N=2]	[T=2] [B=0] [R=0] [CB=3] [CT=2] [N=3]	[T=2] [B=0] [R=0] [CB=3] [CT=3] [N=0]	[T=2] [B=0] [R=0] [CB=3] [CT=3] [N=1]	[T=2] [B=0] [R=0] [CB=3] [CT=3] [N=2]	[T=2] [B=0] [R=0] [CB=3] [CT=3] [N=3]	[T=2] [B=0] [R=0] [CB=3] [CT=4] [N=0]	[T=2] [B=0] [R=0] [CB=3] [CT=4] [N=1]
R72	ct_coef															
	[T=2] [B=0] [R=0] [CB=3] [CT=4] [N=2]	[T=2] [B=0] [R=0] [CB=3] [CT=4] [N=3]	[T=2] [B=0] [R=0] [CB=3] [CT=5] [N=0]	[T=2] [B=0] [R=0] [CB=3] [CT=5] [N=1]	[T=2] [B=0] [R=0] [CB=3] [CT=5] [N=2]	[T=2] [B=0] [R=0] [CB=3] [CT=5] [N=3]	[T=2] [B=0] [R=0] [CB=4] [CT=0] [N=0]	[T=2] [B=0] [R=0] [CB=4] [CT=0] [N=1]	[T=2] [B=0] [R=0] [CB=4] [CT=0] [N=2]	[T=2] [B=0] [R=0] [CB=4] [CT=0] [N=3]	[T=2] [B=0] [R=0] [CB=4] [CT=1] [N=0]	[T=2] [B=0] [R=0] [CB=4] [CT=1] [N=1]	[T=2] [B=0] [R=0] [CB=4] [CT=1] [N=2]	[T=2] [B=0] [R=0] [CB=4] [CT=1] [N=3]	[T=2] [B=0] [R=0] [CB=4] [CT=2] [N=0]	[T=2] [B=0] [R=0] [CB=4] [CT=2] [N=1]
R73	ct_coef															
	[T=2] [B=0] [R=0] [CB=4] [CT=2] [N=2]	[T=2] [B=0] [R=0] [CB=4] [CT=2]	[T=2] [B=0] [R=0] [CB=4] [CT=3]	[T=2] [B=0] [R=0] [CB=4] [CT=3]	[T=2] [B=0] [R=0] [CB=4] [CT=3]	[T=2] [B=0] [R=0] [CB=4] [CT=3]	[T=2] [B=0] [R=0] [CB=4] [CT=4]	[T=2] [B=0] [R=0] [CB=4] [CT=4]	[T=2] [B=0] [R=0] [CB=4] [CT=4]	[T=2] [B=0] [R=0] [CB=4] [CT=4]	[T=2] [B=0] [R=0] [CB=4] [CT=5] [N=0]	[T=2] [B=0] [R=0] [CB=4] [CT=5] [N=1]	[T=2] [B=0] [R=0] [CB=4] [CT=5]	[T=2] [B=0] [R=0] [CB=4] [CT=5]	[T=2] [B=0] [R=0] [CB=5] [CT=0]	[T=2] [B=0] [R=0] [CB=5] [CT=0] [N=1]

Rxxx Value 1 row = 1 Cacheline	16 32-bit counters															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		[N=3]	[N=0]	[N=1]	[N=2]	[N=3]	[N=0]	[N=1]	[N=2]	[N=3]			[N=2]	[N=3]	[N=0]	
R74	ct_coef															
	[T=2] [B=0] [R=0] [CB=5] [CT=0] [N=2]	[T=2] [B=0] [R=0] [CB=5] [CT=0] [N=3]	[T=2] [B=0] [R=0] [CB=5] [CT=1] [N=0]	[T=2] [B=0] [R=0] [CB=5] [CT=1] [N=1]	[T=2] [B=0] [R=0] [CB=5] [CT=1] [N=2]	[T=2] [B=0] [R=0] [CB=5] [CT=1] [N=3]	[T=2] [B=0] [R=0] [CB=5] [CT=2] [N=0]	[T=2] [B=0] [R=0] [CB=5] [CT=2] [N=1]	[T=2] [B=0] [R=0] [CB=5] [CT=2] [N=2]	[T=2] [B=0] [R=0] [CB=5] [CT=2] [N=3]	[T=2] [B=0] [R=0] [CB=5] [CT=3] [N=0]	[T=2] [B=0] [R=0] [CB=5] [CT=3] [N=1]	[T=2] [B=0] [R=0] [CB=5] [CT=3] [N=2]	[T=2] [B=0] [R=0] [CB=5] [CT=3] [N=3]	[T=2] [B=0] [R=0] [CB=5] [CT=4] [N=0]	[T=2] [B=0] [R=0] [CB=5] [CT=4] [N=1]
R75	ct_coef															
	[T=2] [B=0] [R=0] [CB=5] [CT=4] [N=2]	[T=2] [B=0] [R=0] [CB=5] [CT=4] [N=3]	[T=2] [B=0] [R=0] [CB=5] [CT=5] [N=0]	[T=2] [B=0] [R=0] [CB=5] [CT=5] [N=1]	[T=2] [B=0] [R=0] [CB=5] [CT=5] [N=2]	[T=2] [B=0] [R=0] [CB=5] [CT=5] [N=3]	[T=2] [B=0] [R=1] [CB=0] [CT=0] [N=0]	[T=2] [B=0] [R=1] [CB=0] [CT=0] [N=1]	[T=2] [B=0] [R=1] [CB=0] [CT=0] [N=2]	[T=2] [B=0] [R=1] [CB=0] [CT=0] [N=3]	[T=2] [B=0] [R=1] [CB=0] [CT=1] [N=0]	[T=2] [B=0] [R=1] [CB=0] [CT=1] [N=1]	[T=2] [B=0] [R=1] [CB=0] [CT=1] [N=2]	[T=2] [B=0] [R=1] [CB=0] [CT=1] [N=3]	[T=2] [B=0] [R=1] [CB=0] [CT=2] [N=0]	[T=2] [B=0] [R=1] [CB=0] [CT=2] [N=1]
R76	ct_coef															
	[T=2] [B=0] [R=1] [CB=0] [CT=2] [N=2]	[T=2] [B=0] [R=1] [CB=0] [CT=2] [N=3]	[T=2] [B=0] [R=1] [CB=1] [CT=0] [N=0]	[T=2] [B=0] [R=1] [CB=1] [CT=0] [N=1]	[T=2] [B=0] [R=1] [CB=1] [CT=0] [N=2]	[T=2] [B=0] [R=1] [CB=1] [CT=0] [N=3]	[T=2] [B=0] [R=1] [CB=1] [CT=1] [N=0]	[T=2] [B=0] [R=1] [CB=1] [CT=1] [N=1]	[T=2] [B=0] [R=1] [CB=1] [CT=1] [N=2]	[T=2] [B=0] [R=1] [CB=1] [CT=1] [N=3]	[T=2] [B=0] [R=1] [CB=1] [CT=2] [N=0]	[T=2] [B=0] [R=1] [CB=1] [CT=2] [N=1]	[T=2] [B=0] [R=1] [CB=1] [CT=2] [N=2]	[T=2] [B=0] [R=1] [CB=1] [CT=2] [N=3]	[T=2] [B=0] [R=1] [CB=1] [CT=3] [N=0]	[T=2] [B=0] [R=1] [CB=1] [CT=3] [N=1]
R77	ct_coef															

Rxxx Value 1 row = 1 Cacheline	16 32-bit counters															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	[T=2] [B=0] [R=1] [CB=1] [CT=3] [N=2]	[T=2] [B=0] [R=1] [CB=1] [CT=3] [N=3]	[T=2] [B=0] [R=1] [CB=1] [CT=4] [N=0]	[T=2] [B=0] [R=1] [CB=1] [CT=4] [N=1]	[T=2] [B=0] [R=1] [CB=1] [CT=4] [N=2]	[T=2] [B=0] [R=1] [CB=1] [CT=4] [N=3]	[T=2] [B=0] [R=1] [CB=1] [CT=5] [N=0]	[T=2] [B=0] [R=1] [CB=1] [CT=5] [N=1]	[T=2] [B=0] [R=1] [CB=1] [CT=5] [N=2]	[T=2] [B=0] [R=1] [CB=1] [CT=5] [N=3]	[T=2] [B=0] [R=1] [CB=2] [CT=0] [N=0]	[T=2] [B=0] [R=1] [CB=2] [CT=0] [N=1]	[T=2] [B=0] [R=1] [CB=2] [CT=0] [N=2]	[T=2] [B=0] [R=1] [CB=2] [CT=0] [N=3]	[T=2] [B=0] [R=1] [CB=2] [CT=1] [N=0]	[T=2] [B=0] [R=1] [CB=2] [CT=1] [N=1]
R78	ct_coef															
	[T=2] [B=0] [R=1] [CB=2] [CT=1] [N=2]	[T=2] [B=0] [R=1] [CB=2] [CT=1] [N=3]	[T=2] [B=0] [R=1] [CB=2] [CT=2] [N=0]	[T=2] [B=0] [R=1] [CB=2] [CT=2] [N=1]	[T=2] [B=0] [R=1] [CB=2] [CT=2] [N=2]	[T=2] [B=0] [R=1] [CB=2] [CT=2] [N=3]	[T=2] [B=0] [R=1] [CB=2] [CT=3] [N=0]	[T=2] [B=0] [R=1] [CB=2] [CT=3] [N=1]	[T=2] [B=0] [R=1] [CB=2] [CT=3] [N=2]	[T=2] [B=0] [R=1] [CB=2] [CT=3] [N=3]	[T=2] [B=0] [R=1] [CB=2] [CT=4] [N=0]	[T=2] [B=0] [R=1] [CB=2] [CT=4] [N=1]	[T=2] [B=0] [R=1] [CB=2] [CT=4] [N=2]	[T=2] [B=0] [R=1] [CB=2] [CT=4] [N=3]	[T=2] [B=0] [R=1] [CB=2] [CT=5] [N=0]	[T=2] [B=0] [R=1] [CB=2] [CT=5] [N=1]
R79	ct_coef															
	[T=2] [B=0] [R=1] [CB=2] [CT=5] [N=2]	[T=2] [B=0] [R=1] [CB=2] [CT=5] [N=3]	[T=2] [B=0] [R=1] [CB=3] [CT=0] [N=0]	[T=2] [B=0] [R=1] [CB=3] [CT=0] [N=1]	[T=2] [B=0] [R=1] [CB=3] [CT=0] [N=2]	[T=2] [B=0] [R=1] [CB=3] [CT=0] [N=3]	[T=2] [B=0] [R=1] [CB=3] [CT=1] [N=0]	[T=2] [B=0] [R=1] [CB=3] [CT=1] [N=1]	[T=2] [B=0] [R=1] [CB=3] [CT=1] [N=2]	[T=2] [B=0] [R=1] [CB=3] [CT=1] [N=3]	[T=2] [B=0] [R=1] [CB=3] [CT=2] [N=0]	[T=2] [B=0] [R=1] [CB=3] [CT=2] [N=1]	[T=2] [B=0] [R=1] [CB=3] [CT=2] [N=2]	[T=2] [B=0] [R=1] [CB=3] [CT=2] [N=3]	[T=2] [B=0] [R=1] [CB=3] [CT=3] [N=0]	[T=2] [B=0] [R=1] [CB=3] [CT=3] [N=1]
R80	ct_coef															
	[T=2] [B=0]	[T=2] [B=0]	[T=2] [B=0]	[T=2] [B=0]	[T=2] [B=0]	[T=2] [B=0]	[T=2] [B=0]	[T=2] [B=0]	[T=2] [B=0]	[T=2] [B=0]	[T=2] [B=0]	[T=2] [B=0]	[T=2] [B=0]	[T=2] [B=0]	[T=2] [B=0]	[T=2] [B=0]

Rxxx Value 1 row = 1 Cacheline	16 32-bit counters															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	[R=1] [CB=3] [CT=3] [N=2]	[R=1] [CB=3] [CT=3] [N=3]	[R=1] [CB=3] [CT=4] [N=0]	[R=1] [CB=3] [CT=4] [N=1]	[R=1] [CB=3] [CT=4] [N=2]	[R=1] [CB=3] [CT=4] [N=3]	[R=1] [CB=3] [CT=5] [N=0]	[R=1] [CB=3] [CT=5] [N=1]	[R=1] [CB=3] [CT=5] [N=2]	[R=1] [CB=3] [CT=5] [N=3]	[R=1] [CB=4] [CT=0] [N=0]	[R=1] [CB=4] [CT=0] [N=1]	[R=1] [CB=4] [CT=0] [N=2]	[R=1] [CB=4] [CT=0] [N=3]	[R=1] [CB=4] [CT=1] [N=0]	[R=1] [CB=4] [CT=1] [N=1]
R81	ct_coef															
	[T=2] [B=0] [R=1] [CB=4] [CT=1] [N=2]	[T=2] [B=0] [R=1] [CB=4] [CT=1] [N=3]	[T=2] [B=0] [R=1] [CB=4] [CT=2] [N=0]	[T=2] [B=0] [R=1] [CB=4] [CT=2] [N=1]	[T=2] [B=0] [R=1] [CB=4] [CT=2] [N=2]	[T=2] [B=0] [R=1] [CB=4] [CT=2] [N=3]	[T=2] [B=0] [R=1] [CB=4] [CT=3] [N=0]	[T=2] [B=0] [R=1] [CB=4] [CT=3] [N=1]	[T=2] [B=0] [R=1] [CB=4] [CT=3] [N=2]	[T=2] [B=0] [R=1] [CB=4] [CT=3] [N=3]	[T=2] [B=0] [R=1] [CB=4] [CT=4] [N=0]	[T=2] [B=0] [R=1] [CB=4] [CT=4] [N=1]	[T=2] [B=0] [R=1] [CB=4] [CT=4] [N=2]	[T=2] [B=0] [R=1] [CB=4] [CT=4] [N=3]	[T=2] [B=0] [R=1] [CB=4] [CT=5] [N=0]	[T=2] [B=0] [R=1] [CB=4] [CT=5] [N=1]
R82	ct_coef															
	[T=2] [B=0] [R=1] [CB=4] [CT=5] [N=2]	[T=2] [B=0] [R=1] [CB=4] [CT=5] [N=3]	[T=2] [B=0] [R=1] [CB=5] [CT=0] [N=0]	[T=2] [B=0] [R=1] [CB=5] [CT=0] [N=1]	[T=2] [B=0] [R=1] [CB=5] [CT=0] [N=2]	[T=2] [B=0] [R=1] [CB=5] [CT=0] [N=3]	[T=2] [B=0] [R=1] [CB=5] [CT=1] [N=0]	[T=2] [B=0] [R=1] [CB=5] [CT=1] [N=1]	[T=2] [B=0] [R=1] [CB=5] [CT=1] [N=2]	[T=2] [B=0] [R=1] [CB=5] [CT=1] [N=3]	[T=2] [B=0] [R=1] [CB=5] [CT=2] [N=0]	[T=2] [B=0] [R=1] [CB=5] [CT=2] [N=1]	[T=2] [B=0] [R=1] [CB=5] [CT=2] [N=2]	[T=2] [B=0] [R=1] [CB=5] [CT=2] [N=3]	[T=2] [B=0] [R=1] [CB=5] [CT=3] [N=0]	[T=2] [B=0] [R=1] [CB=5] [CT=3] [N=1]
R83	ct_coef															
	[T=2] [B=0] [R=1] [CB=5]	[T=2] [B=0] [R=1]	[T=2] [B=0] [R=1]	[T=2] [B=0] [R=1]	[T=2] [B=0] [R=1]	[T=2] [B=0] [R=1]	[T=2] [B=0] [R=1]	[T=2] [B=0] [R=1]	[T=2] [B=0] [R=1]	[T=2] [B=0] [R=1]	[T=2] [B=1] [R=0]	[T=2] [B=1] [R=0]	[T=2] [B=1] [R=0]	[T=2] [B=1] [R=0]	[T=2] [B=1] [R=0]	[T=2] [B=1] [R=0] [CB=0]

Rxxx Value 1 row = 1 Cacheline	16 32-bit counters															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	[CT=3] [N=2]	[CB=5] [CT=3] [N=3]	[CB=5] [CT=4] [N=0]	[CB=5] [CT=4] [N=1]	[CB=5] [CT=4] [N=2]	[CB=5] [CT=4] [N=3]	[CB=5] [CT=5] [N=0]	[CB=5] [CT=5] [N=1]	[CB=5] [CT=5] [N=2]	[CB=5] [CT=5] [N=3]	[CB=0] [CT=0] [N=0]	[CB=0] [CT=0] [N=1]	[CB=0] [CT=0] [N=2]	[CB=0] [CT=0] [N=3]	[CB=0] [CT=1] [N=0]	[CT=1] [N=1]
R84	ct_coef															
	[T=2] [B=1] [R=0] [CB=0] [CT=1] [N=2]	[T=2] [B=1] [R=0] [CB=0] [CT=1] [N=3]	[T=2] [B=1] [R=0] [CB=0] [CT=2] [N=0]	[T=2] [B=1] [R=0] [CB=0] [CT=2] [N=1]	[T=2] [B=1] [R=0] [CB=0] [CT=2] [N=2]	[T=2] [B=1] [R=0] [CB=0] [CT=2] [N=3]	[T=2] [B=1] [R=0] [CB=1] [CT=0] [N=0]	[T=2] [B=1] [R=0] [CB=1] [CT=0] [N=1]	[T=2] [B=1] [R=0] [CB=1] [CT=0] [N=2]	[T=2] [B=1] [R=0] [CB=1] [CT=0] [N=3]	[T=2] [B=1] [R=0] [CB=1] [CT=1] [N=0]	[T=2] [B=1] [R=0] [CB=1] [CT=1] [N=1]	[T=2] [B=1] [R=0] [CB=1] [CT=1] [N=2]	[T=2] [B=1] [R=0] [CB=1] [CT=1] [N=3]	[T=2] [B=1] [R=0] [CB=1] [CT=2] [N=0]	[T=2] [B=1] [R=0] [CB=1] [CT=2] [N=1]
R85	ct_coef															
	[T=2] [B=1] [R=0] [CB=1] [CT=2] [N=2]	[T=2] [B=1] [R=0] [CB=1] [CT=2] [N=3]	[T=2] [B=1] [R=0] [CB=1] [CT=3] [N=0]	[T=2] [B=1] [R=0] [CB=1] [CT=3] [N=1]	[T=2] [B=1] [R=0] [CB=1] [CT=3] [N=2]	[T=2] [B=1] [R=0] [CB=1] [CT=3] [N=3]	[T=2] [B=1] [R=0] [CB=1] [CT=4] [N=0]	[T=2] [B=1] [R=0] [CB=1] [CT=4] [N=1]	[T=2] [B=1] [R=0] [CB=1] [CT=4] [N=2]	[T=2] [B=1] [R=0] [CB=1] [CT=4] [N=3]	[T=2] [B=1] [R=0] [CB=1] [CT=5] [N=0]	[T=2] [B=1] [R=0] [CB=1] [CT=5] [N=1]	[T=2] [B=1] [R=0] [CB=1] [CT=5] [N=2]	[T=2] [B=1] [R=0] [CB=1] [CT=5] [N=3]	[T=2] [B=1] [R=0] [CB=2] [CT=0] [N=0]	[T=2] [B=1] [R=0] [CB=2] [CT=0] [N=1]
R86	ct_coef															
	[T=2] [B=1] [R=0] [CB=2] [CT=0] [N=2]	[T=2] [B=1] [R=0] [CB=2]	[T=2] [B=1] [R=0] [CB=2]	[T=2] [B=1] [R=0] [CB=2]	[T=2] [B=1] [R=0] [CB=2]	[T=2] [B=1] [R=0] [CB=2]	[T=2] [B=1] [R=0] [CB=2]	[T=2] [B=1] [R=0] [CB=2]	[T=2] [B=1] [R=0] [CB=2]	[T=2] [B=1] [R=0] [CB=2]	[T=2] [B=1] [R=0] [CB=2] [CT=3]	[T=2] [B=1] [R=0] [CB=2] [CT=3]	[T=2] [B=1] [R=0] [CB=2]	[T=2] [B=1] [R=0] [CB=2]	[T=2] [B=1] [R=0] [CB=2]	[T=2] [B=1] [R=0] [CB=2] [CT=4] [N=1]

Rxxx Value 1 row = 1 Cacheline	16 32-bit counters															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		[CT=0] [N=3]	[CT=1] [N=0]	[CT=1] [N=1]	[CT=1] [N=2]	[CT=1] [N=3]	[CT=2] [N=0]	[CT=2] [N=1]	[CT=2] [N=2]	[CT=2] [N=3]	[N=0]	[N=1]	[CT=3] [N=2]	[CT=3] [N=3]	[CT=4] [N=0]	
R87	ct_coef															
	[T=2] [B=1] [R=0] [CB=2] [CT=4] [N=2]	[T=2] [B=1] [R=0] [CB=2] [CT=4] [N=3]	[T=2] [B=1] [R=0] [CB=2] [CT=5] [N=0]	[T=2] [B=1] [R=0] [CB=2] [CT=5] [N=1]	[T=2] [B=1] [R=0] [CB=2] [CT=5] [N=2]	[T=2] [B=1] [R=0] [CB=2] [CT=5] [N=3]	[T=2] [B=1] [R=0] [CB=3] [CT=0] [N=0]	[T=2] [B=1] [R=0] [CB=3] [CT=0] [N=1]	[T=2] [B=1] [R=0] [CB=3] [CT=0] [N=2]	[T=2] [B=1] [R=0] [CB=3] [CT=0] [N=3]	[T=2] [B=1] [R=0] [CB=3] [CT=1] [N=0]	[T=2] [B=1] [R=0] [CB=3] [CT=1] [N=1]	[T=2] [B=1] [R=0] [CB=3] [CT=1] [N=2]	[T=2] [B=1] [R=0] [CB=3] [CT=1] [N=3]	[T=2] [B=1] [R=0] [CB=3] [CT=2] [N=0]	[T=2] [B=1] [R=0] [CB=3] [CT=2] [N=1]
R88	ct_coef															
	[T=2] [B=1] [R=0] [CB=3] [CT=2] [N=2]	[T=2] [B=1] [R=0] [CB=3] [CT=2] [N=3]	[T=2] [B=1] [R=0] [CB=3] [CT=3] [N=0]	[T=2] [B=1] [R=0] [CB=3] [CT=3] [N=1]	[T=2] [B=1] [R=0] [CB=3] [CT=3] [N=2]	[T=2] [B=1] [R=0] [CB=3] [CT=3] [N=3]	[T=2] [B=1] [R=0] [CB=3] [CT=4] [N=0]	[T=2] [B=1] [R=0] [CB=3] [CT=4] [N=1]	[T=2] [B=1] [R=0] [CB=3] [CT=4] [N=2]	[T=2] [B=1] [R=0] [CB=3] [CT=4] [N=3]	[T=2] [B=1] [R=0] [CB=3] [CT=5] [N=0]	[T=2] [B=1] [R=0] [CB=3] [CT=5] [N=1]	[T=2] [B=1] [R=0] [CB=3] [CT=5] [N=2]	[T=2] [B=1] [R=0] [CB=3] [CT=5] [N=3]	[T=2] [B=1] [R=0] [CB=4] [CT=0] [N=0]	[T=2] [B=1] [R=0] [CB=4] [CT=0] [N=1]
R89	ct_coef															
	[T=2] [B=1] [R=0] [CB=4] [CT=0] [N=2]	[T=2] [B=1] [R=0] [CB=4] [CT=0] [N=3]	[T=2] [B=1] [R=0] [CB=4] [CT=1] [N=0]	[T=2] [B=1] [R=0] [CB=4] [CT=1] [N=1]	[T=2] [B=1] [R=0] [CB=4] [CT=1] [N=2]	[T=2] [B=1] [R=0] [CB=4] [CT=1] [N=3]	[T=2] [B=1] [R=0] [CB=4] [CT=2] [N=0]	[T=2] [B=1] [R=0] [CB=4] [CT=2] [N=1]	[T=2] [B=1] [R=0] [CB=4] [CT=2] [N=2]	[T=2] [B=1] [R=0] [CB=4] [CT=2] [N=3]	[T=2] [B=1] [R=0] [CB=4] [CT=3] [N=0]	[T=2] [B=1] [R=0] [CB=4] [CT=3] [N=1]	[T=2] [B=1] [R=0] [CB=4] [CT=3] [N=2]	[T=2] [B=1] [R=0] [CB=4] [CT=3] [N=3]	[T=2] [B=1] [R=0] [CB=4] [CT=4] [N=0]	[T=2] [B=1] [R=0] [CB=4] [CT=4] [N=1]

Rxxx Value 1 row = 1 Cacheline	16 32-bit counters															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R90	ct_coef															
	[T=2] [B=1] [R=0] [CB=4] [CT=4] [N=2]	[T=2] [B=1] [R=0] [CB=4] [CT=4] [N=3]	[T=2] [B=1] [R=0] [CB=4] [CT=5] [N=0]	[T=2] [B=1] [R=0] [CB=4] [CT=5] [N=1]	[T=2] [B=1] [R=0] [CB=4] [CT=5] [N=2]	[T=2] [B=1] [R=0] [CB=4] [CT=5] [N=3]	[T=2] [B=1] [R=0] [CB=5] [CT=0] [N=0]	[T=2] [B=1] [R=0] [CB=5] [CT=0] [N=1]	[T=2] [B=1] [R=0] [CB=5] [CT=0] [N=2]	[T=2] [B=1] [R=0] [CB=5] [CT=0] [N=3]	[T=2] [B=1] [R=0] [CB=5] [CT=1] [N=0]	[T=2] [B=1] [R=0] [CB=5] [CT=1] [N=1]	[T=2] [B=1] [R=0] [CB=5] [CT=1] [N=2]	[T=2] [B=1] [R=0] [CB=5] [CT=1] [N=3]	[T=2] [B=1] [R=0] [CB=5] [CT=2] [N=0]	[T=2] [B=1] [R=0] [CB=5] [CT=2] [N=1]
R91	ct_coef															
	[T=2] [B=1] [R=0] [CB=5] [CT=2] [N=2]	[T=2] [B=1] [R=0] [CB=5] [CT=2] [N=3]	[T=2] [B=1] [R=0] [CB=5] [CT=3] [N=0]	[T=2] [B=1] [R=0] [CB=5] [CT=3] [N=1]	[T=2] [B=1] [R=0] [CB=5] [CT=3] [N=2]	[T=2] [B=1] [R=0] [CB=5] [CT=3] [N=3]	[T=2] [B=1] [R=0] [CB=5] [CT=4] [N=0]	[T=2] [B=1] [R=0] [CB=5] [CT=4] [N=1]	[T=2] [B=1] [R=0] [CB=5] [CT=4] [N=2]	[T=2] [B=1] [R=0] [CB=5] [CT=4] [N=3]	[T=2] [B=1] [R=0] [CB=5] [CT=5] [N=0]	[T=2] [B=1] [R=0] [CB=5] [CT=5] [N=1]	[T=2] [B=1] [R=0] [CB=5] [CT=5] [N=2]	[T=2] [B=1] [R=0] [CB=5] [CT=5] [N=3]	[T=2] [B=1] [R=1] [CB=0] [CT=0] [N=0]	[T=2] [B=1] [R=1] [CB=0] [CT=0] [N=1]
R92	ct_coef															
	[T=2] [B=1] [R=1] [CB=0] [CT=0] [N=2]	[T=2] [B=1] [R=1] [CB=0] [CT=0] [N=3]	[T=2] [B=1] [R=1] [CB=0] [CT=1] [N=0]	[T=2] [B=1] [R=1] [CB=0] [CT=1] [N=1]	[T=2] [B=1] [R=1] [CB=0] [CT=1] [N=2]	[T=2] [B=1] [R=1] [CB=0] [CT=1] [N=3]	[T=2] [B=1] [R=1] [CB=0] [CT=2] [N=0]	[T=2] [B=1] [R=1] [CB=0] [CT=2] [N=1]	[T=2] [B=1] [R=1] [CB=0] [CT=2] [N=2]	[T=2] [B=1] [R=1] [CB=0] [CT=2] [N=3]	[T=2] [B=1] [R=1] [CB=1] [CT=0] [N=0]	[T=2] [B=1] [R=1] [CB=1] [CT=0] [N=1]	[T=2] [B=1] [R=1] [CB=1] [CT=0] [N=2]	[T=2] [B=1] [R=1] [CB=1] [CT=0] [N=3]	[T=2] [B=1] [R=1] [CB=1] [CT=1] [N=0]	[T=2] [B=1] [R=1] [CB=1] [CT=1] [N=1]
R93	ct_coef															
	[T=2]	[T=2]	[T=2]	[T=2]	[T=2]	[T=2]	[T=2]	[T=2]	[T=2]	[T=2]	[T=2]	[T=2]	[T=2]	[T=2]	[T=2]	[T=2]

Rxxx Value 1 row = 1 Cacheline	16 32-bit counters															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	[B=1] [R=1] [CB=1] [CT=1] [N=2]	[B=1] [R=1] [CB=1] [CT=1] [N=3]	[B=1] [R=1] [CB=1] [CT=2] [N=0]	[B=1] [R=1] [CB=1] [CT=2] [N=1]	[B=1] [R=1] [CB=1] [CT=2] [N=2]	[B=1] [R=1] [CB=1] [CT=2] [N=3]	[B=1] [R=1] [CB=1] [CT=3] [N=0]	[B=1] [R=1] [CB=1] [CT=3] [N=1]	[B=1] [R=1] [CB=1] [CT=3] [N=2]	[B=1] [R=1] [CB=1] [CT=3] [N=3]	[B=1] [R=1] [CB=1] [CT=4] [N=0]	[B=1] [R=1] [CB=1] [CT=4] [N=1]	[B=1] [R=1] [CB=1] [CT=4] [N=2]	[B=1] [R=1] [CB=1] [CT=4] [N=3]	[B=1] [R=1] [CB=1] [CT=5] [N=0]	[B=1] [R=1] [CB=1] [CT=5] [N=1]
R94	ct_coef															
	[T=2] [B=1] [R=1] [CB=1] [CT=5] [N=2]	[T=2] [B=1] [R=1] [CB=1] [CT=5] [N=3]	[T=2] [B=1] [R=1] [CB=2] [CT=0] [N=0]	[T=2] [B=1] [R=1] [CB=2] [CT=0] [N=1]	[T=2] [B=1] [R=1] [CB=2] [CT=0] [N=2]	[T=2] [B=1] [R=1] [CB=2] [CT=0] [N=3]	[T=2] [B=1] [R=1] [CB=2] [CT=1] [N=0]	[T=2] [B=1] [R=1] [CB=2] [CT=1] [N=1]	[T=2] [B=1] [R=1] [CB=2] [CT=1] [N=2]	[T=2] [B=1] [R=1] [CB=2] [CT=1] [N=3]	[T=2] [B=1] [R=1] [CB=2] [CT=2] [N=0]	[T=2] [B=1] [R=1] [CB=2] [CT=2] [N=1]	[T=2] [B=1] [R=1] [CB=2] [CT=2] [N=2]	[T=2] [B=1] [R=1] [CB=2] [CT=2] [N=3]	[T=2] [B=1] [R=1] [CB=2] [CT=3] [N=0]	[T=2] [B=1] [R=1] [CB=2] [CT=3] [N=1]
R95	ct_coef															
	[T=2] [B=1] [R=1] [CB=2] [CT=3] [N=2]	[T=2] [B=1] [R=1] [CB=2] [CT=3] [N=3]	[T=2] [B=1] [R=1] [CB=2] [CT=4] [N=0]	[T=2] [B=1] [R=1] [CB=2] [CT=4] [N=1]	[T=2] [B=1] [R=1] [CB=2] [CT=4] [N=2]	[T=2] [B=1] [R=1] [CB=2] [CT=4] [N=3]	[T=2] [B=1] [R=1] [CB=2] [CT=5] [N=0]	[T=2] [B=1] [R=1] [CB=2] [CT=5] [N=1]	[T=2] [B=1] [R=1] [CB=2] [CT=5] [N=2]	[T=2] [B=1] [R=1] [CB=2] [CT=5] [N=3]	[T=2] [B=1] [R=1] [CB=3] [CT=0] [N=0]	[T=2] [B=1] [R=1] [CB=3] [CT=0] [N=1]	[T=2] [B=1] [R=1] [CB=3] [CT=0] [N=2]	[T=2] [B=1] [R=1] [CB=3] [CT=0] [N=3]	[T=2] [B=1] [R=1] [CB=3] [CT=1] [N=0]	[T=2] [B=1] [R=1] [CB=3] [CT=1] [N=1]
R96	ct_coef															
	[T=2] [B=1] [R=1]	[T=2] [B=1] [R=1]	[T=2] [B=1] [R=1]	[T=2] [B=1] [R=1]	[T=2] [B=1] [R=1]	[T=2] [B=1] [R=1]	[T=2] [B=1] [R=1]	[T=2] [B=1] [R=1]	[T=2] [B=1] [R=1]	[T=2] [B=1] [R=1]	[T=2] [B=1] [R=1]	[T=2] [B=1] [R=1]	[T=2] [B=1] [R=1]	[T=2] [B=1] [R=1]	[T=2] [B=1] [R=1]	[T=2] [B=1] [R=1]

Rxxx Value 1 row = 1 Cacheline	16 32-bit counters															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	[CB=3] [CT=1] [N=2]	[CB=3] [CT=1] [N=3]	[CB=3] [CT=2] [N=0]	[CB=3] [CT=2] [N=1]	[CB=3] [CT=2] [N=2]	[CB=3] [CT=2] [N=3]	[CB=3] [CT=3] [N=0]	[CB=3] [CT=3] [N=1]	[CB=3] [CT=3] [N=2]	[CB=3] [CT=3] [N=3]	[CB=3] [CT=4] [N=0]	[CB=3] [CT=4] [N=1]	[CB=3] [CT=4] [N=2]	[CB=3] [CT=4] [N=3]	[CB=3] [CT=5] [N=0]	[CB=3] [CT=5] [N=1]
R97	ct_coef															
	[T=2] [B=1] [R=1] [CB=3] [CT=5] [N=2]	[T=2] [B=1] [R=1] [CB=3] [CT=5] [N=3]	[T=2] [B=1] [R=1] [CB=4] [CT=0] [N=0]	[T=2] [B=1] [R=1] [CB=4] [CT=0] [N=1]	[T=2] [B=1] [R=1] [CB=4] [CT=0] [N=2]	[T=2] [B=1] [R=1] [CB=4] [CT=0] [N=3]	[T=2] [B=1] [R=1] [CB=4] [CT=1] [N=0]	[T=2] [B=1] [R=1] [CB=4] [CT=1] [N=1]	[T=2] [B=1] [R=1] [CB=4] [CT=1] [N=2]	[T=2] [B=1] [R=1] [CB=4] [CT=1] [N=3]	[T=2] [B=1] [R=1] [CB=4] [CT=2] [N=0]	[T=2] [B=1] [R=1] [CB=4] [CT=2] [N=1]	[T=2] [B=1] [R=1] [CB=4] [CT=2] [N=2]	[T=2] [B=1] [R=1] [CB=4] [CT=2] [N=3]	[T=2] [B=1] [R=1] [CB=4] [CT=3] [N=0]	[T=2] [B=1] [R=1] [CB=4] [CT=3] [N=1]
R98	ct_coef															
	[T=2] [B=1] [R=1] [CB=4] [CT=3] [N=2]	[T=2] [B=1] [R=1] [CB=4] [CT=3] [N=3]	[T=2] [B=1] [R=1] [CB=4] [CT=4] [N=0]	[T=2] [B=1] [R=1] [CB=4] [CT=4] [N=1]	[T=2] [B=1] [R=1] [CB=4] [CT=4] [N=2]	[T=2] [B=1] [R=1] [CB=4] [CT=4] [N=3]	[T=2] [B=1] [R=1] [CB=4] [CT=5] [N=0]	[T=2] [B=1] [R=1] [CB=4] [CT=5] [N=1]	[T=2] [B=1] [R=1] [CB=4] [CT=5] [N=2]	[T=2] [B=1] [R=1] [CB=4] [CT=5] [N=3]	[T=2] [B=1] [R=1] [CB=5] [CT=0] [N=0]	[T=2] [B=1] [R=1] [CB=5] [CT=0] [N=1]	[T=2] [B=1] [R=1] [CB=5] [CT=0] [N=2]	[T=2] [B=1] [R=1] [CB=5] [CT=0] [N=3]	[T=2] [B=1] [R=1] [CB=5] [CT=1] [N=0]	[T=2] [B=1] [R=1] [CB=5] [CT=1] [N=1]
R99	ct_coef															
	[T=2] [B=1] [R=1] [CB=5] [CT=1]	[T=2] [B=1] [R=1] [CB=5]	[T=2] [B=1] [R=1] [CB=5]	[T=2] [B=1] [R=1] [CB=5]	[T=2] [B=1] [R=1] [CB=5]	[T=2] [B=1] [R=1] [CB=5]	[T=2] [B=1] [R=1] [CB=5]	[T=2] [B=1] [R=1] [CB=5]	[T=2] [B=1] [R=1] [CB=5]	[T=2] [B=1] [R=1] [CB=5]	[T=2] [B=1] [R=1] [CB=5]	[T=2] [B=1] [R=1] [CB=5]	[T=2] [B=1] [R=1] [CB=5]	[T=2] [B=1] [R=1] [CB=5]	[T=2] [B=1] [R=1] [CB=5]	[T=2] [B=1] [R=1] [CB=5] [CT=5]

Rxxx Value 1 row = 1 Cacheline	16 32-bit counters															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	[N=2]	[CT=1] [N=3]	[CT=2] [N=0]	[CT=2] [N=1]	[CT=2] [N=2]	[CT=2] [N=3]	[CT=3] [N=0]	[CT=3] [N=1]	[CT=3] [N=2]	[CT=3] [N=3]	[CT=4] [N=0]	[CT=4] [N=1]	[CT=4] [N=2]	[CT=4] [N=3]	[CT=5] [N=0]	[N=1]
R100	ct_coef															
	[T=2] [B=1] [R=1] [CB=5] [CT=5] [N=2]	[T=2] [B=1] [R=1] [CB=5] [CT=5] [N=3]	[T=3] [B=0] [R=0] [CB=0] [CT=0] [N=0]	[T=3] [B=0] [R=0] [CB=0] [CT=0] [N=1]	[T=3] [B=0] [R=0] [CB=0] [CT=0] [N=2]	[T=3] [B=0] [R=0] [CB=0] [CT=0] [N=3]	[T=3] [B=0] [R=0] [CB=0] [CT=1] [N=0]	[T=3] [B=0] [R=0] [CB=0] [CT=1] [N=1]	[T=3] [B=0] [R=0] [CB=0] [CT=1] [N=2]	[T=3] [B=0] [R=0] [CB=0] [CT=1] [N=3]	[T=3] [B=0] [R=0] [CB=0] [CT=2] [N=0]	[T=3] [B=0] [R=0] [CB=0] [CT=2] [N=1]	[T=3] [B=0] [R=0] [CB=0] [CT=2] [N=2]	[T=3] [B=0] [R=0] [CB=0] [CT=2] [N=3]	[T=3] [B=0] [R=0] [CB=1] [CT=0] [N=0]	[T=3] [B=0] [R=0] [CB=1] [CT=0] [N=1]
R101	ct_coef															
	[T=3] [B=0] [R=0] [CB=1] [CT=0] [N=2]	[T=3] [B=0] [R=0] [CB=1] [CT=0] [N=3]	[T=3] [B=0] [R=0] [CB=1] [CT=1] [N=0]	[T=3] [B=0] [R=0] [CB=1] [CT=1] [N=1]	[T=3] [B=0] [R=0] [CB=1] [CT=1] [N=2]	[T=3] [B=0] [R=0] [CB=1] [CT=1] [N=3]	[T=3] [B=0] [R=0] [CB=1] [CT=2] [N=0]	[T=3] [B=0] [R=0] [CB=1] [CT=2] [N=1]	[T=3] [B=0] [R=0] [CB=1] [CT=2] [N=2]	[T=3] [B=0] [R=0] [CB=1] [CT=2] [N=3]	[T=3] [B=0] [R=0] [CB=1] [CT=3] [N=0]	[T=3] [B=0] [R=0] [CB=1] [CT=3] [N=1]	[T=3] [B=0] [R=0] [CB=1] [CT=3] [N=2]	[T=3] [B=0] [R=0] [CB=1] [CT=3] [N=3]	[T=3] [B=0] [R=0] [CB=1] [CT=4] [N=0]	[T=3] [B=0] [R=0] [CB=1] [CT=4] [N=1]
R102	ct_coef															
	[T=3] [B=0] [R=0] [CB=1] [CT=4] [N=2]	[T=3] [B=0] [R=0] [CB=1] [CT=4]	[T=3] [B=0] [R=0] [CB=1] [CT=5]	[T=3] [B=0] [R=0] [CB=1] [CT=5]	[T=3] [B=0] [R=0] [CB=1] [CT=5]	[T=3] [B=0] [R=0] [CB=1] [CT=5]	[T=3] [B=0] [R=0] [CB=2] [CT=0]	[T=3] [B=0] [R=0] [CB=2] [CT=0]	[T=3] [B=0] [R=0] [CB=2] [CT=0]	[T=3] [B=0] [R=0] [CB=2] [CT=0]	[T=3] [B=0] [R=0] [CB=2] [CT=1] [N=0]	[T=3] [B=0] [R=0] [CB=2] [CT=1] [N=1]	[T=3] [B=0] [R=0] [CB=2] [CT=1]	[T=3] [B=0] [R=0] [CB=2] [CT=1]	[T=3] [B=0] [R=0] [CB=2] [CT=2]	[T=3] [B=0] [R=0] [CB=2] [CT=2] [N=1]

Rxxx Value 1 row = 1 Cacheline	16 32-bit counters															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		[N=3]	[N=0]	[N=1]	[N=2]	[N=3]	[N=0]	[N=1]	[N=2]	[N=3]			[N=2]	[N=3]	[N=0]	
R103	ct_coef															
	[T=3] [B=0] [R=0] [CB=2] [CT=2] [N=2]	[T=3] [B=0] [R=0] [CB=2] [CT=2] [N=3]	[T=3] [B=0] [R=0] [CB=2] [CT=3] [N=0]	[T=3] [B=0] [R=0] [CB=2] [CT=3] [N=1]	[T=3] [B=0] [R=0] [CB=2] [CT=3] [N=2]	[T=3] [B=0] [R=0] [CB=2] [CT=3] [N=3]	[T=3] [B=0] [R=0] [CB=2] [CT=4] [N=0]	[T=3] [B=0] [R=0] [CB=2] [CT=4] [N=1]	[T=3] [B=0] [R=0] [CB=2] [CT=4] [N=2]	[T=3] [B=0] [R=0] [CB=2] [CT=4] [N=3]	[T=3] [B=0] [R=0] [CB=2] [CT=5] [N=0]	[T=3] [B=0] [R=0] [CB=2] [CT=5] [N=1]	[T=3] [B=0] [R=0] [CB=2] [CT=5] [N=2]	[T=3] [B=0] [R=0] [CB=2] [CT=5] [N=3]	[T=3] [B=0] [R=0] [CB=3] [CT=0] [N=0]	[T=3] [B=0] [R=0] [CB=3] [CT=0] [N=1]
R104	ct_coef															
	[T=3] [B=0] [R=0] [CB=3] [CT=0] [N=2]	[T=3] [B=0] [R=0] [CB=3] [CT=0] [N=3]	[T=3] [B=0] [R=0] [CB=3] [CT=1] [N=0]	[T=3] [B=0] [R=0] [CB=3] [CT=1] [N=1]	[T=3] [B=0] [R=0] [CB=3] [CT=1] [N=2]	[T=3] [B=0] [R=0] [CB=3] [CT=1] [N=3]	[T=3] [B=0] [R=0] [CB=3] [CT=2] [N=0]	[T=3] [B=0] [R=0] [CB=3] [CT=2] [N=1]	[T=3] [B=0] [R=0] [CB=3] [CT=2] [N=2]	[T=3] [B=0] [R=0] [CB=3] [CT=2] [N=3]	[T=3] [B=0] [R=0] [CB=3] [CT=3] [N=0]	[T=3] [B=0] [R=0] [CB=3] [CT=3] [N=1]	[T=3] [B=0] [R=0] [CB=3] [CT=3] [N=2]	[T=3] [B=0] [R=0] [CB=3] [CT=3] [N=3]	[T=3] [B=0] [R=0] [CB=3] [CT=4] [N=0]	[T=3] [B=0] [R=0] [CB=3] [CT=4] [N=1]
R105	ct_coef															
	[T=3] [B=0] [R=0] [CB=3] [CT=4] [N=2]	[T=3] [B=0] [R=0] [CB=3] [CT=4] [N=3]	[T=3] [B=0] [R=0] [CB=3] [CT=5] [N=0]	[T=3] [B=0] [R=0] [CB=3] [CT=5] [N=1]	[T=3] [B=0] [R=0] [CB=3] [CT=5] [N=2]	[T=3] [B=0] [R=0] [CB=3] [CT=5] [N=3]	[T=3] [B=0] [R=0] [CB=4] [CT=0] [N=0]	[T=3] [B=0] [R=0] [CB=4] [CT=0] [N=1]	[T=3] [B=0] [R=0] [CB=4] [CT=0] [N=2]	[T=3] [B=0] [R=0] [CB=4] [CT=0] [N=3]	[T=3] [B=0] [R=0] [CB=4] [CT=1] [N=0]	[T=3] [B=0] [R=0] [CB=4] [CT=1] [N=1]	[T=3] [B=0] [R=0] [CB=4] [CT=1] [N=2]	[T=3] [B=0] [R=0] [CB=4] [CT=1] [N=3]	[T=3] [B=0] [R=0] [CB=4] [CT=2] [N=0]	[T=3] [B=0] [R=0] [CB=4] [CT=2] [N=1]
R106	ct_coef															

Rxxx Value 1 row = 1 Cacheline	16 32-bit counters															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	[T=3] [B=0] [R=0] [CB=4] [CT=2] [N=2]	[T=3] [B=0] [R=0] [CB=4] [CT=2] [N=3]	[T=3] [B=0] [R=0] [CB=4] [CT=3] [N=0]	[T=3] [B=0] [R=0] [CB=4] [CT=3] [N=1]	[T=3] [B=0] [R=0] [CB=4] [CT=3] [N=2]	[T=3] [B=0] [R=0] [CB=4] [CT=3] [N=3]	[T=3] [B=0] [R=0] [CB=4] [CT=4] [N=0]	[T=3] [B=0] [R=0] [CB=4] [CT=4] [N=1]	[T=3] [B=0] [R=0] [CB=4] [CT=4] [N=2]	[T=3] [B=0] [R=0] [CB=4] [CT=4] [N=3]	[T=3] [B=0] [R=0] [CB=4] [CT=5] [N=0]	[T=3] [B=0] [R=0] [CB=4] [CT=5] [N=1]	[T=3] [B=0] [R=0] [CB=4] [CT=5] [N=2]	[T=3] [B=0] [R=0] [CB=4] [CT=5] [N=3]	[T=3] [B=0] [R=0] [CB=5] [CT=0] [N=0]	[T=3] [B=0] [R=0] [CB=5] [CT=0] [N=1]
R107	ct_coef															
	[T=3] [B=0] [R=0] [CB=5] [CT=0] [N=2]	[T=3] [B=0] [R=0] [CB=5] [CT=0] [N=3]	[T=3] [B=0] [R=0] [CB=5] [CT=1] [N=0]	[T=3] [B=0] [R=0] [CB=5] [CT=1] [N=1]	[T=3] [B=0] [R=0] [CB=5] [CT=1] [N=2]	[T=3] [B=0] [R=0] [CB=5] [CT=1] [N=3]	[T=3] [B=0] [R=0] [CB=5] [CT=2] [N=0]	[T=3] [B=0] [R=0] [CB=5] [CT=2] [N=1]	[T=3] [B=0] [R=0] [CB=5] [CT=2] [N=2]	[T=3] [B=0] [R=0] [CB=5] [CT=2] [N=3]	[T=3] [B=0] [R=0] [CB=5] [CT=3] [N=0]	[T=3] [B=0] [R=0] [CB=5] [CT=3] [N=1]	[T=3] [B=0] [R=0] [CB=5] [CT=3] [N=2]	[T=3] [B=0] [R=0] [CB=5] [CT=3] [N=3]	[T=3] [B=0] [R=0] [CB=5] [CT=4] [N=0]	[T=3] [B=0] [R=0] [CB=5] [CT=4] [N=1]
R108	ct_coef															
	[T=3] [B=0] [R=0] [CB=5] [CT=4] [N=2]	[T=3] [B=0] [R=0] [CB=5] [CT=4] [N=3]	[T=3] [B=0] [R=0] [CB=5] [CT=5] [N=0]	[T=3] [B=0] [R=0] [CB=5] [CT=5] [N=1]	[T=3] [B=0] [R=0] [CB=5] [CT=5] [N=2]	[T=3] [B=0] [R=0] [CB=5] [CT=5] [N=3]	[T=3] [B=0] [R=1] [CB=0] [CT=0] [N=0]	[T=3] [B=0] [R=1] [CB=0] [CT=0] [N=1]	[T=3] [B=0] [R=1] [CB=0] [CT=0] [N=2]	[T=3] [B=0] [R=1] [CB=0] [CT=0] [N=3]	[T=3] [B=0] [R=1] [CB=0] [CT=1] [N=0]	[T=3] [B=0] [R=1] [CB=0] [CT=1] [N=1]	[T=3] [B=0] [R=1] [CB=0] [CT=1] [N=2]	[T=3] [B=0] [R=1] [CB=0] [CT=1] [N=3]	[T=3] [B=0] [R=1] [CB=0] [CT=2] [N=0]	[T=3] [B=0] [R=1] [CB=0] [CT=2] [N=1]
R109	ct_coef															
	[T=3] [B=0]	[T=3] [B=0]	[T=3] [B=0]	[T=3] [B=0]	[T=3] [B=0]	[T=3] [B=0]	[T=3] [B=0]	[T=3] [B=0]	[T=3] [B=0]	[T=3] [B=0]	[T=3] [B=0]	[T=3] [B=0]	[T=3] [B=0]	[T=3] [B=0]	[T=3] [B=0]	[T=3] [B=0]

Rxxx Value 1 row = 1 Cacheline	16 32-bit counters															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	[R=1] [CB=0] [CT=2] [N=2]	[R=1] [CB=0] [CT=2] [N=3]	[R=1] [CB=1] [CT=0] [N=0]	[R=1] [CB=1] [CT=0] [N=1]	[R=1] [CB=1] [CT=0] [N=2]	[R=1] [CB=1] [CT=0] [N=3]	[R=1] [CB=1] [CT=1] [N=0]	[R=1] [CB=1] [CT=1] [N=1]	[R=1] [CB=1] [CT=1] [N=2]	[R=1] [CB=1] [CT=1] [N=3]	[R=1] [CB=1] [CT=2] [N=0]	[R=1] [CB=1] [CT=2] [N=1]	[R=1] [CB=1] [CT=2] [N=2]	[R=1] [CB=1] [CT=2] [N=3]	[R=1] [CB=1] [CT=3] [N=0]	[R=1] [CB=1] [CT=3] [N=1]
R110	ct_coef															
	[T=3] [B=0] [R=1] [CB=1] [CT=3] [N=2]	[T=3] [B=0] [R=1] [CB=1] [CT=3] [N=3]	[T=3] [B=0] [R=1] [CB=1] [CT=4] [N=0]	[T=3] [B=0] [R=1] [CB=1] [CT=4] [N=1]	[T=3] [B=0] [R=1] [CB=1] [CT=4] [N=2]	[T=3] [B=0] [R=1] [CB=1] [CT=4] [N=3]	[T=3] [B=0] [R=1] [CB=1] [CT=5] [N=0]	[T=3] [B=0] [R=1] [CB=1] [CT=5] [N=1]	[T=3] [B=0] [R=1] [CB=1] [CT=5] [N=2]	[T=3] [B=0] [R=1] [CB=1] [CT=5] [N=3]	[T=3] [B=0] [R=1] [CB=2] [CT=0] [N=0]	[T=3] [B=0] [R=1] [CB=2] [CT=0] [N=1]	[T=3] [B=0] [R=1] [CB=2] [CT=0] [N=2]	[T=3] [B=0] [R=1] [CB=2] [CT=0] [N=3]	[T=3] [B=0] [R=1] [CB=2] [CT=1] [N=0]	[T=3] [B=0] [R=1] [CB=2] [CT=1] [N=1]
R111	ct_coef															
	[T=3] [B=0] [R=1] [CB=2] [CT=1] [N=2]	[T=3] [B=0] [R=1] [CB=2] [CT=1] [N=3]	[T=3] [B=0] [R=1] [CB=2] [CT=2] [N=0]	[T=3] [B=0] [R=1] [CB=2] [CT=2] [N=1]	[T=3] [B=0] [R=1] [CB=2] [CT=2] [N=2]	[T=3] [B=0] [R=1] [CB=2] [CT=2] [N=3]	[T=3] [B=0] [R=1] [CB=2] [CT=3] [N=0]	[T=3] [B=0] [R=1] [CB=2] [CT=3] [N=1]	[T=3] [B=0] [R=1] [CB=2] [CT=3] [N=2]	[T=3] [B=0] [R=1] [CB=2] [CT=3] [N=3]	[T=3] [B=0] [R=1] [CB=2] [CT=4] [N=0]	[T=3] [B=0] [R=1] [CB=2] [CT=4] [N=1]	[T=3] [B=0] [R=1] [CB=2] [CT=4] [N=2]	[T=3] [B=0] [R=1] [CB=2] [CT=4] [N=3]	[T=3] [B=0] [R=1] [CB=2] [CT=5] [N=0]	[T=3] [B=0] [R=1] [CB=2] [CT=5] [N=1]
R112	ct_coef															
	[T=3] [B=0] [R=1] [CB=2]	[T=3] [B=0] [R=1]	[T=3] [B=0] [R=1]	[T=3] [B=0] [R=1]	[T=3] [B=0] [R=1]	[T=3] [B=0] [R=1]	[T=3] [B=0] [R=1]	[T=3] [B=0] [R=1]	[T=3] [B=0] [R=1]	[T=3] [B=0] [R=1]	[T=3] [B=0] [R=1]	[T=3] [B=0] [R=1]	[T=3] [B=0] [R=1]	[T=3] [B=0] [R=1]	[T=3] [B=0] [R=1]	[T=3] [B=0] [R=1] [CB=3]

Rxxx Value 1 row = 1 Cacheline	16 32-bit counters															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	[CT=5] [N=2]	[CB=2] [CT=5] [N=3]	[CB=3] [CT=0] [N=0]	[CB=3] [CT=0] [N=1]	[CB=3] [CT=0] [N=2]	[CB=3] [CT=0] [N=3]	[CB=3] [CT=1] [N=0]	[CB=3] [CT=1] [N=1]	[CB=3] [CT=1] [N=2]	[CB=3] [CT=1] [N=3]	[CB=3] [CT=2] [N=0]	[CB=3] [CT=2] [N=1]	[CB=3] [CT=2] [N=2]	[CB=3] [CT=2] [N=3]	[CB=3] [CT=3] [N=0]	[CT=3] [N=1]
R113	ct_coef															
	[T=3] [B=0] [R=1] [CB=3] [CT=3] [N=2]	[T=3] [B=0] [R=1] [CB=3] [CT=3] [N=3]	[T=3] [B=0] [R=1] [CB=3] [CT=4] [N=0]	[T=3] [B=0] [R=1] [CB=3] [CT=4] [N=1]	[T=3] [B=0] [R=1] [CB=3] [CT=4] [N=2]	[T=3] [B=0] [R=1] [CB=3] [CT=4] [N=3]	[T=3] [B=0] [R=1] [CB=3] [CT=5] [N=0]	[T=3] [B=0] [R=1] [CB=3] [CT=5] [N=1]	[T=3] [B=0] [R=1] [CB=3] [CT=5] [N=2]	[T=3] [B=0] [R=1] [CB=3] [CT=5] [N=3]	[T=3] [B=0] [R=1] [CB=4] [CT=0] [N=0]	[T=3] [B=0] [R=1] [CB=4] [CT=0] [N=1]	[T=3] [B=0] [R=1] [CB=4] [CT=0] [N=2]	[T=3] [B=0] [R=1] [CB=4] [CT=0] [N=3]	[T=3] [B=0] [R=1] [CB=4] [CT=1] [N=0]	[T=3] [B=0] [R=1] [CB=4] [CT=1] [N=1]
R114	ct_coef															
	[T=3] [B=0] [R=1] [CB=4] [CT=1] [N=2]	[T=3] [B=0] [R=1] [CB=4] [CT=1] [N=3]	[T=3] [B=0] [R=1] [CB=4] [CT=2] [N=0]	[T=3] [B=0] [R=1] [CB=4] [CT=2] [N=1]	[T=3] [B=0] [R=1] [CB=4] [CT=2] [N=2]	[T=3] [B=0] [R=1] [CB=4] [CT=2] [N=3]	[T=3] [B=0] [R=1] [CB=4] [CT=3] [N=0]	[T=3] [B=0] [R=1] [CB=4] [CT=3] [N=1]	[T=3] [B=0] [R=1] [CB=4] [CT=3] [N=2]	[T=3] [B=0] [R=1] [CB=4] [CT=3] [N=3]	[T=3] [B=0] [R=1] [CB=4] [CT=4] [N=0]	[T=3] [B=0] [R=1] [CB=4] [CT=4] [N=1]	[T=3] [B=0] [R=1] [CB=4] [CT=4] [N=2]	[T=3] [B=0] [R=1] [CB=4] [CT=4] [N=3]	[T=3] [B=0] [R=1] [CB=4] [CT=5] [N=0]	[T=3] [B=0] [R=1] [CB=4] [CT=5] [N=1]
R115	ct_coef															
	[T=3] [B=0] [R=1] [CB=4] [CT=5] [N=2]	[T=3] [B=0] [R=1] [CB=4]	[T=3] [B=0] [R=1] [CB=5]	[T=3] [B=0] [R=1] [CB=5]	[T=3] [B=0] [R=1] [CB=5]	[T=3] [B=0] [R=1] [CB=5]	[T=3] [B=0] [R=1] [CB=5]	[T=3] [B=0] [R=1] [CB=5]	[T=3] [B=0] [R=1] [CB=5]	[T=3] [B=0] [R=1] [CB=5]	[T=3] [B=0] [R=1] [CB=5] [CT=2]	[T=3] [B=0] [R=1] [CB=5] [CT=2]	[T=3] [B=0] [R=1] [CB=5]	[T=3] [B=0] [R=1] [CB=5]	[T=3] [B=0] [R=1] [CB=5]	[T=3] [B=0] [R=1] [CB=5] [CT=3] [N=1]

Rxxx Value 1 row = 1 Cacheline	16 32-bit counters															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		[CT=5] [N=3]	[CT=0] [N=0]	[CT=0] [N=1]	[CT=0] [N=2]	[CT=0] [N=3]	[CT=1] [N=0]	[CT=1] [N=1]	[CT=1] [N=2]	[CT=1] [N=3]	[N=0]	[N=1]	[CT=2] [N=2]	[CT=2] [N=3]	[CT=3] [N=0]	
R116	ct_coef															
	[T=3] [B=0] [R=1] [CB=5] [CT=3] [N=2]	[T=3] [B=0] [R=1] [CB=5] [CT=3] [N=3]	[T=3] [B=0] [R=1] [CB=5] [CT=4] [N=0]	[T=3] [B=0] [R=1] [CB=5] [CT=4] [N=1]	[T=3] [B=0] [R=1] [CB=5] [CT=4] [N=2]	[T=3] [B=0] [R=1] [CB=5] [CT=4] [N=3]	[T=3] [B=0] [R=1] [CB=5] [CT=5] [N=0]	[T=3] [B=0] [R=1] [CB=5] [CT=5] [N=1]	[T=3] [B=0] [R=1] [CB=5] [CT=5] [N=2]	[T=3] [B=0] [R=1] [CB=5] [CT=5] [N=3]	[T=3] [B=1] [R=0] [CB=0] [CT=0] [N=0]	[T=3] [B=1] [R=0] [CB=0] [CT=0] [N=1]	[T=3] [B=1] [R=0] [CB=0] [CT=0] [N=2]	[T=3] [B=1] [R=0] [CB=0] [CT=0] [N=3]	[T=3] [B=1] [R=0] [CB=0] [CT=1] [N=0]	[T=3] [B=1] [R=0] [CB=0] [CT=1] [N=1]
R117	ct_coef															
	[T=3] [B=1] [R=0] [CB=0] [CT=1] [N=2]	[T=3] [B=1] [R=0] [CB=0] [CT=1] [N=3]	[T=3] [B=1] [R=0] [CB=0] [CT=2] [N=0]	[T=3] [B=1] [R=0] [CB=0] [CT=2] [N=1]	[T=3] [B=1] [R=0] [CB=0] [CT=2] [N=2]	[T=3] [B=1] [R=0] [CB=0] [CT=2] [N=3]	[T=3] [B=1] [R=0] [CB=1] [CT=0] [N=0]	[T=3] [B=1] [R=0] [CB=1] [CT=0] [N=1]	[T=3] [B=1] [R=0] [CB=1] [CT=0] [N=2]	[T=3] [B=1] [R=0] [CB=1] [CT=0] [N=3]	[T=3] [B=1] [R=0] [CB=1] [CT=1] [N=0]	[T=3] [B=1] [R=0] [CB=1] [CT=1] [N=1]	[T=3] [B=1] [R=0] [CB=1] [CT=1] [N=2]	[T=3] [B=1] [R=0] [CB=1] [CT=1] [N=3]	[T=3] [B=1] [R=0] [CB=1] [CT=2] [N=0]	[T=3] [B=1] [R=0] [CB=1] [CT=2] [N=1]
R118	ct_coef															
	[T=3] [B=1] [R=0] [CB=1] [CT=2] [N=2]	[T=3] [B=1] [R=0] [CB=1] [CT=2] [N=3]	[T=3] [B=1] [R=0] [CB=1] [CT=3] [N=0]	[T=3] [B=1] [R=0] [CB=1] [CT=3] [N=1]	[T=3] [B=1] [R=0] [CB=1] [CT=3] [N=2]	[T=3] [B=1] [R=0] [CB=1] [CT=3] [N=3]	[T=3] [B=1] [R=0] [CB=1] [CT=4] [N=0]	[T=3] [B=1] [R=0] [CB=1] [CT=4] [N=1]	[T=3] [B=1] [R=0] [CB=1] [CT=4] [N=2]	[T=3] [B=1] [R=0] [CB=1] [CT=4] [N=3]	[T=3] [B=1] [R=0] [CB=1] [CT=5] [N=0]	[T=3] [B=1] [R=0] [CB=1] [CT=5] [N=1]	[T=3] [B=1] [R=0] [CB=1] [CT=5] [N=2]	[T=3] [B=1] [R=0] [CB=1] [CT=5] [N=3]	[T=3] [B=1] [R=0] [CB=2] [CT=0] [N=0]	[T=3] [B=1] [R=0] [CB=2] [CT=0] [N=1]

Rxxx Value 1 row = 1 Cacheline	16 32-bit counters															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R119	ct_coef															
	[T=3] [B=1] [R=0] [CB=2] [CT=0] [N=2]	[T=3] [B=1] [R=0] [CB=2] [CT=0] [N=3]	[T=3] [B=1] [R=0] [CB=2] [CT=1] [N=0]	[T=3] [B=1] [R=0] [CB=2] [CT=1] [N=1]	[T=3] [B=1] [R=0] [CB=2] [CT=1] [N=2]	[T=3] [B=1] [R=0] [CB=2] [CT=1] [N=3]	[T=3] [B=1] [R=0] [CB=2] [CT=2] [N=0]	[T=3] [B=1] [R=0] [CB=2] [CT=2] [N=1]	[T=3] [B=1] [R=0] [CB=2] [CT=2] [N=2]	[T=3] [B=1] [R=0] [CB=2] [CT=2] [N=3]	[T=3] [B=1] [R=0] [CB=2] [CT=3] [N=0]	[T=3] [B=1] [R=0] [CB=2] [CT=3] [N=1]	[T=3] [B=1] [R=0] [CB=2] [CT=3] [N=2]	[T=3] [B=1] [R=0] [CB=2] [CT=3] [N=3]	[T=3] [B=1] [R=0] [CB=2] [CT=4] [N=0]	[T=3] [B=1] [R=0] [CB=2] [CT=4] [N=1]
R120	ct_coef															
	[T=3] [B=1] [R=0] [CB=2] [CT=4] [N=2]	[T=3] [B=1] [R=0] [CB=2] [CT=4] [N=3]	[T=3] [B=1] [R=0] [CB=2] [CT=5] [N=0]	[T=3] [B=1] [R=0] [CB=2] [CT=5] [N=1]	[T=3] [B=1] [R=0] [CB=2] [CT=5] [N=2]	[T=3] [B=1] [R=0] [CB=2] [CT=5] [N=3]	[T=3] [B=1] [R=0] [CB=3] [CT=0] [N=0]	[T=3] [B=1] [R=0] [CB=3] [CT=0] [N=1]	[T=3] [B=1] [R=0] [CB=3] [CT=0] [N=2]	[T=3] [B=1] [R=0] [CB=3] [CT=0] [N=3]	[T=3] [B=1] [R=0] [CB=3] [CT=1] [N=0]	[T=3] [B=1] [R=0] [CB=3] [CT=1] [N=1]	[T=3] [B=1] [R=0] [CB=3] [CT=1] [N=2]	[T=3] [B=1] [R=0] [CB=3] [CT=1] [N=3]	[T=3] [B=1] [R=0] [CB=3] [CT=2] [N=0]	[T=3] [B=1] [R=0] [CB=3] [CT=2] [N=1]
R121	ct_coef															
	[T=3] [B=1] [R=0] [CB=3] [CT=2] [N=2]	[T=3] [B=1] [R=0] [CB=3] [CT=2] [N=3]	[T=3] [B=1] [R=0] [CB=3] [CT=3] [N=0]	[T=3] [B=1] [R=0] [CB=3] [CT=3] [N=1]	[T=3] [B=1] [R=0] [CB=3] [CT=3] [N=2]	[T=3] [B=1] [R=0] [CB=3] [CT=3] [N=3]	[T=3] [B=1] [R=0] [CB=3] [CT=4] [N=0]	[T=3] [B=1] [R=0] [CB=3] [CT=4] [N=1]	[T=3] [B=1] [R=0] [CB=3] [CT=4] [N=2]	[T=3] [B=1] [R=0] [CB=3] [CT=4] [N=3]	[T=3] [B=1] [R=0] [CB=3] [CT=5] [N=0]	[T=3] [B=1] [R=0] [CB=3] [CT=5] [N=1]	[T=3] [B=1] [R=0] [CB=3] [CT=5] [N=2]	[T=3] [B=1] [R=0] [CB=3] [CT=5] [N=3]	[T=3] [B=1] [R=0] [CB=4] [CT=0] [N=0]	[T=3] [B=1] [R=0] [CB=4] [CT=0] [N=1]
R122	ct_coef															
	[T=3]	[T=3]	[T=3]	[T=3]	[T=3]	[T=3]	[T=3]	[T=3]	[T=3]	[T=3]	[T=3]	[T=3]	[T=3]	[T=3]	[T=3]	[T=3]

Rxxx Value 1 row = 1 Cacheline	16 32-bit counters															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	[B=1] [R=0] [CB=4] [CT=0] [N=2]	[B=1] [R=0] [CB=4] [CT=0] [N=3]	[B=1] [R=0] [CB=4] [CT=1] [N=0]	[B=1] [R=0] [CB=4] [CT=1] [N=1]	[B=1] [R=0] [CB=4] [CT=1] [N=2]	[B=1] [R=0] [CB=4] [CT=1] [N=3]	[B=1] [R=0] [CB=4] [CT=2] [N=0]	[B=1] [R=0] [CB=4] [CT=2] [N=1]	[B=1] [R=0] [CB=4] [CT=2] [N=2]	[B=1] [R=0] [CB=4] [CT=2] [N=3]	[B=1] [R=0] [CB=4] [CT=3] [N=0]	[B=1] [R=0] [CB=4] [CT=3] [N=1]	[B=1] [R=0] [CB=4] [CT=3] [N=2]	[B=1] [R=0] [CB=4] [CT=3] [N=3]	[B=1] [R=0] [CB=4] [CT=4] [N=0]	[B=1] [R=0] [CB=4] [CT=4] [N=1]
R123	ct_coef															
	[T=3] [B=1] [R=0] [CB=4] [CT=4] [N=2]	[T=3] [B=1] [R=0] [CB=4] [CT=4] [N=3]	[T=3] [B=1] [R=0] [CB=4] [CT=5] [N=0]	[T=3] [B=1] [R=0] [CB=4] [CT=5] [N=1]	[T=3] [B=1] [R=0] [CB=4] [CT=5] [N=2]	[T=3] [B=1] [R=0] [CB=4] [CT=5] [N=3]	[T=3] [B=1] [R=0] [CB=5] [CT=0] [N=0]	[T=3] [B=1] [R=0] [CB=5] [CT=0] [N=1]	[T=3] [B=1] [R=0] [CB=5] [CT=0] [N=2]	[T=3] [B=1] [R=0] [CB=5] [CT=0] [N=3]	[T=3] [B=1] [R=0] [CB=5] [CT=1] [N=0]	[T=3] [B=1] [R=0] [CB=5] [CT=1] [N=1]	[T=3] [B=1] [R=0] [CB=5] [CT=1] [N=2]	[T=3] [B=1] [R=0] [CB=5] [CT=1] [N=3]	[T=3] [B=1] [R=0] [CB=5] [CT=2] [N=0]	[T=3] [B=1] [R=0] [CB=5] [CT=2] [N=1]
R124	ct_coef															
	[T=3] [B=1] [R=0] [CB=5] [CT=2] [N=2]	[T=3] [B=1] [R=0] [CB=5] [CT=2] [N=3]	[T=3] [B=1] [R=0] [CB=5] [CT=3] [N=0]	[T=3] [B=1] [R=0] [CB=5] [CT=3] [N=1]	[T=3] [B=1] [R=0] [CB=5] [CT=3] [N=2]	[T=3] [B=1] [R=0] [CB=5] [CT=3] [N=3]	[T=3] [B=1] [R=0] [CB=5] [CT=4] [N=0]	[T=3] [B=1] [R=0] [CB=5] [CT=4] [N=1]	[T=3] [B=1] [R=0] [CB=5] [CT=4] [N=2]	[T=3] [B=1] [R=0] [CB=5] [CT=4] [N=3]	[T=3] [B=1] [R=0] [CB=5] [CT=5] [N=0]	[T=3] [B=1] [R=0] [CB=5] [CT=5] [N=1]	[T=3] [B=1] [R=0] [CB=5] [CT=5] [N=2]	[T=3] [B=1] [R=0] [CB=5] [CT=5] [N=3]	[T=3] [B=1] [R=1] [CB=0] [CT=0] [N=0]	[T=3] [B=1] [R=1] [CB=0] [CT=0] [N=1]
R125	ct_coef															
	[T=3] [B=1] [R=1]	[T=3] [B=1] [R=1]	[T=3] [B=1] [R=1]	[T=3] [B=1] [R=1]	[T=3] [B=1] [R=1]	[T=3] [B=1] [R=1]	[T=3] [B=1] [R=1]	[T=3] [B=1] [R=1]	[T=3] [B=1] [R=1]	[T=3] [B=1] [R=1]	[T=3] [B=1] [R=1]	[T=3] [B=1] [R=1]	[T=3] [B=1] [R=1]	[T=3] [B=1] [R=1]	[T=3] [B=1] [R=1]	[T=3] [B=1] [R=1]

Rxxx Value 1 row = 1 Cacheline	16 32-bit counters															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	[CB=0] [CT=0] [N=2]	[CB=0] [CT=0] [N=3]	[CB=0] [CT=1] [N=0]	[CB=0] [CT=1] [N=1]	[CB=0] [CT=1] [N=2]	[CB=0] [CT=1] [N=3]	[CB=0] [CT=2] [N=0]	[CB=0] [CT=2] [N=1]	[CB=0] [CT=2] [N=2]	[CB=0] [CT=2] [N=3]	[CB=1] [CT=0] [N=0]	[CB=1] [CT=0] [N=1]	[CB=1] [CT=0] [N=2]	[CB=1] [CT=0] [N=3]	[CB=1] [CT=1] [N=0]	[CB=1] [CT=1] [N=1]
R126	ct_coef															
	[T=3] [B=1] [R=1] [CB=1] [CT=1] [N=2]	[T=3] [B=1] [R=1] [CB=1] [CT=1] [N=3]	[T=3] [B=1] [R=1] [CB=1] [CT=2] [N=0]	[T=3] [B=1] [R=1] [CB=1] [CT=2] [N=1]	[T=3] [B=1] [R=1] [CB=1] [CT=2] [N=2]	[T=3] [B=1] [R=1] [CB=1] [CT=2] [N=3]	[T=3] [B=1] [R=1] [CB=1] [CT=3] [N=0]	[T=3] [B=1] [R=1] [CB=1] [CT=3] [N=1]	[T=3] [B=1] [R=1] [CB=1] [CT=3] [N=2]	[T=3] [B=1] [R=1] [CB=1] [CT=3] [N=3]	[T=3] [B=1] [R=1] [CB=1] [CT=4] [N=0]	[T=3] [B=1] [R=1] [CB=1] [CT=4] [N=1]	[T=3] [B=1] [R=1] [CB=1] [CT=4] [N=2]	[T=3] [B=1] [R=1] [CB=1] [CT=4] [N=3]	[T=3] [B=1] [R=1] [CB=1] [CT=5] [N=0]	[T=3] [B=1] [R=1] [CB=1] [CT=5] [N=1]
R127	ct_coef															
	[T=3] [B=1] [R=1] [CB=1] [CT=5] [N=2]	[T=3] [B=1] [R=1] [CB=1] [CT=5] [N=3]	[T=3] [B=1] [R=1] [CB=2] [CT=0] [N=0]	[T=3] [B=1] [R=1] [CB=2] [CT=0] [N=1]	[T=3] [B=1] [R=1] [CB=2] [CT=0] [N=2]	[T=3] [B=1] [R=1] [CB=2] [CT=0] [N=3]	[T=3] [B=1] [R=1] [CB=2] [CT=1] [N=0]	[T=3] [B=1] [R=1] [CB=2] [CT=1] [N=1]	[T=3] [B=1] [R=1] [CB=2] [CT=1] [N=2]	[T=3] [B=1] [R=1] [CB=2] [CT=1] [N=3]	[T=3] [B=1] [R=1] [CB=2] [CT=2] [N=0]	[T=3] [B=1] [R=1] [CB=2] [CT=2] [N=1]	[T=3] [B=1] [R=1] [CB=2] [CT=2] [N=2]	[T=3] [B=1] [R=1] [CB=2] [CT=2] [N=3]	[T=3] [B=1] [R=1] [CB=2] [CT=3] [N=0]	[T=3] [B=1] [R=1] [CB=2] [CT=3] [N=1]
R128	ct_coef															
	[T=3] [B=1] [R=1] [CB=2] [CT=3]	[T=3] [B=1] [R=1] [CB=2]	[T=3] [B=1] [R=1] [CB=2]	[T=3] [B=1] [R=1] [CB=2]	[T=3] [B=1] [R=1] [CB=2]	[T=3] [B=1] [R=1] [CB=2]	[T=3] [B=1] [R=1] [CB=2]	[T=3] [B=1] [R=1] [CB=2]	[T=3] [B=1] [R=1] [CB=2]	[T=3] [B=1] [R=1] [CB=2]	[T=3] [B=1] [R=1] [CB=3]	[T=3] [B=1] [R=1] [CB=3]	[T=3] [B=1] [R=1] [CB=3]	[T=3] [B=1] [R=1] [CB=3]	[T=3] [B=1] [R=1] [CB=3]	[T=3] [B=1] [R=1] [CB=3] [CT=1]

Rxxx Value 1 row = 1 Cacheline	16 32-bit counters															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	[N=2]	[CT=3] [N=3]	[CT=4] [N=0]	[CT=4] [N=1]	[CT=4] [N=2]	[CT=4] [N=3]	[CT=5] [N=0]	[CT=5] [N=1]	[CT=5] [N=2]	[CT=5] [N=3]	[CT=0] [N=0]	[CT=0] [N=1]	[CT=0] [N=2]	[CT=0] [N=3]	[CT=1] [N=0]	[N=1]
R129	ct_coef															
	[T=3] [B=1] [R=1] [CB=3] [CT=1] [N=2]	[T=3] [B=1] [R=1] [CB=3] [CT=1] [N=3]	[T=3] [B=1] [R=1] [CB=3] [CT=2] [N=0]	[T=3] [B=1] [R=1] [CB=3] [CT=2] [N=1]	[T=3] [B=1] [R=1] [CB=3] [CT=2] [N=2]	[T=3] [B=1] [R=1] [CB=3] [CT=2] [N=3]	[T=3] [B=1] [R=1] [CB=3] [CT=3] [N=0]	[T=3] [B=1] [R=1] [CB=3] [CT=3] [N=1]	[T=3] [B=1] [R=1] [CB=3] [CT=3] [N=2]	[T=3] [B=1] [R=1] [CB=3] [CT=3] [N=3]	[T=3] [B=1] [R=1] [CB=3] [CT=4] [N=0]	[T=3] [B=1] [R=1] [CB=3] [CT=4] [N=1]	[T=3] [B=1] [R=1] [CB=3] [CT=4] [N=2]	[T=3] [B=1] [R=1] [CB=3] [CT=4] [N=3]	[T=3] [B=1] [R=1] [CB=3] [CT=5] [N=0]	[T=3] [B=1] [R=1] [CB=3] [CT=5] [N=1]
R130	ct_coef															
	[T=3] [B=1] [R=1] [CB=3] [CT=5] [N=2]	[T=3] [B=1] [R=1] [CB=3] [CT=5] [N=3]	[T=3] [B=1] [R=1] [CB=4] [CT=0] [N=0]	[T=3] [B=1] [R=1] [CB=4] [CT=0] [N=1]	[T=3] [B=1] [R=1] [CB=4] [CT=0] [N=2]	[T=3] [B=1] [R=1] [CB=4] [CT=0] [N=3]	[T=3] [B=1] [R=1] [CB=4] [CT=1] [N=0]	[T=3] [B=1] [R=1] [CB=4] [CT=1] [N=1]	[T=3] [B=1] [R=1] [CB=4] [CT=1] [N=2]	[T=3] [B=1] [R=1] [CB=4] [CT=1] [N=3]	[T=3] [B=1] [R=1] [CB=4] [CT=2] [N=0]	[T=3] [B=1] [R=1] [CB=4] [CT=2] [N=1]	[T=3] [B=1] [R=1] [CB=4] [CT=2] [N=2]	[T=3] [B=1] [R=1] [CB=4] [CT=2] [N=3]	[T=3] [B=1] [R=1] [CB=4] [CT=3] [N=0]	[T=3] [B=1] [R=1] [CB=4] [CT=3] [N=1]
R131	ct_coef															
	[T=3] [B=1] [R=1] [CB=4] [CT=3] [N=2]	[T=3] [B=1] [R=1] [CB=4] [CT=3]	[T=3] [B=1] [R=1] [CB=4] [CT=4]	[T=3] [B=1] [R=1] [CB=4] [CT=4]	[T=3] [B=1] [R=1] [CB=4] [CT=4]	[T=3] [B=1] [R=1] [CB=4] [CT=4]	[T=3] [B=1] [R=1] [CB=4] [CT=5]	[T=3] [B=1] [R=1] [CB=4] [CT=5]	[T=3] [B=1] [R=1] [CB=4] [CT=5]	[T=3] [B=1] [R=1] [CB=4] [CT=5]	[T=3] [B=1] [R=1] [CB=5] [CT=0] [N=0]	[T=3] [B=1] [R=1] [CB=5] [CT=0] [N=1]	[T=3] [B=1] [R=1] [CB=5] [CT=0]	[T=3] [B=1] [R=1] [CB=5] [CT=0]	[T=3] [B=1] [R=1] [CB=5] [CT=1]	[T=3] [B=1] [R=1] [CB=5] [CT=1] [N=1]

Rxxx Value 1 row = 1 Cacheline	16 32-bit counters															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		[N=3]	[N=0]	[N=1]	[N=2]	[N=3]	[N=0]	[N=1]	[N=2]	[N=3]			[N=2]	[N=3]	[N=0]	
R132	ct_coef															
	[T=3] [B=1] [R=1] [CB=5] [CT=1] [N=2]	[T=3] [B=1] [R=1] [CB=5] [CT=1] [N=3]	[T=3] [B=1] [R=1] [CB=5] [CT=2] [N=0]	[T=3] [B=1] [R=1] [CB=5] [CT=2] [N=1]	[T=3] [B=1] [R=1] [CB=5] [CT=2] [N=2]	[T=3] [B=1] [R=1] [CB=5] [CT=2] [N=3]	[T=3] [B=1] [R=1] [CB=5] [CT=3] [N=0]	[T=3] [B=1] [R=1] [CB=5] [CT=3] [N=1]	[T=3] [B=1] [R=1] [CB=5] [CT=3] [N=2]	[T=3] [B=1] [R=1] [CB=5] [CT=3] [N=3]	[T=3] [B=1] [R=1] [CB=5] [CT=4] [N=0]	[T=3] [B=1] [R=1] [CB=5] [CT=4] [N=1]	[T=3] [B=1] [R=1] [CB=5] [CT=4] [N=2]	[T=3] [B=1] [R=1] [CB=5] [CT=4] [N=3]	[T=3] [B=1] [R=1] [CB=5] [CT=5] [N=0]	[T=3] [B=1] [R=1] [CB=5] [CT=5] [N=1]
R133	ct_coef		ct_mbskip						ct_inter_mode							
	[T=3] [B=1] [R=1] [CB=5] [CT=5] [N=2]	[T=3] [B=1] [R=1] [CB=5] [CT=5] [N=3]	[0] [0]	[0] [1]	[1] [0]	[1] [1]	[2] [0]	[2] [1]	[0] [0]	[0] [1]	[0] [2]	[0] [3]	[1] [0]	[1] [1]	[1] [2]	[1] [3]
R134	ct_inter_mode															
	[2] [0]	[2] [1]	[2] [2]	[2] [3]	[3] [0]	[3] [1]	[3] [2]	[3] [3]	[4] [0]	[4] [1]	[4] [2]	[4] [3]	[5] [0]	[5] [1]	[5] [2]	[5] [3]
R135	ct_inter_mode				ct_switchable_interp											
	[6] [0]	[6] [1]	[6] [2]	[6] [3]	[0] [0]	[0] [1]	[0] [2]	[1] [0]	[1] [1]	[1] [2]	[2] [0]	[2] [1]	[2] [2]	[3] [0]	[3] [1]	[3] [2]
R136	ct_intra_inter								ct_comp_inter							
	[0] [0]	[0] [1]	[1] [0]	[1] [1]	[2] [0]	[2] [1]	[3] [0]	[3] [1]	[0] [0]	[0] [1]	[1] [0]	[1] [1]	[2] [0]	[2] [1]	[3] [0]	[3] [1]

Rxxx Value 1 row = 1 Cacheline	16 32-bit counters															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R137	ct_comp_inter		ct_single_ref													
	[4] [0]	[4] [1]	[0] [0] [0]	[0] [0] [1]	[0] [1] [0]	[0] [1] [1]	[1] [0] [0]	[1] [0] [1]	[1] [1] [0]	[1] [1] [1]	[2] [0] [0]	[2] [0] [1]	[2] [1] [0]	[2] [1] [1]	[3] [0] [0]	[3] [0] [1]
R138	ct_single_ref						ct_comp_ref									
	[3] [1] [0]	[3] [1] [1]	[4] [0] [0]	[4] [0] [1]	[4] [1] [0]	[4] [1] [1]	[0] [0]	[0] [1]	[1] [0]	[1] [1]	[2] [0]	[2] [1]	[3] [0]	[3] [1]	[4] [0]	[4] [1]
R139	ct_y_mode															
	[0] [0]	[0] [1]	[0] [2]	[0] [3]	[0] [4]	[0] [5]	[0] [6]	[0] [7]	[0] [8]	[0] [9]	[1] [0]	[1] [1]	[1] [2]	[1] [3]	[1] [4]	[1] [5]
R140	ct_y_mode															
	[1] [6]	[1] [7]	[1] [8]	[1] [9]	[2] [0]	[2] [1]	[2] [2]	[2] [3]	[2] [4]	[2] [5]	[2] [6]	[2] [7]	[2] [8]	[2] [9]	[3] [0]	[3] [1]
R141	ct_y_mode								ct_partition							
	[3] [2]	[3] [3]	[3] [4]	[3] [5]	[3] [6]	[3] [7]	[3] [8]	[3] [9]	[0] [0]	[0] [1]	[0] [2]	[0] [3]	[1] [0]	[1] [1]	[1] [2]	[1] [3]
R142	ct_partition															
	[2] [0]	[2] [1]	[2] [2]	[2] [3]	[3] [0]	[3] [1]	[3] [2]	[3] [3]	[4] [0]	[4] [1]	[4] [2]	[4] [3]	[5] [0]	[5] [1]	[5] [2]	[5] [3]
R143	ct_partition															
	[6] [0]	[6] [1]	[6] [2]	[6] [3]	[7] [0]	[7] [1]	[7] [2]	[7] [3]	[8] [0]	[8] [1]	[8] [2]	[8] [3]	[9] [0]	[9] [1]	[9] [2]	[9] [3]
R144	ct_partition															
	[10] [0]	[10] [1]	[10] [2]	[10] [3]	[11] [0]	[11] [1]	[11] [2]	[11] [3]	[12] [0]	[12] [1]	[12] [2]	[12] [3]	[13] [0]	[13] [1]	[13] [2]	[13] [3]
R145	ct_partition								ct_mv_joints				ct_mv_sign		ct_mv_classes	

Rxxx Value 1 row = 1 Cacheline	16 32-bit counters															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	[14] [0]	[14] [1]	[14] [2]	[14] [3]	[15] [0]	[15] [1]	[15] [2]	[15] [3]	[0]	[1]	[2]	[3]	[0] [0]	[0] [1]	[0] [0]	[0] [1]
R146	ct_mv_classes									ct_mv_class0		ct_mv_bits				
	[0] [2]	[0] [3]	[0] [4]	[0] [5]	[0] [6]	[0] [7]	[0] [8]	[0] [9]	[0] [10]	[0] [0]	[0] [1]	[0] [0] [0]	[0] [0] [1]	[0] [1] [0]	[0] [1] [1]	[0] [2] [0]
R147	ct_mv_bits															ct_mv_sign
	[0] [2] [1]	[0] [3] [0]	[0] [3] [1]	[0] [4] [0]	[0] [4] [1]	[0] [5] [0]	[0] [5] [1]	[0] [6] [0]	[0] [6] [1]	[0] [7] [0]	[0] [7] [1]	[0] [8] [0]	[0] [8] [1]	[0] [9] [0]	[0] [9] [1]	[1] [0]
R148	ct_mv_sign	ct_mv_classes											ct_mv_class0		ct_mv_bits	
	[1] [1]	[1] [0]	[1] [1]	[1] [2]	[1] [3]	[1] [4]	[1] [5]	[1] [6]	[1] [7]	[1] [8]	[1] [9]	[1] [10]	[1] [0]	[1] [1]	[1] [0] [0]	[1] [0] [1]
R149	ct_mv_bits															
	[1] [1] [0]	[1] [1] [1]	[1] [2] [0]	[1] [2] [1]	[1] [3] [0]	[1] [3] [1]	[1] [4] [0]	[1] [4] [1]	[1] [5] [0]	[1] [5] [1]	[1] [6] [0]	[1] [6] [1]	[1] [7] [0]	[1] [7] [1]	[1] [8] [0]	[1] [8] [1]
R150	ct_mv_bits		ct_mv_class0_fp								ct_mv_fp				ct_mv_class0_fp	
	[1] [9] [0]	[1] [9] [1]	[0] [0] [0]	[0] [0] [1]	[0] [0] [2]	[0] [0] [3]	[0] [1] [0]	[0] [1] [1]	[0] [1] [2]	[0] [1] [3]	[0] [0]	[0] [1]	[0] [2]	[0] [3]	[1] [0] [0]	[1] [0] [1]
R151	ct_mv_class0_fp						ct_mv_fp				ct_mv_class0_hp		ct_mv_hp		ct_mv_class0_hp	
	[1] [0] [2]	[1] [0] [3]	[1] [1] [0]	[1] [1] [1]	[1] [1] [2]	[1] [1] [3]	[1] [0]	[1] [1]	[1] [2]	[1] [3]	[0] [0]	[0] [1]	[0] [0]	[0] [1]	[1] [0]	[1] [1]
R152	ct_mv_hp		ct_eob_br													

Rxxx Value 1 row = 1 Cacheline	16 32-bit counters															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	[1] [0]	[1] [1]	[T=0] [B=0] [R=0] [CB=0] [CT=0]	[T=0] [B=0] [R=0] [CB=0] [CT=1]	[T=0] [B=0] [R=0] [CB=0] [CT=2]	[T=0] [B=0] [R=0] [CB=1] [CT=0]	[T=0] [B=0] [R=0] [CB=1] [CT=1]	[T=0] [B=0] [R=0] [CB=1] [CT=2]	[T=0] [B=0] [R=0] [CB=1] [CT=3]	[T=0] [B=0] [R=0] [CB=1] [CT=4]	[T=0] [B=0] [R=0] [CB=1] [CT=5]	[T=0] [B=0] [R=0] [CB=2] [CT=0]	[T=0] [B=0] [R=0] [CB=2] [CT=1]	[T=0] [B=0] [R=0] [CB=2] [CT=2]	[T=0] [B=0] [R=0] [CB=2] [CT=3]	[T=0] [B=0] [R=0] [CB=2] [CT=4]
R153	ct_eob_br															
	[T=0] [B=0] [R=0] [CB=2] [CT=5]	[T=0] [B=0] [R=0] [CB=3] [CT=0]	[T=0] [B=0] [R=0] [CB=3] [CT=1]	[T=0] [B=0] [R=0] [CB=3] [CT=2]	[T=0] [B=0] [R=0] [CB=3] [CT=3]	[T=0] [B=0] [R=0] [CB=3] [CT=4]	[T=0] [B=0] [R=0] [CB=3] [CT=5]	[T=0] [B=0] [R=0] [CB=4] [CT=0]	[T=0] [B=0] [R=0] [CB=4] [CT=1]	[T=0] [B=0] [R=0] [CB=4] [CT=2]	[T=0] [B=0] [R=0] [CB=4] [CT=3]	[T=0] [B=0] [R=0] [CB=4] [CT=4]	[T=0] [B=0] [R=0] [CB=4] [CT=5]	[T=0] [B=0] [R=0] [CB=5] [CT=0]	[T=0] [B=0] [R=0] [CB=5] [CT=1]	[T=0] [B=0] [R=0] [CB=5] [CT=2]
R154	ct_eob_br															
	[T=0] [B=0] [R=0] [CB=5] [CT=3]	[T=0] [B=0] [R=0] [CB=5] [CT=4]	[T=0] [B=0] [R=0] [CB=5] [CT=5]	[T=0] [B=0] [R=1] [CB=0] [CT=0]	[T=0] [B=0] [R=1] [CB=0] [CT=1]	[T=0] [B=0] [R=1] [CB=0] [CT=2]	[T=0] [B=0] [R=1] [CB=1] [CT=0]	[T=0] [B=0] [R=1] [CB=1] [CT=1]	[T=0] [B=0] [R=1] [CB=1] [CT=2]	[T=0] [B=0] [R=1] [CB=1] [CT=3]	[T=0] [B=0] [R=1] [CB=1] [CT=4]	[T=0] [B=0] [R=1] [CB=1] [CT=5]	[T=0] [B=0] [R=1] [CB=2] [CT=0]	[T=0] [B=0] [R=1] [CB=2] [CT=1]	[T=0] [B=0] [R=1] [CB=2] [CT=2]	[T=0] [B=0] [R=1] [CB=2] [CT=3]
R155	ct_eob_br															
	[T=0] [B=0] [R=1] [CB=2] [CT=4]	[T=0] [B=0] [R=1] [CB=2]	[T=0] [B=0] [R=1] [CB=3]	[T=0] [B=0] [R=1] [CB=3]	[T=0] [B=0] [R=1] [CB=3]	[T=0] [B=0] [R=1] [CB=3]	[T=0] [B=0] [R=1] [CB=3]	[T=0] [B=0] [R=1] [CB=3]	[T=0] [B=0] [R=1] [CB=4]	[T=0] [B=0] [R=1] [CB=4]	[T=0] [B=0] [R=1] [CB=4]	[T=0] [B=0] [R=1] [CB=4]	[T=0] [B=0] [R=1] [CB=4]	[T=0] [B=0] [R=1] [CB=4]	[T=0] [B=0] [R=1] [CB=5]	[T=0] [B=0] [R=1] [CB=5] [CT=1]

Rxxx Value 1 row = 1 Cacheline	16 32-bit counters															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		[CT=5]	[CT=0]	[CT=1]	[CT=2]	[CT=3]	[CT=4]	[CT=5]	[CT=0]	[CT=1]	[CT=2]	[CT=3]	[CT=4]	[CT=5]	[CT=0]	
R156	ct_eob_br															
	[T=0] [B=0] [R=1] [CB=5] [CT=2]	[T=0] [B=0] [R=1] [CB=5] [CT=3]	[T=0] [B=0] [R=1] [CB=5] [CT=4]	[T=0] [B=0] [R=1] [CB=5] [CT=5]	[T=0] [B=1] [R=0] [CB=0] [CT=0]	[T=0] [B=1] [R=0] [CB=0] [CT=1]	[T=0] [B=1] [R=0] [CB=0] [CT=2]	[T=0] [B=1] [R=0] [CB=1] [CT=0]	[T=0] [B=1] [R=0] [CB=1] [CT=1]	[T=0] [B=1] [R=0] [CB=1] [CT=2]	[T=0] [B=1] [R=0] [CB=1] [CT=3]	[T=0] [B=1] [R=0] [CB=1] [CT=4]	[T=0] [B=1] [R=0] [CB=1] [CT=5]	[T=0] [B=1] [R=0] [CB=2] [CT=0]	[T=0] [B=1] [R=0] [CB=2] [CT=1]	[T=0] [B=1] [R=0] [CB=2] [CT=2]
R157	ct_eob_br															
	[T=0] [B=1] [R=0] [CB=2] [CT=3]	[T=0] [B=1] [R=0] [CB=2] [CT=4]	[T=0] [B=1] [R=0] [CB=2] [CT=5]	[T=0] [B=1] [R=0] [CB=3] [CT=0]	[T=0] [B=1] [R=0] [CB=3] [CT=1]	[T=0] [B=1] [R=0] [CB=3] [CT=2]	[T=0] [B=1] [R=0] [CB=3] [CT=3]	[T=0] [B=1] [R=0] [CB=3] [CT=4]	[T=0] [B=1] [R=0] [CB=3] [CT=5]	[T=0] [B=1] [R=0] [CB=4] [CT=0]	[T=0] [B=1] [R=0] [CB=4] [CT=1]	[T=0] [B=1] [R=0] [CB=4] [CT=2]	[T=0] [B=1] [R=0] [CB=4] [CT=3]	[T=0] [B=1] [R=0] [CB=4] [CT=4]	[T=0] [B=1] [R=0] [CB=4] [CT=5]	[T=0] [B=1] [R=0] [CB=5] [CT=0]
R158	ct_eob_br															
	[T=0] [B=1] [R=0] [CB=5] [CT=1]	[T=0] [B=1] [R=0] [CB=5] [CT=2]	[T=0] [B=1] [R=0] [CB=5] [CT=3]	[T=0] [B=1] [R=0] [CB=5] [CT=4]	[T=0] [B=1] [R=0] [CB=5] [CT=5]	[T=0] [B=1] [R=1] [CB=0] [CT=0]	[T=0] [B=1] [R=1] [CB=0] [CT=1]	[T=0] [B=1] [R=1] [CB=0] [CT=2]	[T=0] [B=1] [R=1] [CB=1] [CT=0]	[T=0] [B=1] [R=1] [CB=1] [CT=1]	[T=0] [B=1] [R=1] [CB=1] [CT=2]	[T=0] [B=1] [R=1] [CB=1] [CT=3]	[T=0] [B=1] [R=1] [CB=1] [CT=4]	[T=0] [B=1] [R=1] [CB=1] [CT=5]	[T=0] [B=1] [R=1] [CB=2] [CT=0]	[T=0] [B=1] [R=1] [CB=2] [CT=1]
R159	ct_eob_br															
	[T=0] [B=1]	[T=0] [B=1]	[T=0] [B=1]	[T=0] [B=1]	[T=0] [B=1]	[T=0] [B=1]	[T=0] [B=1]	[T=0] [B=1]	[T=0] [B=1]	[T=0] [B=1]	[T=0] [B=1]	[T=0] [B=1]	[T=0] [B=1]	[T=0] [B=1]	[T=0] [B=1]	[T=0] [B=1]

Rxxx Value 1 row = 1 Cacheline	16 32-bit counters															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	[R=1] [CB=2] [CT=2]	[R=1] [CB=2] [CT=3]	[R=1] [CB=2] [CT=4]	[R=1] [CB=2] [CT=5]	[R=1] [CB=3] [CT=0]	[R=1] [CB=3] [CT=1]	[R=1] [CB=3] [CT=2]	[R=1] [CB=3] [CT=3]	[R=1] [CB=3] [CT=4]	[R=1] [CB=3] [CT=5]	[R=1] [CB=4] [CT=0]	[R=1] [CB=4] [CT=1]	[R=1] [CB=4] [CT=2]	[R=1] [CB=4] [CT=3]	[R=1] [CB=4] [CT=4]	[R=1] [CB=4] [CT=5]
R160	ct_eob_br															
	[T=0] [B=1] [R=1] [CB=5] [CT=0]	[T=0] [B=1] [R=1] [CB=5] [CT=1]	[T=0] [B=1] [R=1] [CB=5] [CT=2]	[T=0] [B=1] [R=1] [CB=5] [CT=3]	[T=0] [B=1] [R=1] [CB=5] [CT=4]	[T=0] [B=1] [R=1] [CB=5] [CT=5]	[T=1] [B=0] [R=0] [CB=0] [CT=0]	[T=1] [B=0] [R=0] [CB=0] [CT=1]	[T=1] [B=0] [R=0] [CB=0] [CT=2]	[T=1] [B=0] [R=0] [CB=1] [CT=0]	[T=1] [B=0] [R=0] [CB=1] [CT=1]	[T=1] [B=0] [R=0] [CB=1] [CT=2]	[T=1] [B=0] [R=0] [CB=1] [CT=3]	[T=1] [B=0] [R=0] [CB=1] [CT=4]	[T=1] [B=0] [R=0] [CB=1] [CT=5]	[T=1] [B=0] [R=0] [CB=2] [CT=0]
R161	ct_eob_br															
	[T=1] [B=0] [R=0] [CB=2] [CT=1]	[T=1] [B=0] [R=0] [CB=2] [CT=2]	[T=1] [B=0] [R=0] [CB=2] [CT=3]	[T=1] [B=0] [R=0] [CB=2] [CT=4]	[T=1] [B=0] [R=0] [CB=2] [CT=5]	[T=1] [B=0] [R=0] [CB=3] [CT=0]	[T=1] [B=0] [R=0] [CB=3] [CT=1]	[T=1] [B=0] [R=0] [CB=3] [CT=2]	[T=1] [B=0] [R=0] [CB=3] [CT=3]	[T=1] [B=0] [R=0] [CB=3] [CT=4]	[T=1] [B=0] [R=0] [CB=3] [CT=5]	[T=1] [B=0] [R=0] [CB=4] [CT=0]	[T=1] [B=0] [R=0] [CB=4] [CT=1]	[T=1] [B=0] [R=0] [CB=4] [CT=2]	[T=1] [B=0] [R=0] [CB=4] [CT=3]	[T=1] [B=0] [R=0] [CB=4] [CT=4]
R162	ct_eob_br															
	[T=1] [B=0] [R=0] [CB=4] [CT=5]	[T=1] [B=0] [R=0] [CB=5] [CT=0]	[T=1] [B=0] [R=0] [CB=5] [CT=1]	[T=1] [B=0] [R=0] [CB=5] [CT=2]	[T=1] [B=0] [R=0] [CB=5] [CT=3]	[T=1] [B=0] [R=0] [CB=5] [CT=4]	[T=1] [B=0] [R=0] [CB=5] [CT=5]	[T=1] [B=0] [R=1] [CB=0] [CT=0]	[T=1] [B=0] [R=1] [CB=0] [CT=1]	[T=1] [B=0] [R=1] [CB=0] [CT=2]	[T=1] [B=0] [R=1] [CB=1] [CT=0]	[T=1] [B=0] [R=1] [CB=1] [CT=1]	[T=1] [B=0] [R=1] [CB=1] [CT=2]	[T=1] [B=0] [R=1] [CB=1] [CT=3]	[T=1] [B=0] [R=1] [CB=1] [CT=4]	[T=1] [B=0] [R=1] [CB=1] [CT=5]

Rxxx Value 1 row = 1 Cacheline	16 32-bit counters															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R163	ct_eob_br															
	[T=1] [B=0] [R=1] [CB=2] [CT=0]	[T=1] [B=0] [R=1] [CB=2] [CT=1]	[T=1] [B=0] [R=1] [CB=2] [CT=2]	[T=1] [B=0] [R=1] [CB=2] [CT=3]	[T=1] [B=0] [R=1] [CB=2] [CT=4]	[T=1] [B=0] [R=1] [CB=2] [CT=5]	[T=1] [B=0] [R=1] [CB=3] [CT=0]	[T=1] [B=0] [R=1] [CB=3] [CT=1]	[T=1] [B=0] [R=1] [CB=3] [CT=2]	[T=1] [B=0] [R=1] [CB=3] [CT=3]	[T=1] [B=0] [R=1] [CB=3] [CT=4]	[T=1] [B=0] [R=1] [CB=3] [CT=5]	[T=1] [B=0] [R=1] [CB=4] [CT=0]	[T=1] [B=0] [R=1] [CB=4] [CT=1]	[T=1] [B=0] [R=1] [CB=4] [CT=2]	[T=1] [B=0] [R=1] [CB=4] [CT=3]
R164	ct_eob_br															
	[T=1] [B=0] [R=1] [CB=4] [CT=4]	[T=1] [B=0] [R=1] [CB=4] [CT=5]	[T=1] [B=0] [R=1] [CB=5] [CT=0]	[T=1] [B=0] [R=1] [CB=5] [CT=1]	[T=1] [B=0] [R=1] [CB=5] [CT=2]	[T=1] [B=0] [R=1] [CB=5] [CT=3]	[T=1] [B=0] [R=1] [CB=5] [CT=4]	[T=1] [B=0] [R=1] [CB=5] [CT=5]	[T=1] [B=1] [R=0] [CB=0] [CT=0]	[T=1] [B=1] [R=0] [CB=0] [CT=1]	[T=1] [B=1] [R=0] [CB=0] [CT=2]	[T=1] [B=1] [R=0] [CB=1] [CT=0]	[T=1] [B=1] [R=0] [CB=1] [CT=1]	[T=1] [B=1] [R=0] [CB=1] [CT=2]	[T=1] [B=1] [R=0] [CB=1] [CT=3]	[T=1] [B=1] [R=0] [CB=1] [CT=4]
R165	ct_eob_br															
	[T=1] [B=1] [R=0] [CB=1] [CT=5]	[T=1] [B=1] [R=0] [CB=2] [CT=0]	[T=1] [B=1] [R=0] [CB=2] [CT=1]	[T=1] [B=1] [R=0] [CB=2] [CT=2]	[T=1] [B=1] [R=0] [CB=2] [CT=3]	[T=1] [B=1] [R=0] [CB=2] [CT=4]	[T=1] [B=1] [R=0] [CB=2] [CT=5]	[T=1] [B=1] [R=0] [CB=3] [CT=0]	[T=1] [B=1] [R=0] [CB=3] [CT=1]	[T=1] [B=1] [R=0] [CB=3] [CT=2]	[T=1] [B=1] [R=0] [CB=3] [CT=3]	[T=1] [B=1] [R=0] [CB=3] [CT=4]	[T=1] [B=1] [R=0] [CB=3] [CT=5]	[T=1] [B=1] [R=0] [CB=4] [CT=0]	[T=1] [B=1] [R=0] [CB=4] [CT=1]	[T=1] [B=1] [R=0] [CB=4] [CT=2]
R166	ct_eob_br															
	[T=1] [B=1] [R=0] [CB=4]	[T=1] [B=1] [R=0]	[T=1] [B=1] [R=0]	[T=1] [B=1] [R=0]	[T=1] [B=1] [R=0]	[T=1] [B=1] [R=0]	[T=1] [B=1] [R=0]	[T=1] [B=1] [R=0]	[T=1] [B=1] [R=0]	[T=1] [B=1] [R=1]	[T=1] [B=1] [R=1]	[T=1] [B=1] [R=1]	[T=1] [B=1] [R=1]	[T=1] [B=1] [R=1]	[T=1] [B=1] [R=1]	[T=1] [B=1] [R=1] [CB=1]

Rxxx Value 1 row = 1 Cacheline	16 32-bit counters															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	[CT=3]	[CB=4] [CT=4]	[CB=4] [CT=5]	[CB=5] [CT=0]	[CB=5] [CT=1]	[CB=5] [CT=2]	[CB=5] [CT=3]	[CB=5] [CT=4]	[CB=5] [CT=5]	[CB=0] [CT=0]	[CB=0] [CT=1]	[CB=0] [CT=2]	[CB=1] [CT=0]	[CB=1] [CT=1]	[CB=1] [CT=2]	[CT=3]
R167	ct_eob_br															
	[T=1] [B=1] [R=1] [CB=1] [CT=4]	[T=1] [B=1] [R=1] [CB=1] [CT=5]	[T=1] [B=1] [R=1] [CB=2] [CT=0]	[T=1] [B=1] [R=1] [CB=2] [CT=1]	[T=1] [B=1] [R=1] [CB=2] [CT=2]	[T=1] [B=1] [R=1] [CB=2] [CT=3]	[T=1] [B=1] [R=1] [CB=2] [CT=4]	[T=1] [B=1] [R=1] [CB=2] [CT=5]	[T=1] [B=1] [R=1] [CB=3] [CT=0]	[T=1] [B=1] [R=1] [CB=3] [CT=1]	[T=1] [B=1] [R=1] [CB=3] [CT=2]	[T=1] [B=1] [R=1] [CB=3] [CT=3]	[T=1] [B=1] [R=1] [CB=3] [CT=4]	[T=1] [B=1] [R=1] [CB=3] [CT=5]	[T=1] [B=1] [R=1] [CB=4] [CT=0]	[T=1] [B=1] [R=1] [CB=4] [CT=1]
R168	ct_eob_br															
	[T=1] [B=1] [R=1] [CB=4] [CT=2]	[T=1] [B=1] [R=1] [CB=4] [CT=3]	[T=1] [B=1] [R=1] [CB=4] [CT=4]	[T=1] [B=1] [R=1] [CB=4] [CT=5]	[T=1] [B=1] [R=1] [CB=5] [CT=0]	[T=1] [B=1] [R=1] [CB=5] [CT=1]	[T=1] [B=1] [R=1] [CB=5] [CT=2]	[T=1] [B=1] [R=1] [CB=5] [CT=3]	[T=1] [B=1] [R=1] [CB=5] [CT=4]	[T=1] [B=1] [R=1] [CB=5] [CT=5]	[T=2] [B=0] [R=0] [CB=0] [CT=0]	[T=2] [B=0] [R=0] [CB=0] [CT=1]	[T=2] [B=0] [R=0] [CB=0] [CT=2]	[T=2] [B=0] [R=0] [CB=1] [CT=0]	[T=2] [B=0] [R=0] [CB=1] [CT=1]	[T=2] [B=0] [R=0] [CB=1] [CT=2]
R169	ct_eob_br															
	[T=2] [B=0] [R=0] [CB=1] [CT=3]	[T=2] [B=0] [R=0] [CB=1] [CT=4]	[T=2] [B=0] [R=0] [CB=1] [CT=5]	[T=2] [B=0] [R=0] [CB=2] [CT=0]	[T=2] [B=0] [R=0] [CB=2] [CT=1]	[T=2] [B=0] [R=0] [CB=2] [CT=2]	[T=2] [B=0] [R=0] [CB=2] [CT=3]	[T=2] [B=0] [R=0] [CB=2] [CT=4]	[T=2] [B=0] [R=0] [CB=2] [CT=5]	[T=2] [B=0] [R=0] [CB=3] [CT=0]	[T=2] [B=0] [R=0] [CB=3] [CT=1]	[T=2] [B=0] [R=0] [CB=3] [CT=2]	[T=2] [B=0] [R=0] [CB=3] [CT=3]	[T=2] [B=0] [R=0] [CB=3] [CT=4]	[T=2] [B=0] [R=0] [CB=3] [CT=5]	[T=2] [B=0] [R=0] [CB=4] [CT=0]
R170	ct_eob_br															
	[T=2]	[T=2]	[T=2]	[T=2]	[T=2]	[T=2]	[T=2]	[T=2]	[T=2]	[T=2]	[T=2]	[T=2]	[T=2]	[T=2]	[T=2]	[T=2]

Rxxx Value 1 row = 1 Cacheline	16 32-bit counters															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	[B=0] [R=0] [CB=4] [CT=1]	[B=0] [R=0] [CB=4] [CT=2]	[B=0] [R=0] [CB=4] [CT=3]	[B=0] [R=0] [CB=4] [CT=4]	[B=0] [R=0] [CB=4] [CT=5]	[B=0] [R=0] [CB=5] [CT=0]	[B=0] [R=0] [CB=5] [CT=1]	[B=0] [R=0] [CB=5] [CT=2]	[B=0] [R=0] [CB=5] [CT=3]	[B=0] [R=0] [CB=5] [CT=4]	[B=0] [R=0] [CB=5] [CT=5]	[B=0] [R=1] [CB=0] [CT=0]	[B=0] [R=1] [CB=0] [CT=1]	[B=0] [R=1] [CB=0] [CT=2]	[B=0] [R=1] [CB=1] [CT=0]	[B=0] [R=1] [CB=1] [CT=1]
R171	ct_eob_br															
	[T=2] [B=0] [R=1] [CB=1] [CT=2]	[T=2] [B=0] [R=1] [CB=1] [CT=3]	[T=2] [B=0] [R=1] [CB=1] [CT=4]	[T=2] [B=0] [R=1] [CB=1] [CT=5]	[T=2] [B=0] [R=1] [CB=2] [CT=0]	[T=2] [B=0] [R=1] [CB=2] [CT=1]	[T=2] [B=0] [R=1] [CB=2] [CT=2]	[T=2] [B=0] [R=1] [CB=2] [CT=3]	[T=2] [B=0] [R=1] [CB=2] [CT=4]	[T=2] [B=0] [R=1] [CB=2] [CT=5]	[T=2] [B=0] [R=1] [CB=3] [CT=0]	[T=2] [B=0] [R=1] [CB=3] [CT=1]	[T=2] [B=0] [R=1] [CB=3] [CT=2]	[T=2] [B=0] [R=1] [CB=3] [CT=3]	[T=2] [B=0] [R=1] [CB=3] [CT=4]	[T=2] [B=0] [R=1] [CB=3] [CT=5]
R172	ct_eob_br															
	[T=2] [B=0] [R=1] [CB=4] [CT=0]	[T=2] [B=0] [R=1] [CB=4] [CT=1]	[T=2] [B=0] [R=1] [CB=4] [CT=2]	[T=2] [B=0] [R=1] [CB=4] [CT=3]	[T=2] [B=0] [R=1] [CB=4] [CT=4]	[T=2] [B=0] [R=1] [CB=4] [CT=5]	[T=2] [B=0] [R=1] [CB=5] [CT=0]	[T=2] [B=0] [R=1] [CB=5] [CT=1]	[T=2] [B=0] [R=1] [CB=5] [CT=2]	[T=2] [B=0] [R=1] [CB=5] [CT=3]	[T=2] [B=0] [R=1] [CB=5] [CT=4]	[T=2] [B=0] [R=1] [CB=5] [CT=5]	[T=2] [B=1] [R=0] [CB=0] [CT=0]	[T=2] [B=1] [R=0] [CB=0] [CT=1]	[T=2] [B=1] [R=0] [CB=0] [CT=2]	[T=2] [B=1] [R=0] [CB=1] [CT=0]
R173	ct_eob_br															
	[T=2] [B=1] [R=0] [CB=1] [CT=1]	[T=2] [B=1] [R=0] [CB=1]	[T=2] [B=1] [R=0] [CB=1]	[T=2] [B=1] [R=0] [CB=1]	[T=2] [B=1] [R=0] [CB=1]	[T=2] [B=1] [R=0] [CB=2]	[T=2] [B=1] [R=0] [CB=2]	[T=2] [B=1] [R=0] [CB=2]	[T=2] [B=1] [R=0] [CB=2]	[T=2] [B=1] [R=0] [CB=2]	[T=2] [B=1] [R=0] [CB=2] [CT=5]	[T=2] [B=1] [R=0] [CB=3] [CT=0]	[T=2] [B=1] [R=0] [CB=3]	[T=2] [B=1] [R=0] [CB=3]	[T=2] [B=1] [R=0] [CB=3]	[T=2] [B=1] [R=0] [CB=3] [CT=4]

Rxxx Value 1 row = 1 Cacheline	16 32-bit counters															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		[CT=2]	[CT=3]	[CT=4]	[CT=5]	[CT=0]	[CT=1]	[CT=2]	[CT=3]	[CT=4]			[CT=1]	[CT=2]	[CT=3]	
R174	ct_eob_br															
	[T=2] [B=1] [R=0] [CB=3] [CT=5]	[T=2] [B=1] [R=0] [CB=4] [CT=0]	[T=2] [B=1] [R=0] [CB=4] [CT=1]	[T=2] [B=1] [R=0] [CB=4] [CT=2]	[T=2] [B=1] [R=0] [CB=4] [CT=3]	[T=2] [B=1] [R=0] [CB=4] [CT=4]	[T=2] [B=1] [R=0] [CB=4] [CT=5]	[T=2] [B=1] [R=0] [CB=5] [CT=0]	[T=2] [B=1] [R=0] [CB=5] [CT=1]	[T=2] [B=1] [R=0] [CB=5] [CT=2]	[T=2] [B=1] [R=0] [CB=5] [CT=3]	[T=2] [B=1] [R=0] [CB=5] [CT=4]	[T=2] [B=1] [R=0] [CB=5] [CT=5]	[T=2] [B=1] [R=1] [CB=0] [CT=0]	[T=2] [B=1] [R=1] [CB=0] [CT=1]	[T=2] [B=1] [R=1] [CB=0] [CT=2]
R175	ct_eob_br															
	[T=2] [B=1] [R=1] [CB=1] [CT=0]	[T=2] [B=1] [R=1] [CB=1] [CT=1]	[T=2] [B=1] [R=1] [CB=1] [CT=2]	[T=2] [B=1] [R=1] [CB=1] [CT=3]	[T=2] [B=1] [R=1] [CB=1] [CT=4]	[T=2] [B=1] [R=1] [CB=1] [CT=5]	[T=2] [B=1] [R=1] [CB=2] [CT=0]	[T=2] [B=1] [R=1] [CB=2] [CT=1]	[T=2] [B=1] [R=1] [CB=2] [CT=2]	[T=2] [B=1] [R=1] [CB=2] [CT=3]	[T=2] [B=1] [R=1] [CB=2] [CT=4]	[T=2] [B=1] [R=1] [CB=2] [CT=5]	[T=2] [B=1] [R=1] [CB=3] [CT=0]	[T=2] [B=1] [R=1] [CB=3] [CT=1]	[T=2] [B=1] [R=1] [CB=3] [CT=2]	[T=2] [B=1] [R=1] [CB=3] [CT=3]
R176	ct_eob_br															
	[T=2] [B=1] [R=1] [CB=3] [CT=4]	[T=2] [B=1] [R=1] [CB=3] [CT=5]	[T=2] [B=1] [R=1] [CB=4] [CT=0]	[T=2] [B=1] [R=1] [CB=4] [CT=1]	[T=2] [B=1] [R=1] [CB=4] [CT=2]	[T=2] [B=1] [R=1] [CB=4] [CT=3]	[T=2] [B=1] [R=1] [CB=4] [CT=4]	[T=2] [B=1] [R=1] [CB=4] [CT=5]	[T=2] [B=1] [R=1] [CB=5] [CT=0]	[T=2] [B=1] [R=1] [CB=5] [CT=1]	[T=2] [B=1] [R=1] [CB=5] [CT=2]	[T=2] [B=1] [R=1] [CB=5] [CT=3]	[T=2] [B=1] [R=1] [CB=5] [CT=4]	[T=2] [B=1] [R=1] [CB=5] [CT=5]	[T=3] [B=0] [R=0] [CB=0] [CT=0]	[T=3] [B=0] [R=0] [CB=0] [CT=1]
R177	ct_eob_br															
	[T=3] [B=0] [R=0]	[T=3] [B=0] [R=0]	[T=3] [B=0] [R=0]	[T=3] [B=0] [R=0]	[T=3] [B=0] [R=0]	[T=3] [B=0] [R=0]	[T=3] [B=0] [R=0]	[T=3] [B=0] [R=0]	[T=3] [B=0] [R=0]	[T=3] [B=0] [R=0]	[T=3] [B=0] [R=0]	[T=3] [B=0] [R=0]	[T=3] [B=0] [R=0]	[T=3] [B=0] [R=0]	[T=3] [B=0] [R=0]	[T=3] [B=0] [R=0]

Rxxx Value 1 row = 1 Cacheline	16 32-bit counters															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	[CB=0] [CT=2]	[CB=1] [CT=0]	[CB=1] [CT=1]	[CB=1] [CT=2]	[CB=1] [CT=3]	[CB=1] [CT=4]	[CB=1] [CT=5]	[CB=2] [CT=0]	[CB=2] [CT=1]	[CB=2] [CT=2]	[CB=2] [CT=3]	[CB=2] [CT=4]	[CB=2] [CT=5]	[CB=3] [CT=0]	[CB=3] [CT=1]	[CB=3] [CT=2]
R178	ct_eob_br															
	[T=3] [B=0] [R=0] [CB=3] [CT=3]	[T=3] [B=0] [R=0] [CB=3] [CT=4]	[T=3] [B=0] [R=0] [CB=3] [CT=5]	[T=3] [B=0] [R=0] [CB=4] [CT=0]	[T=3] [B=0] [R=0] [CB=4] [CT=1]	[T=3] [B=0] [R=0] [CB=4] [CT=2]	[T=3] [B=0] [R=0] [CB=4] [CT=3]	[T=3] [B=0] [R=0] [CB=4] [CT=4]	[T=3] [B=0] [R=0] [CB=4] [CT=5]	[T=3] [B=0] [R=0] [CB=5] [CT=0]	[T=3] [B=0] [R=0] [CB=5] [CT=1]	[T=3] [B=0] [R=0] [CB=5] [CT=2]	[T=3] [B=0] [R=0] [CB=5] [CT=3]	[T=3] [B=0] [R=0] [CB=5] [CT=4]	[T=3] [B=0] [R=0] [CB=5] [CT=5]	[T=3] [B=0] [R=1] [CB=0] [CT=0]
R179	ct_eob_br															
	[T=3] [B=0] [R=1] [CB=0] [CT=1]	[T=3] [B=0] [R=1] [CB=0] [CT=2]	[T=3] [B=0] [R=1] [CB=1] [CT=0]	[T=3] [B=0] [R=1] [CB=1] [CT=1]	[T=3] [B=0] [R=1] [CB=1] [CT=2]	[T=3] [B=0] [R=1] [CB=1] [CT=3]	[T=3] [B=0] [R=1] [CB=1] [CT=4]	[T=3] [B=0] [R=1] [CB=1] [CT=5]	[T=3] [B=0] [R=1] [CB=2] [CT=0]	[T=3] [B=0] [R=1] [CB=2] [CT=1]	[T=3] [B=0] [R=1] [CB=2] [CT=2]	[T=3] [B=0] [R=1] [CB=2] [CT=3]	[T=3] [B=0] [R=1] [CB=2] [CT=4]	[T=3] [B=0] [R=1] [CB=2] [CT=5]	[T=3] [B=0] [R=1] [CB=3] [CT=0]	[T=3] [B=0] [R=1] [CB=3] [CT=1]
R180	ct_eob_br															
	[T=3] [B=0] [R=1] [CB=3] [CT=2]	[T=3] [B=0] [R=1] [CB=3] [CT=3]	[T=3] [B=0] [R=1] [CB=3] [CT=4]	[T=3] [B=0] [R=1] [CB=3] [CT=5]	[T=3] [B=0] [R=1] [CB=4] [CT=0]	[T=3] [B=0] [R=1] [CB=4] [CT=1]	[T=3] [B=0] [R=1] [CB=4] [CT=2]	[T=3] [B=0] [R=1] [CB=4] [CT=3]	[T=3] [B=0] [R=1] [CB=4] [CT=4]	[T=3] [B=0] [R=1] [CB=4] [CT=5]	[T=3] [B=0] [R=1] [CB=5] [CT=0]	[T=3] [B=0] [R=1] [CB=5] [CT=1]	[T=3] [B=0] [R=1] [CB=5] [CT=2]	[T=3] [B=0] [R=1] [CB=5] [CT=3]	[T=3] [B=0] [R=1] [CB=5] [CT=4]	[T=3] [B=0] [R=1] [CB=5] [CT=5]
R181	ct_eob_br															

Rxxx Value 1 row = 1 Cacheline	16 32-bit counters															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	[T=3] [B=1] [R=0] [CB=0] [CT=0]	[T=3] [B=1] [R=0] [CB=0] [CT=1]	[T=3] [B=1] [R=0] [CB=0] [CT=2]	[T=3] [B=1] [R=0] [CB=1] [CT=0]	[T=3] [B=1] [R=0] [CB=1] [CT=1]	[T=3] [B=1] [R=0] [CB=1] [CT=2]	[T=3] [B=1] [R=0] [CB=1] [CT=3]	[T=3] [B=1] [R=0] [CB=1] [CT=4]	[T=3] [B=1] [R=0] [CB=1] [CT=5]	[T=3] [B=1] [R=0] [CB=2] [CT=0]	[T=3] [B=1] [R=0] [CB=2] [CT=1]	[T=3] [B=1] [R=0] [CB=2] [CT=2]	[T=3] [B=1] [R=0] [CB=2] [CT=3]	[T=3] [B=1] [R=0] [CB=2] [CT=4]	[T=3] [B=1] [R=0] [CB=2] [CT=5]	[T=3] [B=1] [R=0] [CB=3] [CT=0]
R182	ct_eob_br															
	[T=3] [B=1] [R=0] [CB=3] [CT=1]	[T=3] [B=1] [R=0] [CB=3] [CT=2]	[T=3] [B=1] [R=0] [CB=3] [CT=3]	[T=3] [B=1] [R=0] [CB=3] [CT=4]	[T=3] [B=1] [R=0] [CB=3] [CT=5]	[T=3] [B=1] [R=0] [CB=4] [CT=0]	[T=3] [B=1] [R=0] [CB=4] [CT=1]	[T=3] [B=1] [R=0] [CB=4] [CT=2]	[T=3] [B=1] [R=0] [CB=4] [CT=3]	[T=3] [B=1] [R=0] [CB=4] [CT=4]	[T=3] [B=1] [R=0] [CB=4] [CT=5]	[T=3] [B=1] [R=0] [CB=5] [CT=0]	[T=3] [B=1] [R=0] [CB=5] [CT=1]	[T=3] [B=1] [R=0] [CB=5] [CT=2]	[T=3] [B=1] [R=0] [CB=5] [CT=3]	[T=3] [B=1] [R=0] [CB=5] [CT=4]
R183	ct_eob_br															
	[T=3] [B=1] [R=0] [CB=5] [CT=5]	[T=3] [B=1] [R=1] [CB=0] [CT=0]	[T=3] [B=1] [R=1] [CB=0] [CT=1]	[T=3] [B=1] [R=1] [CB=0] [CT=2]	[T=3] [B=1] [R=1] [CB=1] [CT=0]	[T=3] [B=1] [R=1] [CB=1] [CT=1]	[T=3] [B=1] [R=1] [CB=1] [CT=2]	[T=3] [B=1] [R=1] [CB=1] [CT=3]	[T=3] [B=1] [R=1] [CB=1] [CT=4]	[T=3] [B=1] [R=1] [CB=1] [CT=5]	[T=3] [B=1] [R=1] [CB=2] [CT=0]	[T=3] [B=1] [R=1] [CB=2] [CT=1]	[T=3] [B=1] [R=1] [CB=2] [CT=2]	[T=3] [B=1] [R=1] [CB=2] [CT=3]	[T=3] [B=1] [R=1] [CB=2] [CT=4]	[T=3] [B=1] [R=1] [CB=2] [CT=5]
R184	ct_eob_br															
	[T=3] [B=1] [R=1] [CB=3] [CT=0]	[T=3] [B=1] [R=1] [CB=3]	[T=3] [B=1] [R=1] [CB=3]	[T=3] [B=1] [R=1] [CB=3]	[T=3] [B=1] [R=1] [CB=3]	[T=3] [B=1] [R=1] [CB=3]	[T=3] [B=1] [R=1] [CB=4]	[T=3] [B=1] [R=1] [CB=4]	[T=3] [B=1] [R=1] [CB=4]	[T=3] [B=1] [R=1] [CB=4]	[T=3] [B=1] [R=1] [CB=4]	[T=3] [B=1] [R=1] [CB=4]	[T=3] [B=1] [R=1] [CB=5]	[T=3] [B=1] [R=1] [CB=5]	[T=3] [B=1] [R=1] [CB=5]	[T=3] [B=1] [R=1] [CB=5] [CT=3]

Rxxx Value 1 row = 1 Cacheline	16 32-bit counters															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		[CT=1]	[CT=2]	[CT=3]	[CT=4]	[CT=5]	[CT=0]	[CT=1]	[CT=2]	[CT=3]	[CT=4]	[CT=5]	[CT=0]	[CT=1]	[CT=2]	
R185	ct_eob_br		ct_uv_mode													
	[T=3] [B=1] [R=1] [CB=5] [CT=4]	[T=3] [B=1] [R=1] [CB=5] [CT=5]	[0] [0]	[0] [1]	[0] [2]	[0] [3]	[0] [4]	[0] [5]	[0] [6]	[0] [7]	[0] [8]	[0] [9]	[1] [0]	[1] [1]	[1] [2]	[1] [3]
R186	ct_uv_mode															
	[1] [4]	[1] [5]	[1] [6]	[1] [7]	[1] [8]	[1] [9]	[2] [0]	[2] [1]	[2] [2]	[2] [3]	[2] [4]	[2] [5]	[2] [6]	[2] [7]	[2] [8]	[2] [9]
R187	ct_uv_mode															
	[3] [0]	[3] [1]	[3] [2]	[3] [3]	[3] [4]	[3] [5]	[3] [6]	[3] [7]	[3] [8]	[3] [9]	[4] [0]	[4] [1]	[4] [2]	[4] [3]	[4] [4]	[4] [5]
R188	ct_uv_mode															
	[4] [6]	[4] [7]	[4] [8]	[4] [9]	[5] [0]	[5] [1]	[5] [2]	[5] [3]	[5] [4]	[5] [5]	[5] [6]	[5] [7]	[5] [8]	[5] [9]	[6] [0]	[6] [1]
R189	ct_uv_mode															
	[6] [2]	[6] [3]	[6] [4]	[6] [5]	[6] [6]	[6] [7]	[6] [8]	[6] [9]	[7] [0]	[7] [1]	[7] [2]	[7] [3]	[7] [4]	[7] [5]	[7] [6]	[7] [7]
R190	ct_uv_mode															
	[7] [8]	[7] [9]	[8] [0]	[8] [1]	[8] [2]	[8] [3]	[8] [4]	[8] [5]	[8] [6]	[8] [7]	[8] [8]	[8] [9]	[9] [0]	[9] [1]	[9] [2]	[9] [3]
R191	ct_uv_mode						ct_seg_id								ct_seg_pred	
	[9]	[9]	[9]	[9]	[9]	[9]	[0]	[1]	[2]	[3]	[4]	[5]	[6]	[7]	[0]	[0]

Rxxx Value 1 row = 1 Cacheline	16 32-bit counters															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	[4]	[5]	[6]	[7]	[8]	[9]									[0]	[1]
R192	ct_seg_pred															
	[1] [0]	[1] [1]	[2] [0]	[2] [1]												

Probability Statistics Counters Context Legend

Counter	i	j	k	l	m	n	Dimension	Total Number of Counters
ct_tx_8x8 [i] [j]	Context	Node					2X2	4
ct_tx_16x16 [i] [j]	Context	Node					2X3	6
ct_tx_32x32 [i] [j]	Context	Node					2X4	8
ct_coef [T=i] [B=j] [R=k] [CB=l] [CT=m] [N=n]	T = TransformSize (0 4x4, 1 8x8, 2 16x16, 3 32x32)	B = BlockType (0 Y, 1 UV)	R = ReferenceType (0 Intra, 1 Inter)	CB = CoefficientBand	CT = Context	N = Node (0 ZERO, 1 ONE, 2 TWO, 3	4X2X2X6X6X4	2112

Counter	i	j	k	l	m	n	Dimension	Total Number of Counters
						EOB)		
ct_mbskip [i] [j]	Context	Node					3X2	6
ct_inter_mode [i] [j]	Context (BOTH_ZERO, ZERO_PLUS_PREDICTED, BOTH_PREDICTED, NEW_PLUS_NON_INTRA, BOTH_NEW, INTRA_PLUS_NON_INTRA, BOTH_INTRA)	Node (NEARESTMV, NEARMV, ZEROMV, NEWMV)					7X4	28
ct_switchable_interp [i] [j]	Context	Node (MV_JOINT_ZERO, MV_JOINT_HNZVZ, MV_JOINT_HZVNZ, MV_JOINT_HNZVNZ)					3X4	12
ct_intra_inter [i] [j]	Context	Node					4X2	8
ct_comp_inter [i] [j]	Context	Node					5X2	10
ct_single_ref [i] [j] [k]	P0,P1	Context	Node				2X5X2	20
ct_comp_ref	Context	Node					5X2	10

Counter	i	j	k	l	m	n	Dimension	Total Number of Counters
[i] [j]								
ct_y_mode [i] [j]	BLOCK_SIZE_GROUPS	Node (DC_PRED, TM_PRED, V_PRED, H_PRED, D135_PRED, D117_PRED, D45_PRED, D63_PRED, D153_PRED, D27_PRED)					4x10	40
ct_partition [i] [j]	Context	Node (00: NONE, 01: HORZ, 10: VERT, 11: SPLIT)					16X4	64
ct_mv_joints [i]	Node (MV_JOINT_ZERO, MV_JOINT_HNZVZ, MV_JOINT_HZVNZ, MV_JOINT_HNZVNZ)						4	4
ct_mv_sign [i] [j]	XY	Node					2X2	4
ct_mv_classes [i] [j]	XY	MV CLASS					2X10	20
ct_mv_class0 [i] [j]	XY	Node					2X2	4
ct_mv_bits	XY	MV BIT POSITION	Node				2X10X2	40

Counter	i	j	k	l	m	n	Dimension	Total Number of Counters
[i] [j] [k]								
ct_mv_class0_fp	XY	MV_CLASS0 BIT	Node				2X2X4	16
[i] [j] [k]								
ct_mv_fp	XY	Node					2X4	8
[i] [j]								
ct_mv_class0_hp	XY	Node					2X2	4
[i] [j]								
ct_mv_hp	XY	Node					2X2	4
[i] [j]								
ct_eob_br	T = TransformSize (0 4x4, 1 8x8, 2 16x16, 3 32x32)	B = BlockType (0 Y, 1 UV)	R = ReferenceType (0 Intra, 1 Inter)	CB = CoefficientBand	CT = Context		4X2X2X6X6	528
[T=i] [B=j] [R=k] [CB=l] [CT=m]								
ct_uv_mode	Context	Node(DC_PRED, TM_PRED, V_PRED, H_PRED, D135_PRED, D117_PRED, D45_PRED,					10x10	100
[i] [j]								

Counter	i	j	k	l	m	n	Dimension	Total Number of Counters
		D63_PRED, D153_PRED, D27_PRED)						
ct_seg_id[i] [i]	Node						8	8
ct_seg_pred [i] [j]	Context	Node					3X2	6
								3074

VP9 PAK Quant Lookup Tables

Qindex	IQ_Scale						FQ_Shift						FQ_Quant					
	8b		10b		12b		8b		10b		12b		8b		10b		12b	
	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC
0	4	4	4	4	4	4	1	1	1	1	1	1	32768	32768	32768	32768	32768	32768
1	8	8	9	9	12	13	2	2	2	2	2	2	32768	32768	29127	29127	21845	20164
2	8	9	10	11	18	19	2	2	2	2	3	3	32768	29127	26214	23831	29127	27594
3	9	10	13	13	25	27	2	2	2	2	3	3	29127	26214	20164	20164	20971	19418
4	10	11	15	16	33	35	2	2	2	3	4	4	26214	23831	17476	32768	31775	29959
5	11	12	17	18	41	44	2	2	3	3	4	4	23831	21845	30840	29127	25575	23831
6	12	13	20	21	50	54	2	2	3	3	4	4	21845	20164	26214	24966	20971	19418
7	12	14	22	24	60	64	2	2	3	3	4	5	21845	18724	23831	21845	17476	32768
8	13	15	25	27	70	75	2	2	3	3	5	5	20164	17476	20971	19418	29959	27962
9	14	16	28	30	80	87	2	3	3	3	5	5	18724	32768	18724	17476	26214	24105
10	15	17	31	33	91	99	2	3	3	4	5	5	17476	30840	16912	31775	23045	21183
11	16	18	34	37	103	112	3	3	4	4	5	5	32768	29127	30840	28339	20360	18724
12	17	19	37	40	115	126	3	3	4	4	5	5	30840	27594	28339	26214	18236	16644
13	18	20	40	44	127	139	3	3	4	4	5	6	29127	26214	26214	23831	16513	30174
14	19	21	43	48	140	154	3	3	4	4	6	6	27594	24966	24385	21845	29959	27235
15	19	22	47	51	153	168	3	3	4	4	6	6	27594	23831	22310	20560	27413	24966
16	20	23	50	55	166	183	3	3	4	4	6	6	26214	22795	20971	19065	25266	22919
17	21	24	53	59	180	199	3	3	4	4	6	6	24966	21845	19784	17772	23301	21076

Qindex	IQ_Scale						FQ_Shift						FQ_Quant					
	8b		10b		12b		8b		10b		12b		8b		10b		12b	
	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC
18	22	25	57	63	194	214	3	3	4	4	6	6	23831	20971	18396	16644	21620	19599
19	23	26	60	67	208	230	3	3	4	5	6	6	22795	20164	17476	31300	20164	18236
20	24	27	64	71	222	247	3	3	5	5	6	6	21845	19418	32768	29537	18893	16980
21	25	28	68	75	237	263	3	3	5	5	6	7	20971	18724	30840	27962	17697	31895
22	26	29	71	79	251	280	3	3	5	5	6	7	20164	18078	29537	26546	16710	29959
23	26	30	75	83	266	297	3	3	5	5	7	7	20164	17476	27962	25266	31536	28244
24	27	31	78	88	281	314	3	3	5	5	7	7	19418	16912	26886	23831	29852	26715
25	28	32	82	92	296	331	3	4	5	5	7	7	18724	32768	25575	22795	28339	25343
26	29	33	86	96	312	349	3	4	5	5	7	7	18078	31775	24385	21845	26886	24036
27	30	34	90	100	327	366	3	4	5	5	7	7	17476	30840	23301	20971	25653	22919
28	31	35	93	105	343	384	3	4	5	5	7	7	16912	29959	22550	19972	24456	21845
29	32	36	97	109	358	402	4	4	5	5	7	7	32768	29127	21620	19239	23431	20867
30	32	37	101	114	374	420	4	4	5	5	7	7	32768	28339	20763	18396	22429	19972
31	33	38	105	118	390	438	4	4	5	5	7	7	31775	27594	19972	17772	21509	19152
32	34	39	109	122	405	456	4	4	5	5	7	7	30840	26886	19239	17189	20712	18396
33	35	40	113	127	421	475	4	4	5	5	7	7	29959	26214	18558	16513	19925	17660
34	36	41	116	131	437	493	4	4	5	6	7	7	29127	25575	18078	32017	19195	17015
35	37	42	120	136	453	511	4	4	5	6	7	7	28339	24966	17476	30840	18517	16416
36	38	43	124	140	469	530	4	4	5	6	7	8	2759	2438	1691	2995	1788	3165

Qindex	IQ_Scale						FQ_Shift						FQ_Quant					
	8b		10b		12b		8b		10b		12b		8b		10b		12b	
	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC
													4	5	2	9	6	5
37	38	44	128	145	484	548	4	4	6	6	7	8	27594	23831	32768	28926	17331	30615
38	39	45	132	149	500	567	4	4	6	6	7	8	26886	23301	31775	28149	16777	29589
39	40	46	136	154	516	586	4	4	6	6	8	8	26214	22795	30840	27235	32513	28630
40	41	47	140	158	532	604	4	4	6	6	8	8	25575	22310	29959	26546	31536	27776
41	42	48	143	163	548	623	4	4	6	6	8	8	24966	21845	29330	25731	30615	26929
42	43	49	147	168	564	642	4	4	6	6	8	8	24385	21399	28532	24966	29746	26132
43	43	50	151	172	580	660	4	4	6	6	8	8	24385	20971	27776	24385	28926	25420
44	44	51	155	177	596	679	4	4	6	6	8	8	23831	20560	27060	23696	28149	24708
45	45	52	159	181	611	698	4	4	6	6	8	8	23301	20164	26379	23172	27458	24036
46	46	53	163	186	627	716	4	4	6	6	8	8	22795	19784	25731	22550	26757	23431
47	47	54	166	190	643	735	4	4	6	6	8	8	22310	19418	25266	22075	26092	22826
48	48	55	170	195	659	753	4	4	6	6	8	8	21845	19065	24672	21509	25458	22280
49	48	56	174	199	674	772	4	4	6	6	8	8	21845	18724	24105	21076	24892	21732
50	49	57	178	204	690	791	4	4	6	6	8	8	21399	18396	23563	20560	24314	21210
51	50	58	182	208	706	809	4	4	6	6	8	8	20971	18078	23045	20164	23763	20738
52	51	59	185	213	721	828	4	4	6	6	8	8	20560	17772	22671	19691	23269	20262
53	52	60	189	217	737	846	4	4	6	6	8	8	20164	17476	22192	19328	22764	19831
54	53	61	193	222	752	865	4	4	6	6	8	8	19784	17189	21732	18893	22310	19395

Qindex	IQ_Scale						FQ_Shift						FQ_Quant					
	8b		10b		12b		8b		10b		12b		8b		10b		12b	
	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC
55	53	62	197	226	768	884	4	4	6	6	8	8	19784	16912	21290	18558	21845	18978
56	54	63	200	231	783	902	4	4	6	6	8	8	19418	16644	20971	18157	21426	18600
57	55	64	204	235	798	920	4	5	6	6	8	8	19065	32768	20560	17848	21024	18236
58	56	65	208	240	814	939	4	5	6	6	8	8	18724	32263	20164	17476	20610	17867
59	57	66	212	244	829	957	4	5	6	6	8	8	18396	31775	19784	17189	20237	17531
60	57	67	215	249	844	976	4	5	6	6	8	8	18396	31300	19508	16844	19878	17189
61	58	68	219	253	859	994	4	5	6	6	8	8	18078	30840	19152	16578	19531	16878
62	59	69	223	258	874	1012	4	5	6	7	8	8	17772	30393	18808	32513	19195	16578
63	60	70	226	262	889	1030	4	5	6	7	8	9	17476	29959	18558	32017	18872	32577
64	61	71	230	267	904	1049	4	5	6	7	8	9	17189	29537	18236	31418	18558	31987
65	62	72	233	271	919	1067	4	5	6	7	8	9	16912	29127	18001	30954	18255	31447
66	62	73	237	275	934	1085	4	5	6	7	8	9	16912	28728	17697	30504	17962	30925
67	63	74	241	280	949	1103	4	5	6	7	8	9	16644	28339	17403	29959	17678	30421
68	64	75	244	284	964	1121	5	5	6	7	8	9	32768	27962	17189	29537	17403	29932
69	65	76	248	289	978	1139	5	5	6	7	8	9	32263	27594	16912	29026	17154	29459
70	66	77	251	293	993	1157	5	5	6	7	8	9	31775	27235	16710	28630	16895	29001
71	66	78	255	297	1008	1175	5	5	6	7	8	9	31775	26886	16448	28244	16644	28556
72	67	79	259	302	1022	1193	5	5	7	7	8	9	31300	26546	32388	27776	16416	28126
73	68	80	262	306	1037	1211	5	5	7	7	9	9	3084	2621	3201	2741	3235	2770

Qindex	IQ_Scale						FQ_Shift						FQ_Quant					
	8b		10b		12b		8b		10b		12b		8b		10b		12b	
	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC
													0	4	7	3	7	8
74	69	81	266	311	1051	1229	5	5	7	7	9	9	30393	25890	31536	26973	31926	27302
75	70	82	269	315	1065	1246	5	5	7	7	9	9	29959	25575	31184	26630	31506	26929
76	70	83	273	319	1080	1264	5	5	7	7	9	9	29959	25266	30727	26296	31068	26546
77	71	84	276	324	1094	1282	5	5	7	7	9	9	29537	24966	30393	25890	30671	26173
78	72	85	280	328	1108	1299	5	5	7	7	9	9	29127	24672	29959	25575	30283	25830
79	73	86	283	332	1122	1317	5	5	7	7	9	9	28728	24385	29641	25266	29905	25477
80	74	87	287	337	1136	1335	5	5	7	7	9	9	28339	24105	29228	24892	29537	25134
81	74	88	290	341	1151	1352	5	5	7	7	9	9	28339	23831	28926	24600	29152	24818
82	75	89	293	345	1165	1370	5	5	7	7	9	9	27962	23563	28630	24314	28802	24492
83	76	90	297	349	1179	1387	5	5	7	7	9	9	27594	23301	28244	24036	28460	24192
84	77	91	300	354	1192	1405	5	5	7	7	9	9	27235	23045	27962	23696	28149	23882
85	78	92	304	358	1206	1422	5	5	7	7	9	9	26886	22795	27594	23431	27822	23596
86	78	93	307	362	1220	1440	5	5	7	7	9	9	26886	22550	27324	23172	27503	23301
87	79	94	310	367	1234	1457	5	5	7	7	9	9	26546	22310	27060	22857	27191	23029
88	80	95	314	371	1248	1474	5	5	7	7	9	9	26214	22075	26715	22610	26886	22764
89	81	96	317	375	1261	1491	5	5	7	7	9	9	25890	21845	26462	22369	26609	22504
90	81	97	321	379	1275	1509	5	5	7	7	9	9	25890	21620	26132	22133	26317	22236
91	82	98	324	384	1288	1526	5	5	7	7	9	9	25575	21399	25890	21845	26051	21988

Qindex	IQ_Scale						FQ_Shift						FQ_Quant					
	8b		10b		12b		8b		10b		12b		8b		10b		12b	
	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC
92	83	99	327	388	1302	1543	5	5	7	7	9	9	25266	21183	25653	21620	25771	21746
93	84	100	331	392	1315	1560	5	5	7	7	9	9	24966	20971	25343	21399	25516	21509
94	85	101	334	396	1329	1577	5	5	7	7	9	9	24672	20763	25115	21183	25247	21277
95	85	102	337	401	1342	1595	5	5	7	7	9	9	24672	20560	24892	20919	25003	21037
96	87	104	343	409	1368	1627	5	5	7	7	9	9	24105	20164	24456	20510	24528	20623
97	88	106	350	417	1393	1660	5	5	7	7	9	9	23831	19784	23967	20116	24087	20213
98	90	108	356	425	1419	1693	5	5	7	7	9	9	23301	19418	23563	19737	23646	19819
99	92	110	362	433	1444	1725	5	5	7	7	9	9	22795	19065	23172	19373	23237	19451
100	93	112	369	441	1469	1758	5	5	7	7	9	9	22550	18724	22733	19021	22841	19086
101	95	114	375	449	1494	1791	5	5	7	7	9	9	22075	18396	22369	18682	22459	18735
102	96	116	381	458	1519	1824	5	5	7	7	9	9	21845	18078	22017	18315	22089	18396
103	98	118	387	466	1544	1856	5	5	7	7	9	9	21399	17772	21675	18001	21732	18078
104	99	120	394	474	1569	1889	5	5	7	7	9	9	21183	17476	21290	17697	21385	17763
105	101	122	400	482	1594	1922	5	5	7	7	9	9	20763	17189	20971	17403	21050	17458
106	102	124	406	490	1618	1954	5	5	7	7	9	9	20560	16912	20661	17119	20738	17172
107	104	126	412	498	1643	1987	5	5	7	7	9	9	20164	16644	20360	16844	20422	16886
108	105	128	418	506	1668	2020	5	6	7	7	9	9	19972	32768	20068	16578	20116	16611
109	107	130	424	514	1692	2052	5	6	7	8	9	10	19599	32263	19784	32640	19831	32704
110	108	132	430	523	1717	2085	5	6	7	8	9	10	1941	3177	1950	3207	1954	3218

Qindex	IQ_Scale						FQ_Shift						FQ_Quant					
	8b		10b		12b		8b		10b		12b		8b		10b		12b	
	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC
													8	5	8	8	2	6
111	110	134	436	531	1741	2118	5	6	7	8	9	10	19065	31300	19239	31595	19273	31685
112	111	136	442	539	1765	2150	5	6	7	8	9	10	18893	30840	18978	31126	19011	31213
113	113	138	448	547	1789	2183	5	6	7	8	9	10	18558	30393	18724	30671	18755	30741
114	114	140	454	555	1814	2216	5	6	7	8	9	10	18396	29959	18477	30229	18497	30283
115	116	142	460	563	1838	2248	5	6	7	8	9	10	18078	29537	18236	29799	18255	29852
116	117	144	466	571	1862	2281	5	6	7	8	9	10	17924	29127	18001	29382	18020	29420
117	118	146	472	579	1885	2313	5	6	7	8	9	10	17772	28728	17772	28976	17800	29013
118	120	148	478	588	1909	2346	5	6	7	8	9	10	17476	28339	17549	28532	17576	28605
119	121	150	484	596	1933	2378	5	6	7	8	9	10	17331	27962	17331	28149	17358	28220
120	123	152	490	604	1957	2411	5	6	7	8	9	10	17050	27594	17119	27776	17145	27834
121	125	155	499	616	1992	2459	5	6	7	8	9	10	16777	27060	16810	27235	16844	27291
122	127	158	507	628	2027	2508	5	6	7	8	9	10	16513	26546	16545	26715	16553	26757
123	129	161	516	640	2061	2556	6	6	8	8	10	10	32513	26051	32513	26214	32561	26255
124	131	164	525	652	2096	2605	6	6	8	8	10	10	32017	25575	31956	25731	32017	25761
125	134	167	533	664	2130	2653	6	6	8	8	10	10	31300	25115	31476	25266	31506	25295
126	136	170	542	676	2165	2701	6	6	8	8	10	10	30840	24672	30954	24818	30997	24845
127	138	173	550	688	2199	2750	6	6	8	8	10	10	30393	24244	30504	24385	30517	24403
128	140	176	559	700	2233	2798	6	6	8	8	10	10	29959	23831	30012	23967	30053	23984

Qindex	IQ_Scale						FQ_Shift						FQ_Quant					
	8b		10b		12b		8b		10b		12b		8b		10b		12b	
	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC
129	142	179	567	713	2267	2847	6	6	8	8	10	10	29537	23431	29589	23530	29602	23571
130	144	182	576	725	2300	2895	6	6	8	8	10	10	29127	23045	29127	23140	29177	23180
131	146	185	584	737	2334	2943	6	6	8	8	10	10	28728	22671	28728	22764	28752	22802
132	148	188	592	749	2367	2992	6	6	8	8	10	10	28339	22310	28339	22399	28351	22429
133	150	191	601	761	2400	3040	6	6	8	8	10	10	27962	21959	27915	22046	27962	22075
134	152	194	609	773	2434	3088	6	6	8	8	10	10	27594	21620	27548	21704	27571	21732
135	154	197	617	785	2467	3137	6	6	8	8	10	10	27235	21290	27191	21372	27202	21392
136	156	200	625	797	2499	3185	6	6	8	8	10	10	26886	20971	26843	21050	26854	21070
137	158	203	634	809	2532	3234	6	6	8	8	10	10	26546	20661	26462	20738	26504	20751
138	161	207	644	825	2575	3298	6	6	8	8	10	10	26051	20262	26051	20336	26061	20348
139	164	211	655	841	2618	3362	6	6	8	8	10	10	25575	19878	25614	19949	25633	19960
140	166	215	666	857	2661	3426	6	6	8	8	10	10	25266	19508	25191	19576	25219	19588
141	169	219	676	873	2704	3491	6	6	8	8	10	10	24818	19152	24818	19217	24818	19223
142	172	223	687	889	2746	3555	6	6	8	8	10	10	24385	18808	24420	18872	24438	18877
143	174	227	698	905	2788	3619	6	6	8	8	10	10	24105	18477	24036	18538	24070	18543
144	177	231	708	922	2830	3684	6	6	8	8	10	10	23696	18157	23696	18196	23713	18216
145	180	235	718	938	2872	3748	6	6	8	8	10	10	23301	17848	23366	17886	23366	17905
146	182	239	729	954	2913	3812	6	6	8	8	10	10	23045	17549	23014	17586	23037	17604
147	185	243	739	970	2954	3876	6	6	8	8	10	10	2267	1726	2270	1729	2271	1731

Qindex	IQ_Scale						FQ_Shift						FQ_Quant					
	8b		10b		12b		8b		10b		12b		8b		10b		12b	
	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC
													1	0	2	6	7	3
148	187	247	749	986	2995	3941	6	6	8	8	10	10	22429	16980	22399	17015	22406	17028
149	190	251	759	1002	3036	4005	6	6	8	8	10	10	22075	16710	22104	16743	22104	16756
150	192	255	770	1018	3076	4069	6	6	8	8	10	10	21845	16448	21788	16480	21816	16492
151	195	260	782	1038	3127	4149	6	7	8	9	10	11	21509	32263	21454	32326	21461	32349
152	199	265	795	1058	3177	4230	6	7	8	9	10	11	21076	31655	21103	31714	21123	31729
153	202	270	807	1078	3226	4310	6	7	8	9	10	11	20763	31068	20789	31126	20802	31141
154	205	275	819	1098	3275	4390	6	7	8	9	10	11	20460	30504	20485	30559	20491	30573
155	208	280	831	1118	3324	4470	6	7	8	9	10	11	20164	29959	20189	30012	20189	30026
156	211	285	844	1138	3373	4550	6	7	8	9	10	11	19878	29433	19878	29485	19895	29498
157	214	290	856	1158	3421	4631	6	7	8	9	10	11	19599	28926	19599	28976	19616	28982
158	217	295	868	1178	3469	4711	6	7	8	9	10	11	19328	28435	19328	28484	19345	28490
159	220	300	880	1198	3517	4791	6	7	8	9	10	11	19065	27962	19065	28008	19081	28014
160	223	305	891	1218	3565	4871	6	7	8	9	10	11	18808	27503	18829	27548	18824	27554
161	226	311	906	1242	3621	4967	6	7	8	9	10	11	18558	26973	18517	27016	18533	27021
162	230	317	920	1266	3677	5064	6	7	8	9	10	11	18236	26462	18236	26504	18250	26504
163	233	323	933	1290	3733	5160	6	7	8	9	10	11	18001	25970	17982	26011	17977	26011
164	237	329	947	1314	3788	5256	6	7	8	9	10	11	17697	25497	17716	25536	17716	25536
165	240	335	961	1338	3843	5352	6	7	8	9	10	11	17476	25040	17458	25078	17462	25078

Qindex	IQ_Scale						FQ_Shift						FQ_Quant					
	8b		10b		12b		8b		10b		12b		8b		10b		12b	
	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC
166	243	341	975	1362	3897	5448	6	7	8	9	10	11	17260	24600	17207	24636	17220	24636
167	247	347	988	1386	3951	5544	6	7	8	9	10	11	16980	24174	16980	24209	16985	24209
168	250	353	1001	1411	4005	5641	6	7	8	9	10	11	16777	23763	16760	23780	16756	23793
169	253	359	1015	1435	4058	5737	6	7	8	9	10	11	16578	23366	16529	23382	16537	23395
170	257	366	1030	1463	4119	5849	7	7	9	9	11	11	32640	22919	32577	22935	32585	22947
171	261	373	1045	1491	4181	5961	7	7	9	9	11	11	32140	22489	32109	22504	32101	22515
172	265	380	1061	1519	4241	6073	7	7	9	9	11	11	31655	22075	31625	22089	31647	22100
173	269	387	1076	1547	4301	6185	7	7	9	9	11	11	31184	21675	31184	21690	31206	21700
174	272	394	1090	1575	4361	6297	7	7	9	9	11	11	30840	21290	30783	21304	30776	21314
175	276	401	1105	1603	4420	6410	7	7	9	9	11	11	30393	20919	30366	20932	30366	20938
176	280	408	1120	1631	4479	6522	7	7	9	9	11	11	29959	20560	29959	20572	29966	20579
177	284	416	1137	1663	4546	6650	7	7	9	9	11	11	29537	20164	29511	20177	29524	20183
178	288	424	1153	1695	4612	6778	7	7	9	9	11	11	29127	19784	29101	19796	29101	19801
179	292	432	1170	1727	4677	6906	7	7	9	9	11	11	28728	19418	28679	19429	28697	19434
180	296	440	1186	1759	4742	7034	7	7	9	9	11	11	28339	19065	28292	19075	28304	19081
181	300	448	1202	1791	4807	7162	7	7	9	9	11	11	27962	18724	27915	18735	27921	18740
182	304	456	1218	1823	4871	7290	7	7	9	9	11	11	27594	18396	27548	18406	27554	18411
183	309	465	1236	1859	4942	7435	7	7	9	9	11	11	27147	18040	27147	18049	27158	18052
184	313	474	125	189	5013	7579	7	7	9	9	11	11	2680	1769	2677	1770	2677	1770

Qindex	IQ_Scale						FQ_Shift						FQ_Quant					
	8b		10b		12b		8b		10b		12b		8b		10b		12b	
	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC
			3	5									0	7	9	6	3	9
185	317	483	1271	1931	5083	7723	7	7	9	9	11	11	26462	17367	26400	17376	26405	17378
186	322	492	1288	1967	5153	7867	7	7	9	9	11	11	26051	17050	26051	17058	26046	17060
187	326	501	1306	2003	5222	8011	7	7	9	9	11	11	25731	16743	25692	16752	25702	16754
188	330	510	1323	2039	5291	8155	7	7	9	9	11	11	25420	16448	25362	16456	25367	16458
189	335	520	1342	2079	5367	8315	7	8	9	10	11	12	25040	32263	25003	32279	25007	32283
190	340	530	1361	2119	5442	8475	7	8	9	10	11	12	24672	31655	24654	31670	24663	31673
191	344	540	1379	2159	5517	8635	7	8	9	10	11	12	24385	31068	24332	31083	24328	31086
192	349	550	1398	2199	5591	8795	7	8	9	10	11	12	24036	30504	24001	30517	24006	30521
193	354	560	1416	2239	5665	8956	7	8	9	10	11	12	23696	29959	23696	29972	23692	29972
194	359	571	1436	2283	5745	9132	7	8	9	10	11	12	23366	29382	23366	29395	23362	29395
195	364	582	1456	2327	5825	9308	7	8	9	10	11	12	23045	28826	23045	28839	23041	28839
196	369	593	1476	2371	5905	9484	7	8	9	10	11	12	22733	28292	22733	28304	22729	28304
197	374	604	1496	2415	5984	9660	7	8	9	10	11	12	22429	27776	22429	27788	22429	27788
198	379	615	1516	2459	6063	9836	7	8	9	10	11	12	22133	27280	22133	27291	22137	27291
199	384	627	1537	2507	6149	10028	7	8	9	10	11	12	21845	26757	21831	26768	21827	26768
200	389	639	1559	2555	6234	10220	7	8	9	10	11	12	21564	26255	21523	26265	21529	26265
201	395	651	1580	2603	6319	10412	7	8	9	10	11	12	21236	25771	21236	25781	21240	25781
202	400	663	1601	2651	6404	10604	7	8	9	10	11	12	20971	25305	20958	25314	20958	25314

Qindex	IQ_Scale						FQ_Shift						FQ_Quant					
	8b		10b		12b		8b		10b		12b		8b		10b		12b	
	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC
203	406	676	1624	2703	6495	10812	7	8	9	10	11	12	20661	24818	20661	24827	20664	24827
204	411	689	1647	2755	6587	11020	7	8	9	10	11	12	20410	24350	20373	24358	20376	24358
205	417	702	1670	2807	6678	11228	7	8	9	10	11	12	20116	23899	20092	23907	20098	23907
206	423	715	1692	2859	6769	11437	7	8	9	10	11	12	19831	23464	19831	23472	19828	23470
207	429	729	1717	2915	6867	11661	7	8	9	10	11	12	19553	23014	19542	23021	19545	23019
208	435	743	1741	2971	6966	11885	7	8	9	10	11	12	19284	22580	19273	22587	19267	22586
209	441	757	1766	3027	7064	12109	7	8	9	10	11	12	19021	22162	19000	22170	19000	22168
210	447	771	1791	3083	7163	12333	7	8	9	10	11	12	18766	21760	18735	21767	18737	21765
211	454	786	1817	3143	7269	12573	7	8	9	10	11	12	18477	21345	18466	21351	18464	21350
212	461	801	1844	3203	7376	12813	7	8	9	10	11	12	18196	20945	18196	20951	18196	20950
213	467	816	1871	3263	7483	13053	7	8	9	10	11	12	17962	20560	17933	20566	17936	20565
214	475	832	1900	3327	7599	13309	7	8	9	10	11	12	17660	20164	17660	20170	17662	20169
215	482	848	1929	3391	7715	13565	7	8	9	10	11	12	17403	19784	17394	19790	17396	19788
216	489	864	1958	3455	7832	13821	7	8	9	10	11	12	17154	19418	17137	19423	17137	19422
217	497	881	1990	3523	7958	14093	7	8	9	10	11	12	16878	19043	16861	19048	16865	19047
218	505	898	2021	3591	8085	14365	7	8	9	10	11	12	16611	18682	16602	18688	16600	18686
219	513	915	2054	3659	8214	14637	8	8	10	10	12	12	32704	18335	32672	18340	32680	18339
220	522	933	2088	3731	8352	14925	8	8	10	10	12	12	32140	17982	32140	17986	32140	17985
221	530	951	212	380	8492	1521	8	8	10	10	12	12	3165	1764	3161	1764	3161	1764

Qindex	IQ_Scale						FQ_Shift						FQ_Quant					
	8b		10b		12b		8b		10b		12b		8b		10b		12b	
	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC
			3	3		3							5	1	0	6	0	5
222	539	969	2159	3876	8635	15502	8	8	10	10	12	12	31126	17313	31083	17313	31086	17316
223	549	988	2197	3952	8788	15806	8	8	10	10	12	12	30559	16980	30545	16980	30545	16983
224	559	1007	2236	4028	8945	16110	8	8	10	10	12	12	30012	16660	30012	16660	30009	16662
225	569	1026	2276	4104	9104	16414	8	9	10	11	12	13	29485	32704	29485	32704	29485	32708
226	579	1046	2319	4184	9275	16734	8	9	10	11	12	13	28976	32078	28938	32078	28941	32082
227	590	1066	2363	4264	9450	17054	8	9	10	11	12	13	28435	31476	28399	31476	28405	31480
228	602	1087	2410	4348	9639	17390	8	9	10	11	12	13	27869	30868	27846	30868	27848	30872
229	614	1108	2458	4432	9832	17726	8	9	10	11	12	13	27324	30283	27302	30283	27302	30287
230	626	1129	2508	4516	10031	18062	8	9	10	11	12	13	26800	29720	26757	29720	26760	29723
231	640	1151	2561	4604	10245	18414	8	9	10	11	12	13	26214	29152	26204	29152	26201	29155
232	654	1173	2616	4692	10465	18766	8	9	10	11	12	13	25653	28605	25653	28605	25650	28608
233	668	1196	2675	4784	10702	19134	8	9	10	11	12	13	25115	28055	25087	28055	25082	28058
234	684	1219	2737	4876	10946	19502	8	9	10	11	12	13	24528	27526	24519	27526	24523	27529
235	700	1243	2802	4972	11210	19886	8	9	10	11	12	13	23967	26994	23950	26994	23946	26997
236	717	1267	2871	5068	11482	20270	8	9	10	11	12	13	23399	26483	23374	26483	23378	26485
237	736	1292	2944	5168	11776	20670	8	9	10	11	12	13	22795	25970	22795	25970	22795	25973
238	755	1317	3020	5268	12081	21070	8	9	10	11	12	13	22221	25477	22221	25477	22219	25480
239	775	1343	3102	5372	12409	21486	8	9	10	11	12	13	21648	24984	21634	24984	21632	24987

Qindex	IQ_Scale						FQ_Shift						FQ_Quant					
	8b		10b		12b		8b		10b		12b		8b		10b		12b	
	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC	DC	AC
240	796	1369	3188	5476	12750	21902	8	9	10	11	12	13	21076	24510	21050	24510	21053	24512
241	819	1396	3280	5584	13118	22334	8	9	10	11	12	13	20485	24036	20460	24036	20463	24038
242	843	1423	3375	5692	13501	22766	8	9	10	11	12	13	19901	23580	19884	23580	19882	23582
243	869	1451	3478	5804	13913	23214	8	9	10	11	12	13	19306	23125	19295	23125	19293	23127
244	896	1479	3586	5916	14343	23662	8	9	10	11	12	13	18724	22687	18714	22687	18715	22689
245	925	1508	3702	6032	14807	24126	8	9	10	11	12	13	18137	22250	18127	22250	18128	22252
246	955	1537	3823	6148	15290	24590	8	9	10	11	12	13	17567	21831	17553	21831	17556	21832
247	988	1567	3953	6268	15812	25070	8	9	10	11	12	13	16980	21413	16976	21413	16976	21414
248	1022	1597	4089	6388	16356	25551	8	9	10	11	12	13	16416	21010	16412	21010	16412	21011
249	1058	1628	4236	6512	16943	26047	9	9	11	11	13	13	31714	20610	31685	20610	31686	20611
250	1098	1660	4394	6640	17575	26559	9	9	11	11	13	13	30559	20213	30545	20213	30547	20214
251	1139	1692	4559	6768	18237	27071	9	9	11	11	13	13	29459	19831	29440	19831	29438	19831
252	1184	1725	4737	6900	18949	27599	9	9	11	11	13	13	28339	19451	28333	19451	28332	19452
253	1232	1759	4929	7036	19718	28143	9	9	11	11	13	13	27235	19075	27230	19075	27227	19076
254	1282	1793	5130	7172	20521	28687	9	9	11	11	13	13	26173	18714	26163	18714	26162	18714
255	1336	1828	5347	7312	21387	29247	9	9	11	11	13	13	25115	18355	25101	18355	25102	18356

SB, CU/PU and TU Sizes – Encoder Only

CU/PU/TU Partitioning Configurations

SB size	CU size	min/max TU range
64x64	64x64	32x32..4x4
	32x32	32x32..4x4
	16x16	16x16..4x4
	8x8	8x8..4x4

PU Options for a Given CU

Current CU size	Possible CU sizes	Allowed CU/PU partition types.
64x64	64x64	2Nx2N, 2NxN, Nx2N
	32x32	2Nx2N, 2NxN, Nx2N
	16x16	2Nx2N, 2NxN, Nx2N
	8x8	2Nx2N, 2NxN, Nx2N, NxN

Definition of the VP9 CU Record Structure - Encoder Only

The following table defines the CU record structure as indirect data to the PAK Object Command. Entries are DW based (4 bytes) and cache aligned. This memory surface is pointed to by the HCP Indirect CU Object Base Address in the HCP_IND_OBJ_BASE_ADDR_STATE Command.

VP9 CU Record Structure Definition (UnPacked CU)

DW	Bit	Field	Bits	Definition	Comments
0	1:0	cu_size	2	0: 8x8, 1:16x16, 2: 32x32, and 3: 64x64	Indicates size of the CU
	3:2	Reserved	4	MBZ	
	5:4	cu_part_mode	2	0: 2Nx2N, 1: 2NxN, 2: Nx2N, 3: NxN (8x8 only)	
	7:6	Reserved	2	MBZ	
	11:8	intra_chroma_mode[0][3:0]	4	0:DC_PRED 1:V_PRED 2:H_PRED 3:TM_PRED 4:D45_PRED 5:D135_PRED 6:D117_PRED 7:D153_PRED 8:D207_PRED 9:D63_PRED 10-15 Reserved	
	15:12	Reserved	4	MBZ	
	19:16	intra_chroma_mode[1][3:0]	4	0:DC_PRED 1:V_PRED 2:H_PRED 3:TM_PRED 4:D45_PRED	Applicable for part1 of shapes > 8x8

DW	Bit	Field	Bits	Definition	Comments
				5:D135_PRED 6:D117_PRED 7:D153_PRED 8:D207_PRED 9:D63_PRED 10-15 Reserved	
	20	cu_pred_mode0	1	0: Intra 1: Inter	Pred mode for part0 in raster scan order cu_pred_mode=intra means ref_reframe0=intra
	21	cu_pred_mode1	1	0: Intra 1: Inter	Pred mode for part1 in raster scan order cu_pred_mode=intra means ref_reframe0=intra
	23:22	Reserved	2	MBZ	
	24	interpred_comp0	1	0: Single 1: Compound(ref_reframe1>intra)	Interpred comp mode for Part0
	25	interpred_comp1	0	0: Single 1: Compound(ref_reframe1>intra)	Interpred comp mode for Part1
	31:26	Reserved	6	MBZ	
1	3:0	intra_mode[0][3:0]	4	0:DC_PRED 1:V_PRED 2:H_PRED 3:TM_PRED 4:D45_PRED 5:D135_PRED 6:D117_PRED 7:D153_PRED 8:D207_PRED 9:D63_PRED	Luma Intra mode for part0
	7:4	Reserved	4		
	11:8	intra_mode[1][3:0]	4		Luma pred mode for part1
	15:12	Reserved	4		
	19:16	intra_mode[2][3:0]	4		Luma pred mode for part2;

DW	Bit	Field	Bits	Definition	Comments
					applicable for 4x4 only
	23:19	Reserved	4		
	27:24	intra_mode[3][3:0]	4		Luma pred mode for part3; applicable for 4x4 only
	31:28	Reserved	4		
2	15:0	mvx_reframe0[0][15:0]	16		Frame0(Forward) MVx for part0 16-bit each(2's complement with 3 fractional bits); encodable range is [-16382,16382]).
	31:16	mvy_reframe0[0][15:0]	16		Frame0(Forward) MVy for part0 16-bit each(2's complement with 3 fractional bits); encodable range is [-16382,16382]).
3	15:0	mvx_reframe0[1][15:0]	16		Frame0 (Forward) MVx for part1 16-bit each(2's complement with 3 fractional bits); encodable range is [-16382,16382]).
	31:16	mvy_reframe0[1][15:0]	16		Frame0 (Forward) MVy for part1 16-bit each(2's complement with 3 fractional bits); encodable range is [-16382,16382]).
4	15:0	mvx_reframe0[2][15:0]	16		
	31:16	mvy_reframe0[2][15:0]	16		
5	15:0	mvx_reframe0[3][15:0]	16		
	31:16	mvy_reframe0[3][15:0]	16		
6	15:0	mvx_reframe1[0][15:0]	16		
	31:16	mvy_reframe1[0][15:0]	16		
7	15:0	mvx_reframe1[1][15:0]	16		
	31:16	mvy_reframe1[1][15:0]	16		
8	15:0	mvx_reframe1[2][15:0]	16		Interleaved X and Y
	31:16	mvy_reframe1[2][15:0]	16		
9	15:0	mvx_reframe1[3][15:0]	16		
	31:16	mvy_reframe1[3][15:0]	16		
10	1:0	ref_reframe0[0][1:0]	2	0:intra	frame0(forward)reference frame

DW	Bit	Field	Bits	Definition	Comments
				1:last 2:golden 3:altref	id for part0 HW uses if SegmentReferenceEnabled=0 in segment ID command
	3:2	Reserved	2	MBZ	
	5:4	ref_reframe0[1][1:0]	2	0:intra 1:last 2:golden 3:altref	frame0(forward)reference frame id for part1
	7:6	Reserved	2	MBZ	
	9:8	ref_reframe1 [0][1:0]	2	0:intra 1:last 2:golden 3:altref	frame1(backward)reference frame id for part0
	11:10	Reserved	2	MBZ	
	13:12	ref_reframe1 [1][1:0]	2	0:intra 1:last 2:golden 3:altref	frame0(forward)reference frame id for part1
	15:14	Reserved	2	MBZ	
	18:16	QuantRound0	3	0:+1/16 1:+2/16 2:+3/16 3:+4/16 4:+5/16 5:+6/16(default) 6:+7/16 7:+8/16	Quantization Round value for Part0 (8x8 and below shapes will have the same round value)
	19	Reserved		MBZ	
	22:20	QuantRound1	3	0:+1/16	Quantization Round value for Part1

DW	Bit	Field	Bits	Definition	Comments
				1:+2/16 2:+3/16 3:+4/16 4:+5/16 5:+6/16(default) 6:+7/16 7:+8/16	
	31:23	Reserved	1	MBZ	
11	1:0	tu_size[0][1:0]	2	0: 4x4 1: 8x8 2: 16x16 3: 32x32	tu_size[2][1:0], tu_size[3][1:0] must be 0 (4x4)
11	3:2	tu_size[1][1:0]	2	0: 4x4 1: 8x8 2: 16x16 3: 32x32	
11	13:4	Reserved	10	MBZ	
11	14	segmentPredFlag0	1	0:Diaable 1:Enable	Segment Prediction disable for Part0
11	15	segmentPredFlag1	1	0:Diaable 1:Enable	Segment Prediction disable for Part1
11	18:16	SegmentIdx[0][2:0]	3	Segment 0 to 7	SegmentID for part0 of blocks > 8x8
11	21:19	SegmentIdx[1][2:0]	3	Segment 0 to 7	SegmentID for part1 of blocks > 8x8
11	23:22	MotionComp_flttype[0][1:0]	2	0: EIGHTTAP 1: EIGHTTAP_SMOOTH 2: EIGHTTAP_SHARP 3: BILINEAR	HW will use this filtertype if SWITCHABLE=1 in pic state; Used for part0
11	25:24	MotionComp_flttype[1][1:0]	2	0: EIGHTTAP	For part1 of blocks >8x8

DW	Bit	Field	Bits	Definition	Comments
				1: EIGHTTAP_SMOOTH 2: EIGHTTAP_SHARP 3: BILINEAR	
11	31:26	Reserved	6	MBZ	
12..15	31:0	Reserved		MBZ	

Allowed SB Size Encoder Only

The following table details the SB size allowed and the number of records per SB for the encoder.

Allowed SB Size – Encoder Only

SB Size Allowed	Number of Records per SB
64x64	64

Note: HW will support partial SBs within a frame bourndary to a minimun CU8x8 granularity

HCP Commands

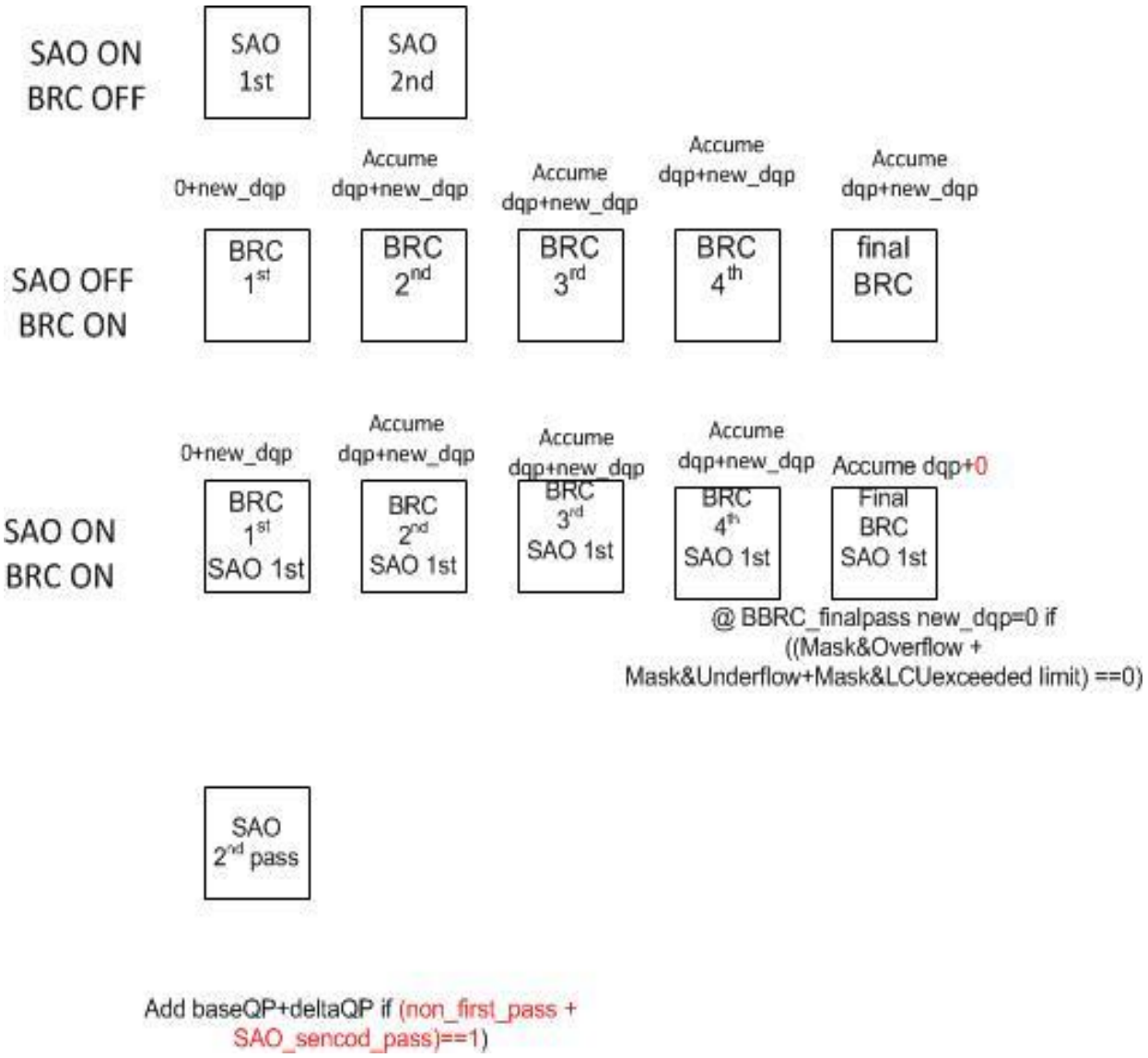
The HCP Commands specify the HEVC BSD object and PAK object level configuration.

HCP_BSD_OBJECT (VideoCS)

HCP_PAK_OBJECT_VideoCS

HCP_PAK_INSERT_OBJECT_VideoCS

Multipass flow during BRC and SAO



CU and Slice level stat streamOut

Along with final bitstream, HLC writes out two statistics related streamout cachelines to the memory. Streamout0 cacheline is composed of 4 quarter cachelines, each containing information on CU skip flag, coding block flag for the TUs in a CU, residual/coefficient bit count for a CU, total bit count for CU, LCU exceed limit flag. A typical streamout0 cacheline, therefore, has information on statistics for 4 CUs and lcu exceed limit flag.

Streamout1 cacheline is composed of quarter cachelines., each quarter cacheline consisting of bit count of current slice.

Pak pipeline streamout enable bit, set by HCP_PIPE_MODE_SELECT command, enables or disables the streamout.

Streamout 0: Per CU Quarter Cacheline Format

Level	Field	Width	Cacheline	Comment
CU	CU Skip Flag	1	qcacheline[0]	Packed in Quarter Cacheline in CU format
LCU	LCU exceed limit	1	qcacheline[1]	Packed in Quarter Cacheline in CU format (valid in last CU of LCU)
	Reserved	14	qcacheline[15:2	Reserved
CU	TU CBF Y/U/V	48	qcacheline[63:16]	Packed in Quarter Cacheline in CU format
CU	CU Coefficient Bit Count (Only residual)	18	qcacheline[81:64]	Packed in Quarter Cacheline in CU format
CU	CU Bit Count (all CU Syntax)	18	qcacheline[113:96]	Packed in Quarter Cacheline in CU format
	Reserved	14	qcacheline[127:114]	Reserved

Streamout 1: Per Slice Quarter Cacheline

Level	Field	Width	Cacheline	Comment
Slice	Slice Bit Count (slice header + data + tail)	32	cacheline[31:0]	
	Reserved	32	cacheline[63:32]	
	SlicePositionX[15:0]	16	cacheline[79:64]	
	SlicePositionY[15:0]	16	cacheline[95:80]	
	Reserved	32	cacheline[127:96]	

Definition of the CU Record Structure for Ext Interface – Encoder Only

The following table defines the CU record structure as indirect data to the PAK Object Command. Entries are DW based (4 bytes) and cache aligned. This memory surface is pointed to by the HCP Indirect CU Object Base Address in the HCP_IND_OBJ_BASE_ADDR_STATE Command.

CU Record Structure Definition

DWord	Bitfield	Field	Bits	Definition	Comments
0	1:0	cu_size	2	0: 8x8	
				1: 16x16	
				2: 32x32	
				3: 64x64	
	2	cu_pred_mode	1	0: Intra	For I slices, pred_mode is always 0.
				1: Inter	
	3	cu_transquant_bypass_flag	1		Note: HW ignores this bit for RhoDomain calculation so the statics will be slightly inaccurate. This bit should not be set to 1 if transform_skip=1
	6:4	cu_part_mode	3	0: 2Nx2N	
				1: 2NxN (inter only)	
				2: Nx2N (inter only)	
				3: NxN (intra only)	only if CU size is 8x8
				4: 2NxhN (inter only)	
				5: hNx2N (inter only)	
	7	IPCM_enable	1	1: Enable IPCM 0: Disable IPCM	MBZ Reserved If IPCM is enabled, then entire CU is IPCM predicted. Both PU and TU sizes should be same as CU size. Cu_pred_mode is ignored when IPCM is enbled. Note: Supports 8bit pixel depth only
	10:8	intra_chroma_mode	3	0: DM	(use Luma mode, from block 0 if NxN)
				1: Reserved	(supposedly to be defined for LM mode)

DWord	Bitfield	Field	Bits	Definition	Comments
				2: Planar	
				3: Vertical	
				4: Horizontal	
				5: DC	
	11	zero_out_coefficient	1	0: Do not force coefficients to zero 1: Force coefficients to zero	If this bit it set to 1, HW will force coefficients to zero.
	15:12	Reserved	5		
	22:16	cu_qp	7	in 7-bit	Valid range: 0 to 51 for 8bit mode -12 to 51 for 10bit mode *diff_cu_qp_delta_depth = 0 (No QP change allowed at CU Level.* Only allow QP change across LCU, no change across CU for PAK only.
	23	cu_qp_sign	1	0:positive 1:negative	Indicates sign bit for QP. Must be zero for 8bit mode
	31:24	interpred_idc[3:0][1:0]	8	2 bits each 0: L0 1: L1 2: Bi 3: reserved	in Z-order interpred_idc[0][1:0] - block 0 = [25:24] interpred_idc[15][1:0] - block 15 = [31:30]
1	5:0	intra_mode[0][5:0]	6	final explicit luma mode. Valid values are 0..34.	1 per cu partition, and only active partitions have valid intra mode value
	7:6	Reserved	2		
	13:8	intra_mode[1][5:0]	6	final explicit luma mode. Valid values are 0..34.	
	15:14	Reserved	2		
	21:16	intra_mode[2][5:0]	6	final explicit luma mode. Valid values are 0..34.	
	23:22	Reserved	2		
	29:24	intra_mode[3][5:0]	6	final explicit luma mode. Valid values are	

DWord	Bitfield	Field	Bits	Definition	Comments
				0..34.	
	31:30	Reserved	2		
2	15:0 31:16	mvx_l0[0][15:0] mvx_l0[1][15:0]	64	16-bit each	[0] in the least sig position in Z-order (1st index starts at LSB and goes up)
3	15:0 31:16	mvx_l0[2][15:0] mvx_l0[3][15:0]			
4	15:0 31:16	mvy_l0[0][15:0] mvy_l0[1][15:0]	64	16-bit each	in Z-order (1st index starts at LSB and goes up)
5	15:0 31:16	mvy_l0[2][15:0] mvy_l0[3][15:0]			
6	15:0 31:16	mvx_l1[0][15:0] mvx_l1[1][15:0]	64	16-bit each	in Z-order (1st index starts at LSB and goes up)
7	15:0 31:16	mvx_l1[2][15:0] mvx_l1[3][15:0]			
8	15:0 31:16	mvy_l1[0][15:0] mvy_l1[1][15:0]	64	16-bit each	in Z-order (1st index starts at LSB and goes up)
9	15:0 31:16	mvy_l1[2][15:0] mvy_l1[3][15:0]			
10	3:0 7:4 11:8 15:12	reserved[0] intra_chroma_mode1[2:0] reserved[0] intra_chroma_mode2[2:0] reserved[0] intra_chroma_mode3[2:0] reserved[3:0]		3-bits each	
10	3:0 7:4 11:8 15:12	ref_idx_l0[0][3:0] ref_idx_l0[1][3:0] ref_idx_l0[2][3:0] ref_idx_l0[3][3:0]	16	4-bit each	in Z-order (1st index starts at LSB and goes up)
	19:16 23:20 27:24 31:28	ref_idx_l1[0][3:0] ref_idx_l1[1][3:0] ref_idx_l1[2][3:0] ref_idx_l1[3][3:0]	16	4-bit each	Combined list is not supported in Z-order (1st index starts at LSB and goes up)
11		tu_size[15:0]	32	0: 4x4	in Z-order (1st index starts at LSB and goes up)
				1: 8x8	
				2: 16x16	
				3: 32x32	
12	15:0	tu_xform_Yskip[15:0]	16	0: TU transform skip flag for luma	In Z-order (1st index starts at LSB and goes up). Populated for each TU even if transform skip

DWord	Bitfield	Field	Bits	Definition	Comments
				component is not set (normal transform) 1: TU transform skip flag for luma component is set	is not supported for that particular TU size. This bit should not be set to 1 if transquant_bypass=1
	27:16	Reserved	12		
	31:28	tu_countm1[3:0]	4	number of TU count per CU minus 1	Intel restriction max 16 TU per CU (however spec allows up to 256 TUs). If there is no TU inside a CU, it is indicated by cbf and skip flag.
13	15:0	tu_xform_Uskip[15:0]	16	0: TU transform skip flag for chroma cb component is not set (normal transform) 1: TU transform skip flag for chroma cb component is set	Indexed by tu_xform_Yskip index. Populated for each TU even if transform skip is not supported for that particular TU size. For the case where a 4x4 chroma TU is associated with a group of four 4x4 luma TUs the chroma cb transform skip is coded in the same position as the last 4x4 luma TU (the prior 3 indexed positions are skipped/ignored). For example an 8x8 CU with four 4x4 luma TUs would code the chroma cb TU transform skip flag as tu_xform_Uskip[3]. Restriction: For 422, 2 TUs for each Chroma correspond to 1 Luma TU share the same transformskip flag. This bit should not be set to 1 if transquant_bypass=1
	31:16	tu_xform_Vskip[15:0]	16	0: TU transform skip flag for chroma cr component is not set (normal transform) 1: TU transform skip flag for chroma cr component is set	Indexing identical tu_xform_Uskip. Populated for each TU even if transform skip is not supported for that particular TU size. This bit should not be set to 1 if transquant_bypass=1

Intel restriction max 16 TU per CU, max 256 TUs in a CU.

Max 64 CUs, and each CU record max is 1 cacheline 64 bytes in size (1 cacheline 64 bytes)

LCU, CU, TU, and PU Sizes – Encoder Only

LCU/CU Partitioning Configurations

LCU size	min CU size	CU Depth	Hierarchical Depth=CU Depth+1
64x64	64x64	0	1
	32x32	1	2
	16x16	2	3
	8x8	3	4
32x32	32x32	0	1
	16x16	1	2
	8x8	2	3
16x16	16x16	0	1
	8x8	1	2
8x8	8x8	X	Not allowed in spec

PU Options for a Given CU

Current CU size (leaf node)	min CU sizes (Pic State)	Allowed PU partition types.
64x64 (2Nx2N) Must be a LCU	64x64	Skip : 2Nx2N Intra : 2Nx2N, NxN Inter : 2Nx2N, 2NxN, Nx2N, NxN
	32x32	Skip : 2Nx2N Intra : 2Nx2N (no NxN defined in the spec.) Inter :

		2Nx2N, 2NxN, Nx2N, 2NxnU, 2NxnD, nLx2N, nRx2N
	16x16	Skip : 2Nx2N Intra : 2Nx2N (no NxN defined in the spec.) Inter : 2Nx2N, 2NxN, Nx2N, 2NxnU, 2NxnD, nLx2N, nRx2N
	8x8	Skip : 2Nx2N Intra : 2Nx2N (no NxN defined in the spec.) Inter : 2Nx2N, 2NxN, Nx2N, 2NxnU, 2NxnD, nLx2N, nRx2N
32x32 (2Nx2N) Can or is not a LCU	32x32	Skip : 2Nx2N Intra : 2Nx2N,

		NxN Inter : 2Nx2N, 2NxN, Nx2N, NxN
	16x16	Skip : 2Nx2N Intra : 2Nx2N Inter : 2Nx2N, 2NxN, Nx2N, 2NxnU, 2NxnD, nLx2N, nRx2N
	8x8	Skip : 2Nx2N Intra : 2Nx2N Inter : 2Nx2N, 2NxN, Nx2N, 2NxnU, 2NxnD, nLx2N, nRx2N
16x16 (2Nx2N) Can or is not a LCU	16x16	Skip : 2Nx2N Intra : 2Nx2N, NxN Inter : 2Nx2N, 2NxN, Nx2N, NxN
	8x8	Skip :

		2Nx2N Intra : 2Nx2N Inter : 2Nx2N, 2NxN, Nx2N, 2NxnU, 2NxnD, nLx2N, nRx2N
8x8 (2Nx2N) Cannot be a LCU	8x8	Skip : 2Nx2N Intra : 2Nx2N and NxN Inter : 2Nx2N, 2NxN, Nx2N (both NxN and AMP are not allowed for 8x8 inter CU)

Note: In an 8x8 Inter CU NxN isn't allowed if the SPS parameter disable_inter_4x4 is 1. In Main profile currently this flag is always 1.

U.D, L and R (Up, Down, Left and Right)

n = ¼ or – .

TU Partitioning for a Given CU

CU size	TU size	TU Depth	Max Depth=TU Depth+1	PAK supported TU sizes and corresponding number of TUs in CU
64x64	64x64	0	1	no 64x64 transform, so automatically breakdown into 4 32x32 TUs.
	32x32	1	2	number of TUs in CU = 4
	16x16	2	3	number of TUs in CU = 16
	8x8	3	4	this configuration is currently not supported.

	4x4	4	5	this configuration is currently not supported.
32x32	32x32	0	1	number of TUs in CU = 1
	16x16	1	2	number of TUs in CU = 4
	8x8	2	3	number of TUs in CU = 16
	4x4	3	4	this configuration is currently not supported.
16x16	16x16	0	1	number of TUs in CU = 1
	8x8	1	2	number of TUs in CU = 4
	4x4	2	3	number of TUs in CU = 16
8x8	8x8	0	1	number of TUs in CU = 1
	4x4	1	2	number of TUs in CU = 4

The actual level of partitioning is governed by

- MaxTUSize and MinTUSize in Pic State.
- max_transform_hierarchy_depth_inter <= 2 (intel restriction) DW4 bit 3:2 Pic State
- max_transform_hierarchy_depth_intra <= 2 (intel restriction) DW4 bit 1:0 Pic State

Allowed LCU Size – Encoder Only

The following table details the LCU size allowed and the number of records per LCU for the encoder.

LCU Size Allowed	Fixed Number of Records per LCU
64x64	64
32x32	16
16x16	4

Note: 0.5 CL per CU record in VME mode and 1 CL per CU record in extENC mode.

HEVC Error Concealment

The HCP implements an error concealment policy, which is always enabled and cannot be disabled. The objective is that the HCP will always complete a frame/field workload by either decoding the bit stream normally until it finishes the workload or by concealing blocks until the slice or workload is completed. It should never be allowed to hang.

Error concealment, implemented by the HCP hardware, is configured for each slice in the HCP_BSD_OBJECT command. The following information in the HCP_BSD_OBJECT command is utilized for error concealment.

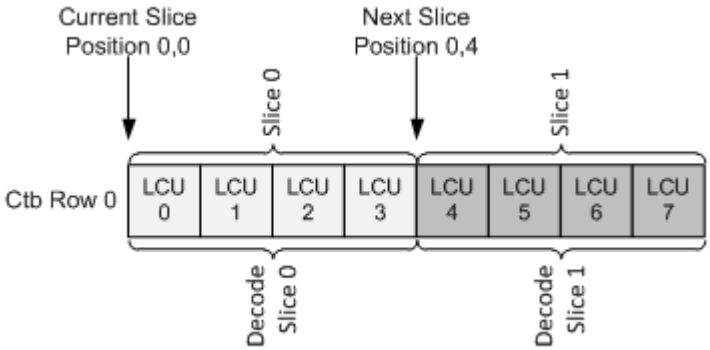
- **SliceStartCtbY, SliceStartCtbX:** The current slice position specified in Ctb coordinates.
- **NextSliceStartCtbY, NextSliceStartCtbX:** The next slice position specified in Ctb coordinates. If the current slice is the last slice in the picture, the next slice values are set to (0,0).
- **LastSliceofPic:** Indicates that the current slice is the last slice in the picture.
- **slice_type:** Indicates the picture type: I, P or B.

The host software will remove all extra slices in the picture. The HCP will not be given a workload that includes extra slices beyond the picture. The last slice in the picture will always be marked by the host software.

The host software will remove any overlapping slices in the picture. The HCP will not be given a workload that includes overlapping slices in the picture.

A HCP_BSD_OBJECT command will include the current slice position and the next slice position. For non-errored streams, it is guaranteed that the slice bit stream will be decoded by the HCP starting from the current slice position through to the Ctb (inclusive) adjacent to the Ctb indicated by the next slice position. *HEVC Error Concealment* illustrates the example of a non-errored stream decode starting with XXX.

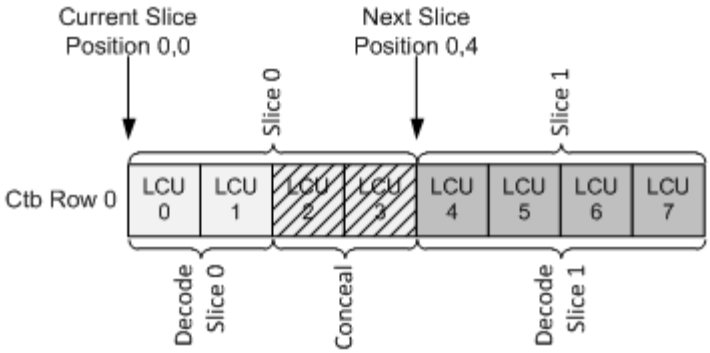
HEVC Slice Decode for Non-errored Stream Cases



For error stream cases where the next slice position does not align itself with the last successfully decoded Ctb in the current slice, the HCP will conceal Ctbs from the last decoded Ctb in the current slice through to the last Ctb prior to the Ctb indicated by the next slice position. If the error occurs such that the current decoded Ctb cannot be decoded, the HCP will ensure that the current Ctb is written out by

any means before writing out concealed Ctbs for the remaining Ctbs in the current slice. In the case of the last slice in a picture, the HCP will conceal Ctbs from the last decoded Ctb in the current slice through to the last Ctb position in the picture indicated by the resolution of the picture in the HCP_PICT_STATE command. *HEVC Error Concealment* illustrates the case described.

HEVC Slice Decode for Missing Blocks in a Slice



Since the host software removes overlapping slices, the next slice position will never be equal to or less than the current slice position.

A concealed Ctb for an I-slice is constructed by the HCP specifying the Intra_Planar prediction mode for the Ctb.

A concealed Ctb for a P-slice is constructed by the HCP specifying the skip_flag.

A concealed Ctb for a B-slice is constructed by the HCP specifying the skip_flag.

VP9 Register Definitions

This section describes the VP9 Register Definitions as follows:

- Register Attributes Description
- VP9 Register Map
- VP9 Encoder Register Descriptions

Register Attributes Description

Host Register Attributes gives the defined register tags and their description.

Host Register Attributes

Tag	Name	Description
R/W	Read/Write	Bit is read and writeable.
R/SW	Read/Special Write	Bit is readable. Write is only allowed once after a reset.
RO	Read Only	Bit is only readable, but writes have no effects.
WO	Write Only	Bit is only writeable, reads return zeroes.
RV	Reserved	Bit is reserved and not visible. Reads will return 0, and writes have no effect.
NA	Not Accessible	This bit is not accessible.

VP9 Register Map

These are MMIO register definitions for decoder/encoder:

VP9 Encoder Register Descriptions

HCP_IMAGE_STATUS_MASK - HCP Image Status Mask

HCP_IMAGE_STATUS_CONTROL - HCP Image Status Control

HCP_UNIT_DONE - HCP Unit Done

HEVC Register Definitions

The Message Channel Interface is a read-only bus used to access the HCP status registers. All registers are 32 bits where reserved bits return a value of zero and subtractive-decode is used to return 0x0000 for all register holes. The Unit ID is 28h. For HCP, the address range is 0x0001E900h to 0001E9FFh.

Register Attributes Description

Host Register Attributes gives the defined register tags and their description.

Host Register Attributes

Tag	Name	Description
R/W	Read/Write	Bit is read and writeable.
R/SW	Read/Special Write	Bit is readable. Write is only allowed once after a reset.
RO	Read Only	Bit is only readable, but writes have no effects.
WO	Write Only	Bit is only writeable, reads return zeros.
RV	Reserved	Bit is reserved and not visible. Reads will return 0, and writes have no effect.
NA	Not Accessible	This bit is not accessible.

HCP Decoder Register Map

This documents all HEVC Decoder MMIO Registers.

HCP Decoder Register Descriptions

The HCP implements the following MMIO registers. A description of the register including its address and DWord descriptions are provided.

HCP CABAC Status

HCP Picture Checksum cIdx0

HCP Picture Checksum cIdx1

HCP Picture Checksum cIdx2

HCP Encoder Register Map

These are MMIO register definitions for encoder.

HCP Encoder Register Descriptions

HCP_FRAME_PERFORMANCE_CT - HCP Frame Performance Count

HCP_LAT_CT1 - HCP Memory Latency Count1

HCP_LAT_CT2 - HCP Memory Latency Count2

HCP_LAT_CT3 - HCP Memory Latency Count3

HCP_LAT_CT4 - HCP Memory Latency Count4

HCP_LAT_CT5 - HCP Memory Latency Count5

HCP_LAT_CT6 - HCP Memory Latency Count6

HCP_BIN_CT - HCP Frame BitStream BIN Count

HCP_READ_CT - HCP Frame Motion Comp Read Count

HCP_MISS_CT - HCP Frame Motion Comp Miss Count

HCP_BITSTREAMSE_BITCOUNT_FRAME - Reported Bitstream Output Bit Count for Syntax Elements Only

HCP_CABAC_BIN_COUNT_FRAME - Reported Bitstream Output CABAC Bin Count Register

HCP_CABAC_INSERTION_COUNT - Reported Bitstream Output CABAC Insertion Count

HCP_MINSIZE_PADDING_COUNT - Bitstream Output Minimal Size Padding Count Report Register

HCP_IMAGE_STATUS_CONTROL - HCP Image Status Control

HCP_QP_STATUS_COUNT - HCP Qp Status Count

HCP_UNIT_DONE - HCP Unit Done

HCP_IMAGE_STATUS_MASK - HCP Image Status Mask

HUC Status Register Descriptions

Following are HUC Status Register Descriptions:

UKERNEL_HDR_INFO - uKernel Header Info

Acronyms and Applicable Standards

Acronyms and Abbreviations

The table below defines acronyms and abbreviations used in this document.

Acronyms

Acronym	Meaning
AAC	Advanced Audio Coding — part of the MPEG specification, AAC is the latest development in audio compression. It provides higher-quality audio reproduction than MPEG-1 Layer 3 (MP3), while requiring nearly 50% less data. It is defined in ISO/IEC 13818-7.
ADSL	Asymmetrical Digital Subscriber Line — an asymmetrical DSL technology that takes advantage of the one-way nature of most multimedia communication, and provides much faster data rates for downstream (to the subscriber) then the upstream.
API	Application Programming Interface — a set of routines used by an application program to request and carry out low-level services performed by the operating system.
ARGB	Alpha Red Green Blue — color channel components.
ARIB	Association of Radio Industries and Business — designated by the Ministry of Public Management, Home Affairs, Posts and Telecommunications (MPHPT) in Japan. ARIB members include broadcasters, radio equipment manufacturers, telecommunication operators, and related organizations.
ASP	Advanced Simple Profile – MPEG4-2
ATSC	ATSC Advanced Television Systems Committee – an organization in US that establishes and promotes technical standards for advanced television systems, such as digital television (DTV).

Acronym	Meaning
BDU	Bit-stream Data Unit
BIST	Built In Self Test
BPP	Bits Per Pixel
BSD	Byte Stream Decoder
CA, CAM	Conditional Access, Conditional Access Module – the removable descrambling module implemented in digital cable or satellite television system. The data flows through the module, which can have any proprietary scrambling algorithm implemented, yet maintaining system interface compatibility. The CAMs are usually provided by the operators in the TV network.
CPU	Central Processing Unit
DAA	Direct Access Arrangement
DAC	Digital-to-Analog Converter
DDA	Digital Difference Analyzer
DDS	Direct Digital Synthesizer
DPB	Decoded Picture Buffer. This buffer holds the decoded pictures for reference and for output along with the currently decoding picture. This differs from the DPB in the standard, which only holds the decoded pictures for reference.
DVB	Digital Video Broadcasting — a set of open worldwide standards that define digital broadcasting using existing satellite, cable, and terrestrial infrastructures. It uses MPEG-2 specification as a universal foundation and expands it with DVB data structures and processes DVB-compliant digital broadcasting and equipment is widely available to consumers and is indicated with the DVB logo.
DVB-S	Satellite television DVB standards, based on QPSK and 8-DPSK modulation.
DVB-T	Terrestrial television DVB standards, based on 2k and 8k OFDM modulation.
DVD	Digital Versatile Disc
DVD-R	Recordable DVD. Since different disk formats are currently in use, including DVD-R,DVD+R, they are collectively mentioned as DVD-R in this document
DVI	Digital Visual Interface standard (EIA/CEA-861A). The standard defines a method for sending digital video signals over DVI and OpenLDI interface specifications. The standard is fully backward compatible with earlier DVI standards. New features include carrying auxiliary video information, such as aspect ratio and native video format information.
DVO	Digital Video Output - the parallel, low voltage signaling interface defined for Intel® video chipsets
DSL xDSL	Digital Subscriber Line – transmission of data over copper telephone lines capable of bringing high-bandwidth to subscribers. Many flavors of DSL are currently in use, which are collectively called xDSL throughout the document.
DSP	Digital Signal Processor
DST	Destination
DWord	A 32-bit word
ES	Elementary Streams — the raw output of an encoder, containing only what is necessary for a decoder to approximate the original picture or audio.
FIFO	First in First Out

Acronym	Meaning
FIR	Finite Impulse Response
FPU	Floating Point Unit
FW	Firmware running on the decoder controller, as used in Volume 4 of the *Olo River Plus Silicon EAS*
IDR	Instantaneous Decoding Refresh
IEEE 1394 1394	IEEE 1394 or iLink* or FireWire* An IEEE electronics industry standard for connecting multimedia and computing Up to 63 devices can be attached to your PC via a single plug-and-socket connection.
IEEE 802.11 802.11	The Institute for Electronics and Electrical Engineers (IEEE) wireless network specification. 802.11g and 802.11a networks can transmit payload at the rates in excess 34Mbits/s and allow for the wireless transmission at distances from several dozen to several hundred feet indoors.
IF	Intermediate Frequency — the fixed, relatively low-frequency carrier to which current programs are ported by the tuner.
GMCH	Graphics and Memory Control Hub — a chip that connects the IA processor to memory and other components in PC.
HDD	Hard Disk Drive — magnetic mass storage device used in media centers for audiovisual program recording.
HDMI	High Definition Multimedia Interface (HDMI). This interface is used between any audio/video source, such as a set-top box, DVD player, or A/V receiver, and an audio or video monitor, such as a DTV. HDMI supports standard, enhanced or high-definition video, plus multi-channel digital audio on a single cable. The format transmits all ATSC HDTV standards and supports eight-channel digital audio (at up to a 192kHz sampling rate), with bandwidth to spare for future enhancements.
HDTV	High-Definition Television — HDTV specifically refers to the highest-resolution formats of the 18 total DTV formats, true HDTV is generally considered to be 1,080-line interlaced (1080i) or 720-line progressive (720p).
HSR	Hidden Surface Removal
HW	Hardware
I/F	Interface
IEEE	IEEE 32-bit Floating Point number format representation
ISP	Image Synthesis Processor — A collective term to describe all components of the hidden surface removal operation within the PowerVR architecture.
LOD	Level Of Detail — used in texturing calculations.
LSB	Least Significant Bit
LUT	Look-up table
MBAFF	Block Adaptive Field Frame mode
MFD	Multi-Format Decoder
MMU	Memory Management Unit
MMMC	Multi-port, Multi-channel Memory Controller
MSA	Intel Micro Signal Architecture — microprocessor architecture combining the features of microcontroller and digital signal processor. MSA is used here as a synonym of the processor core

Acronym	Meaning
	used in Olo River Plus
MSB	Most Significant Bit
MPEG	Motion Picture Experts Group – Organization that develops standards for digital video and digital audio compression.
MPR	Inter Prediction Module
NAL	Network Abstraction Layer
NAL unit	Syntax structure in a H.264 stream
NTSC	National Television System Committee, North American 525-line analog broadcast TV standard.
NIM	Network Interface Module – the integrated tuner and digital demodulator in the (satellite) TV systems. The DVB NIMs output MPEG transport stream.
NOP	No operation
OEM	Original Equipment Manufacturer
OGL/OpenGL	Open GL application programming interface
PAL	Phase Alternation Line - TV standard used in Europe. PAL uses 625 lines per frame, a 25 frames per second update rate and YUV color encoding. The number of visible pixels for PAL video is 768 x 576.
PCI	Peripheral Component Interconnect bus, a bi-directional bus defined in PCI 2.x specification
PES	Packetized Elementary Streams — packetized streams are the ES streams arranged in data packets with PES header starting every packet. The syntax of the ES and PES is defined in MPEG. See definition for ES.
PIP	Picture In Picture display mode
POD	Point of Deployment conditional access module — the removable conditional access module defined in the OpenCable* specification in US.
PPS	Picture Parameter set
PTS	Presentation time stamp
PVR	Personal Video Recorder, also PDR or personal digital recorder — an interactive TV-recording device that records programs in digital format and allows users to search for/record shows based on type (for instance all basketball games or all episodes of a particular program). Users can also pause, rewind, stop, or fast-forward live programs with only a small time lag.
PWL	Piece-wise Linear
PXD	Pixel Decoder Module
RF	Radio Frequency – usually, modulated carriers which can be directly received by the tuners of TVs or radio receivers
RISC	Reduced Instruction Set Computer
RHW	Reciprocal Homogenous W — W is a 3-D coordinate representation like X Y Z
RSB	Row Store Buffer
RTL	Register Transfer Language/Level
SEI	Supplementary Enhancement Information

Acronym	Meaning
SIF	Semaphore Interface Module
SIMD	Single Instruction Multiple Data
SMPTE	Society of Motion Picture and Television Engineers
SOC	System on chip
SP	Simple Profile – MPEG4-2
SPS	Sequence Parameter set
SRC	Source
SDTV	Standard-Definition Television — a digital television system that is similar to current analog TV standards in picture resolution and aspect ratio. Typical SDTV resolution is 480i or 480p.
STB	Set Top Box — a device that effectively turns a television set into an interactive Internet device and/or allows the television to receive and decode digital television (DTV) broadcasts.
TA	Tile Accelerator
TS	MPEG-2 Transport Stream — a sequence of 188-byte packets carrying the multi-program audiovisual data
TSP	Texture Shading Processor — a collective term to describe all components of the texture, shading and pixel blending operations within the PowerVR architecture.
VCL	Video Coded Layer
VCXO	Voltage Controlled Crystal Oscillator
VGP/ VGP Lite	Vertex Geometry Processor
VLC	Variable length coded. This refers to the collection of coding techniques that are used in VC1, and include CABAC, CAVLC and Exp-Golomb.
VOL	Video Object Layer
VOP	Video Object Plane
WAN	Wide Area Network
WSS	Wide Screen Signaling
XDS	Extended Data Services — data services sending data in line 21/283 of the analog NTSC TV signal
XSI	Intel® XScale® System Interconnect
X, Y, Z, W	3-D coordinate representations
YUV	YUV texture format, primarily for video formats